

# LL1 Trigger Overview

Josh Perry

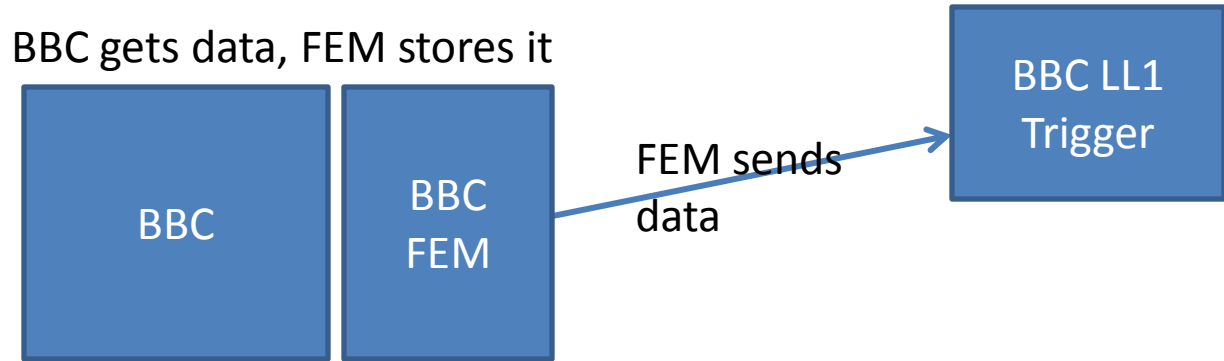
ISU

Spinfest 2013

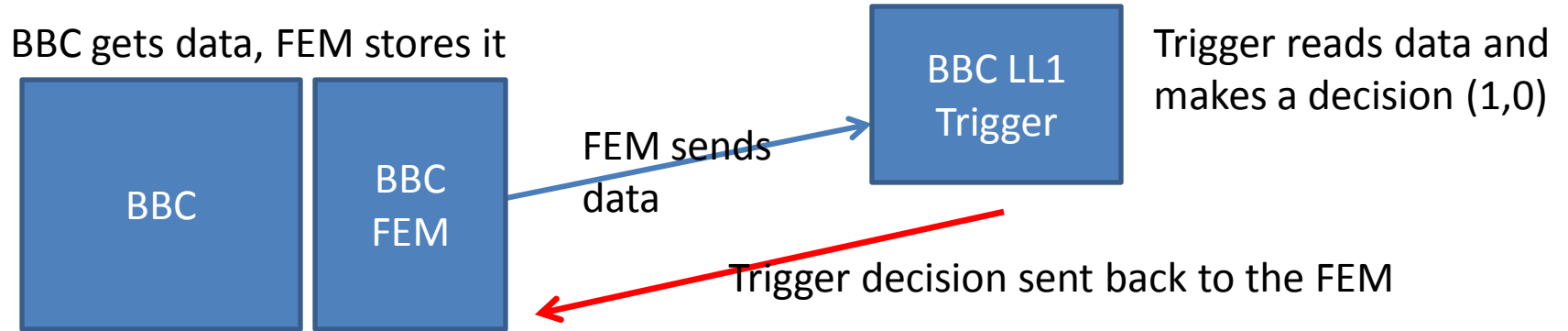
# Trigger theory

- Select out rare events
  - Note: We can only select out events which MIGHT be rare/good events!
- Suppress background and uninteresting events
- We have a given DAQ rate (6kHz)
  - We want to fill this DAQ rate without missing out on good events!

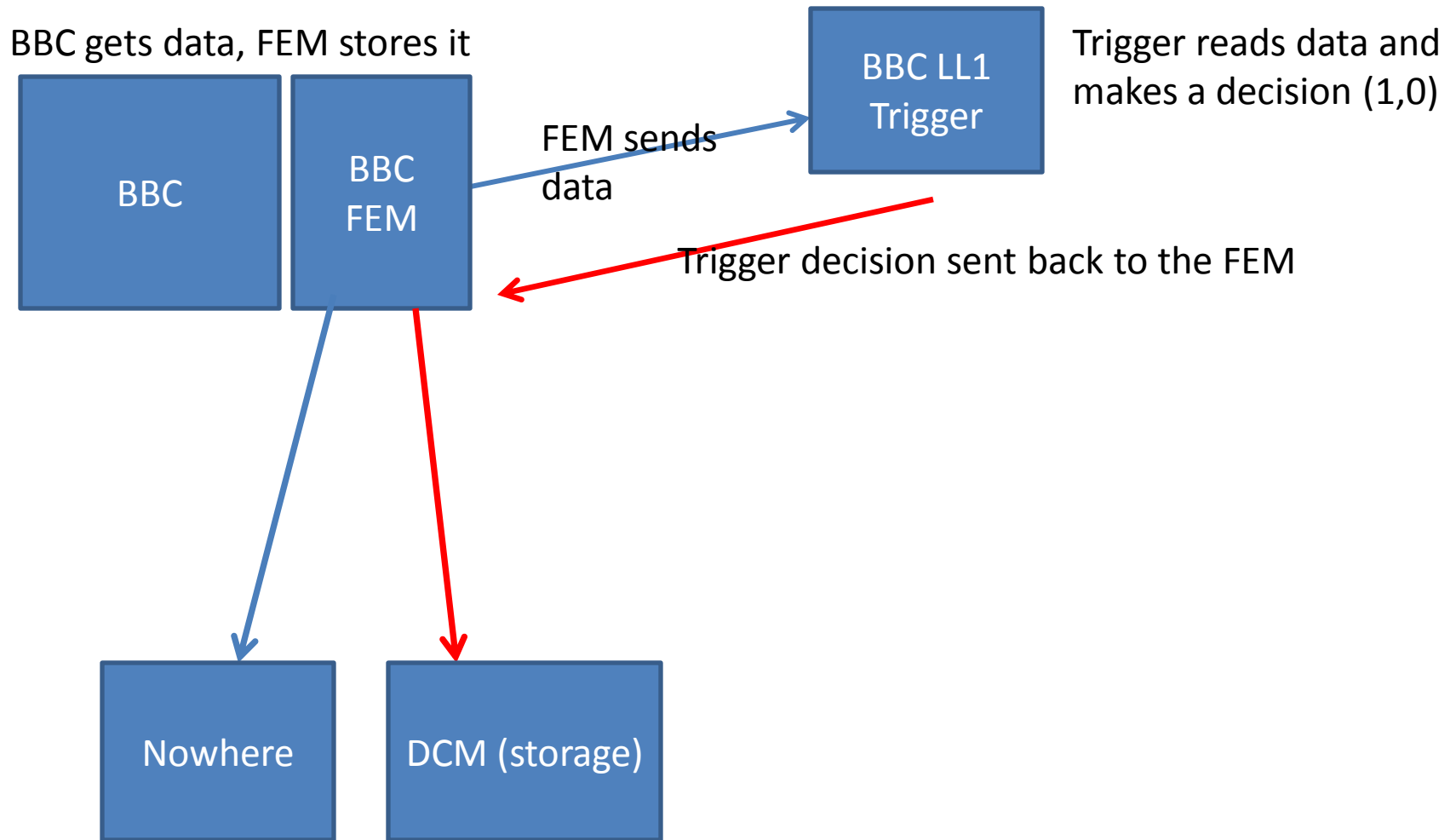
# One Detector Triggering (Instant)



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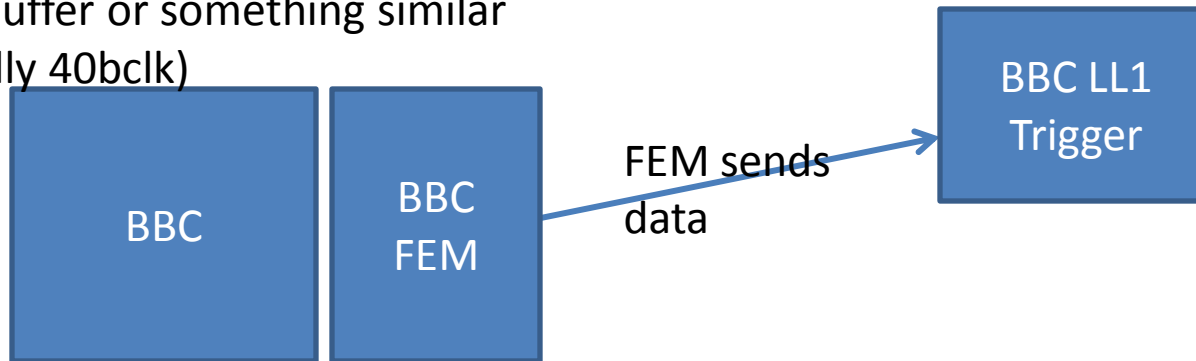


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# One Detector Triggering (Non-Instant)

BBC gets data, FEM stores it in a ring-buffer or something similar (usually 40bclk)

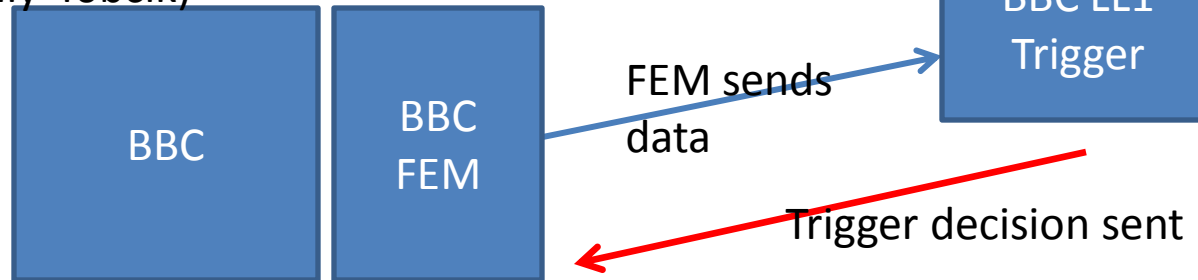


The BBC FEM does ADC on the FEM itself, so it has a long delay (many beam blocks) before the data is sent to LL1; Same with PC, TEC, DC, BBC, ZDC, MuTr (new), MuID, old MPC (using MuID FEMs)

Note: the AMU/ADC32 based FEMs digitize AFTER the accept signal from LL1: MuTr (old), EMC, RICH, ToF; this means the delay is shifted

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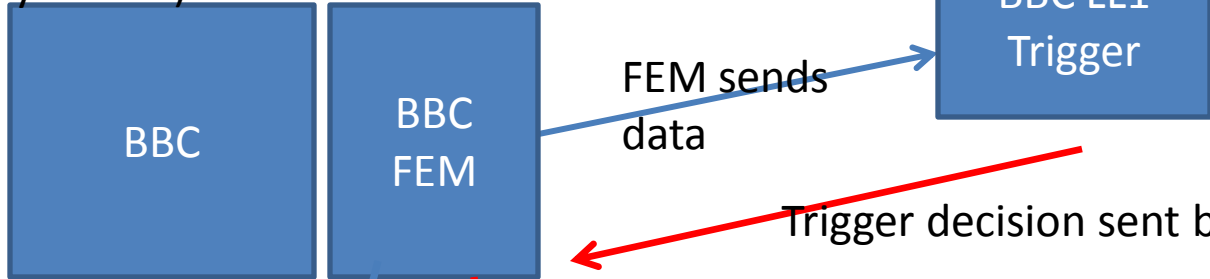
Trigger reads data and makes a decision (1,0). Note: the LL1s must be output a decision EVERY beam clock! If it doesn't, data is lost!

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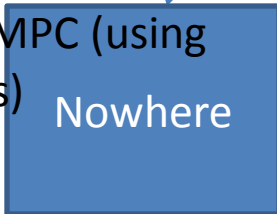
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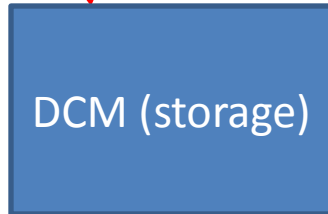


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Now the FEM needs to know WHICH data to send to the DCM! Timing becomes important. Did this whole round trip take 10 beam clocks? 22? 29?

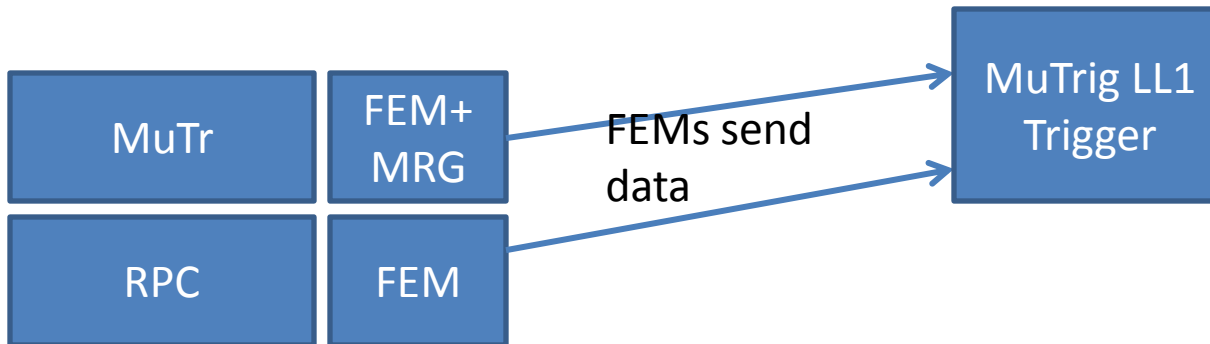
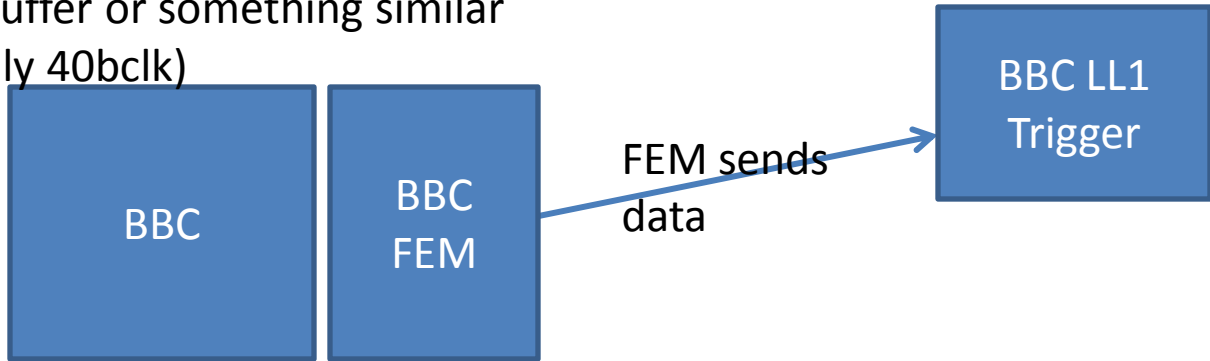


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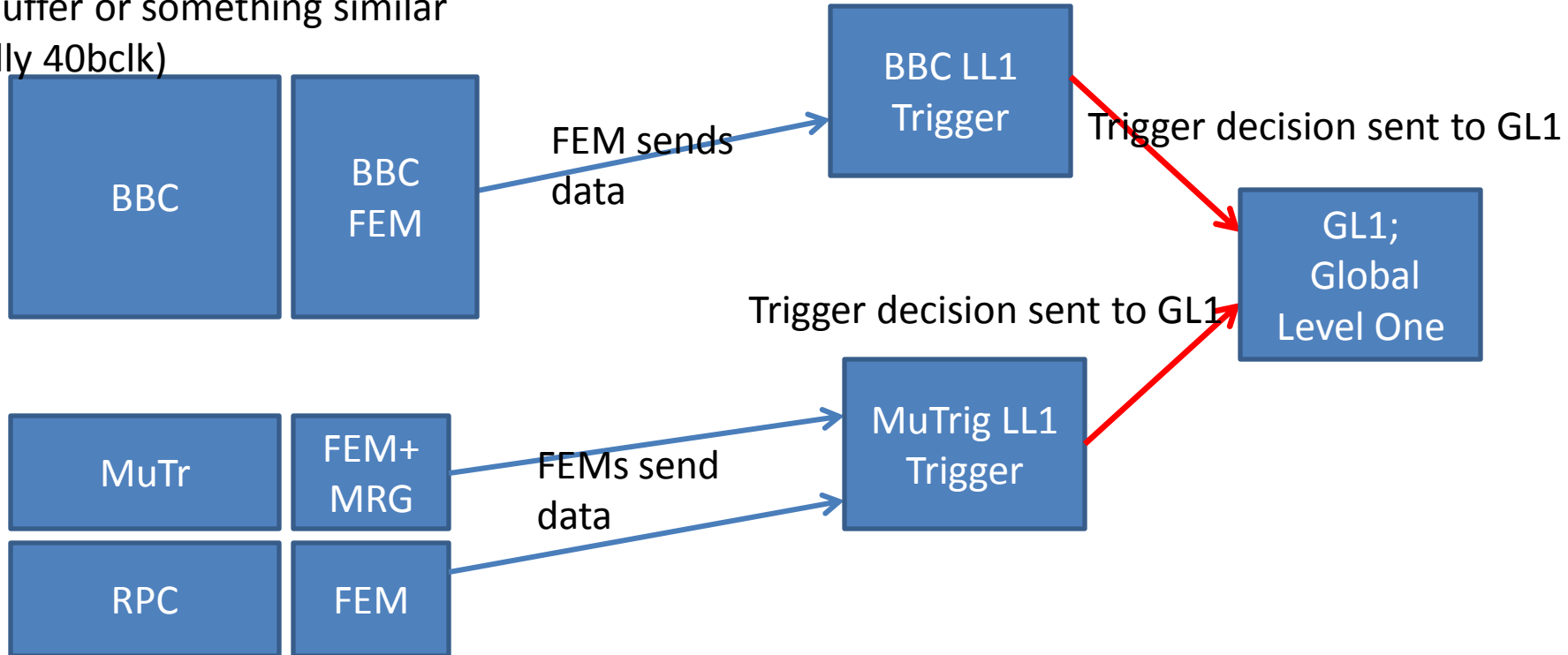
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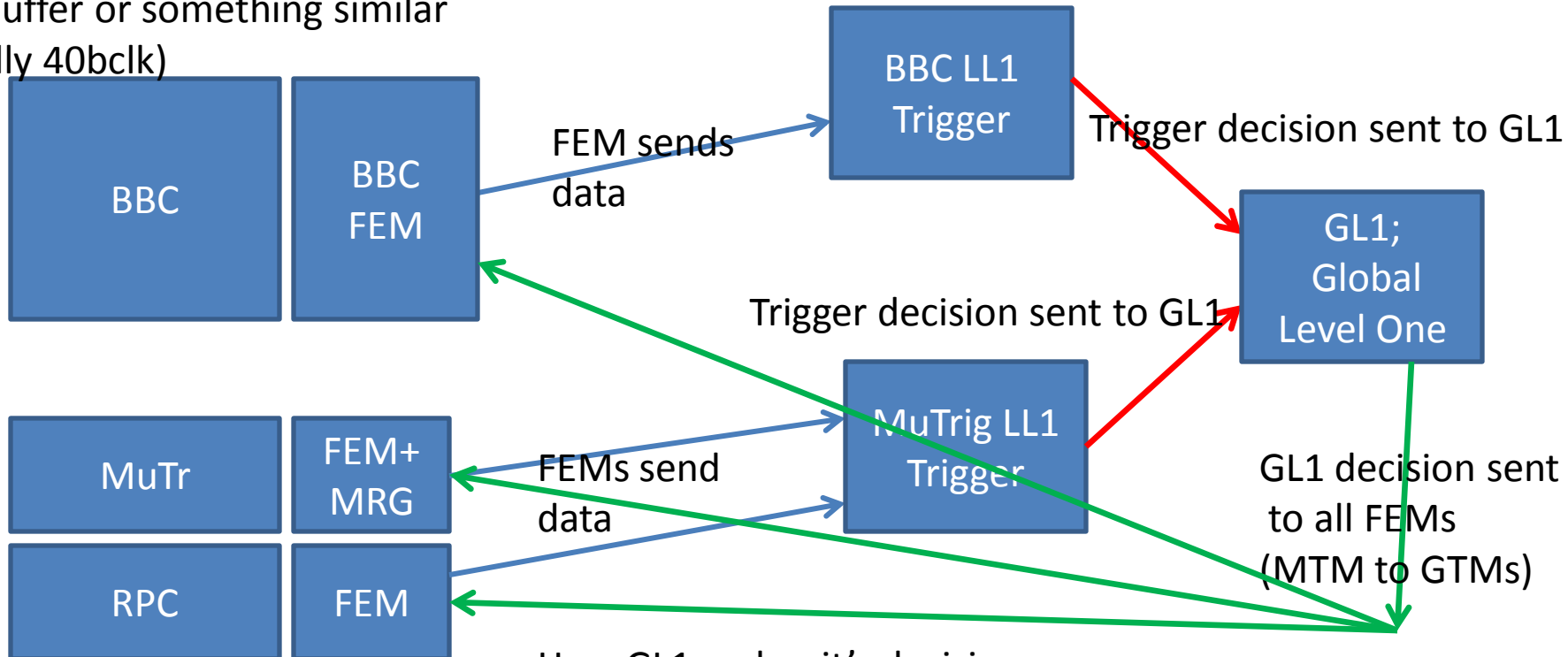
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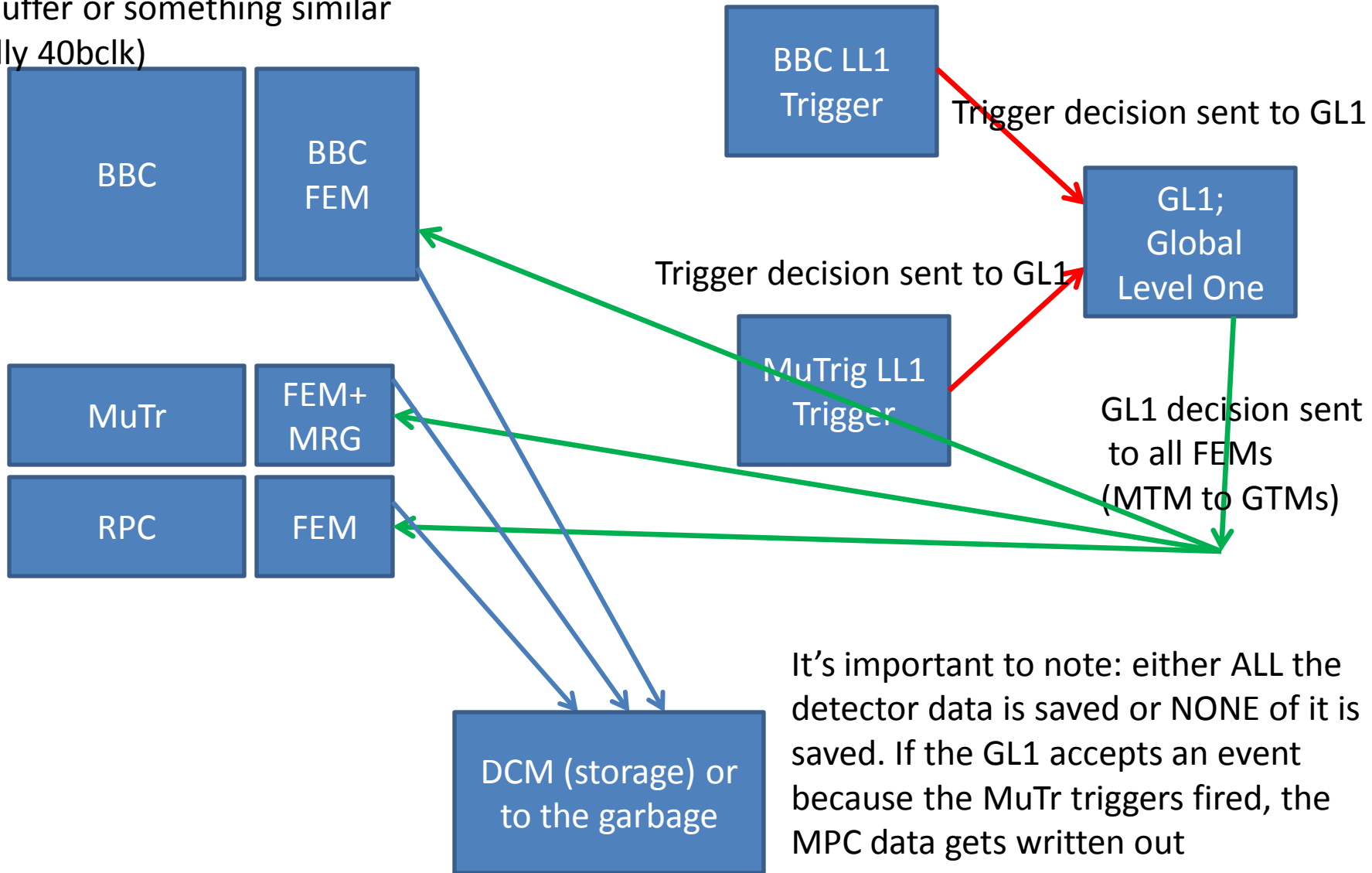


How GL1 makes it's decision:

Prescales. Prescales define how much weight we put on a specific mix of trigger's decision. If a detector is triggering too much (BBC(noVtx), for example), then the GL1 will ignore its pleas for a global accept. However, something like a SG1&BBC&RPC1&RPC3 trigger will never be ignored (prescale 0).

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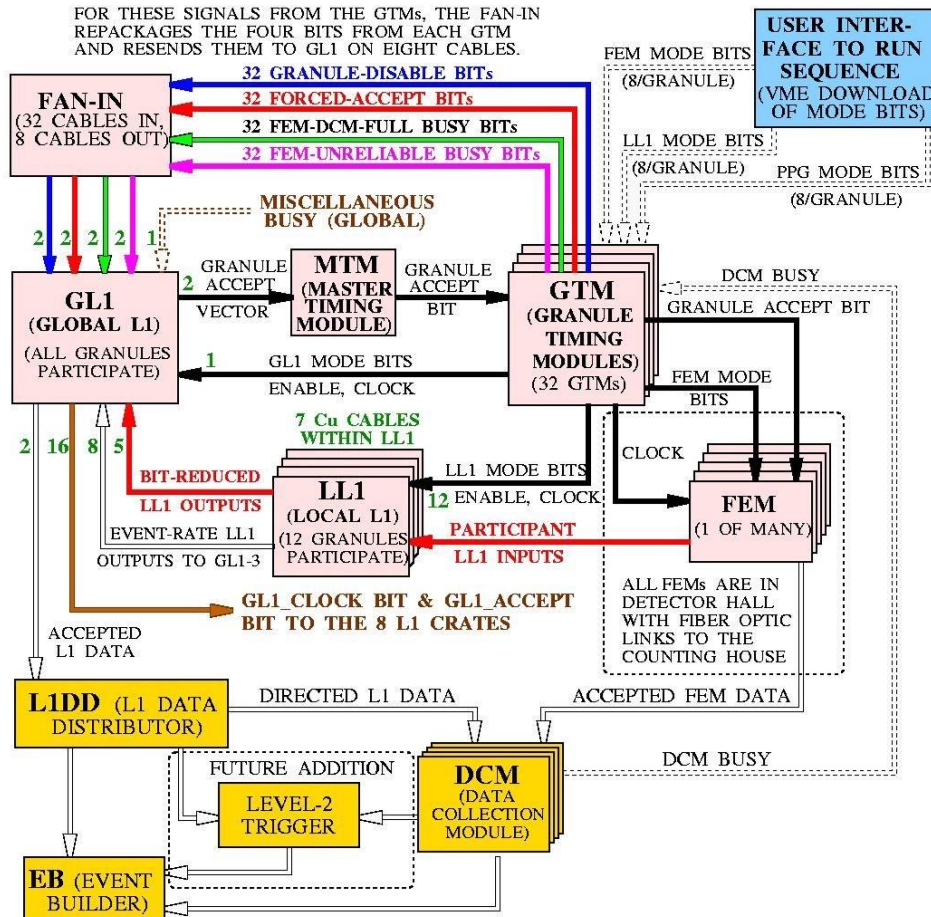


It's important to note: either ALL the detector data is saved or NONE of it is saved. If the GL1 accepts an event because the MuTr triggers fired, the MPC data gets written out

# A simplified view of the system

## COMMUNICATION LINKS/RATES FOR L1

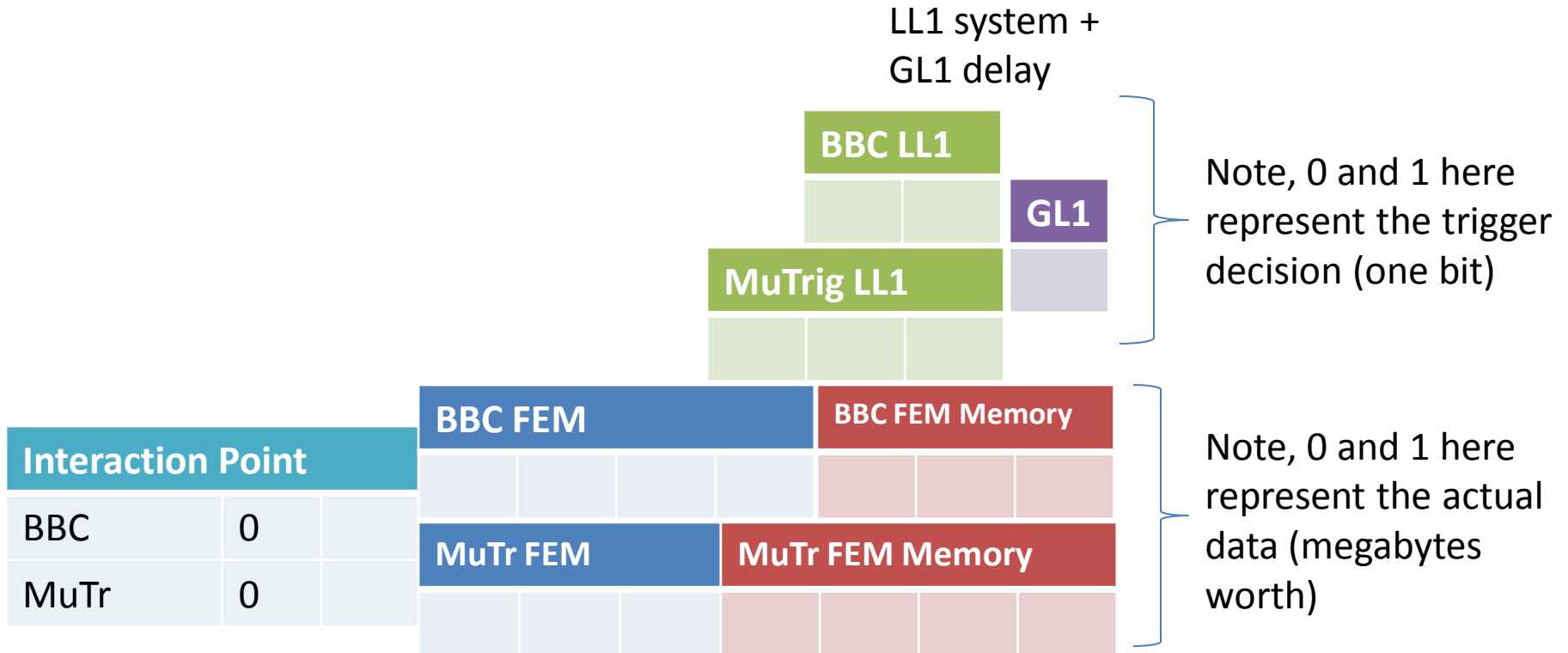
LEGEND:   
 ———▶ FILLED ARROWS FOR DATA TRANSFER AT BEAM CROSSING RATE   
 ———▶ EMPTY ARROWS FOR DATA TRANSFER AT ACCEPTED EVENT RATE   
 - - - - -▶ DASHED ARROWS FOR DATA TRANSFER AT ASYNCHRONOUS RATE   
 GREEN NUMBERS GIVE THE CU CABLES USED IN L1 (45 TOTAL).



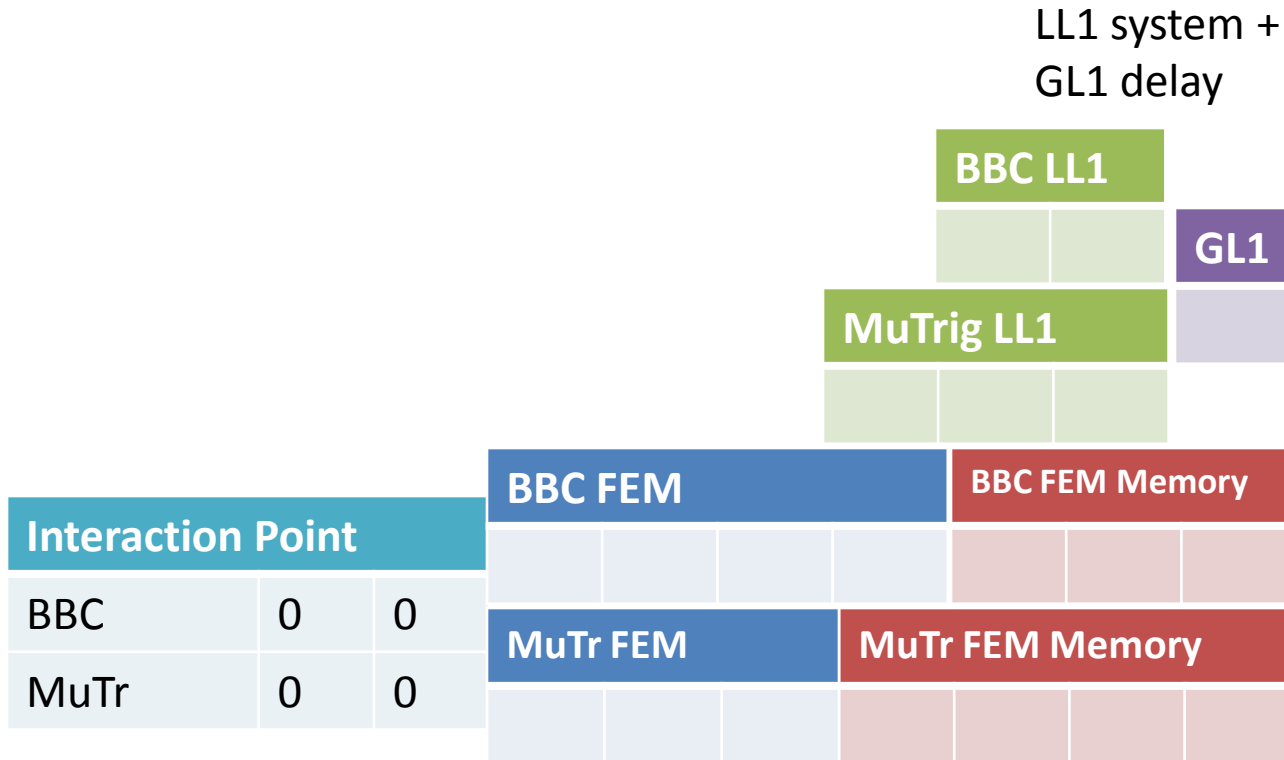
# Animation

- This is a crappy “animation” I made like three years ago and never showed anyone.

# If things are in time

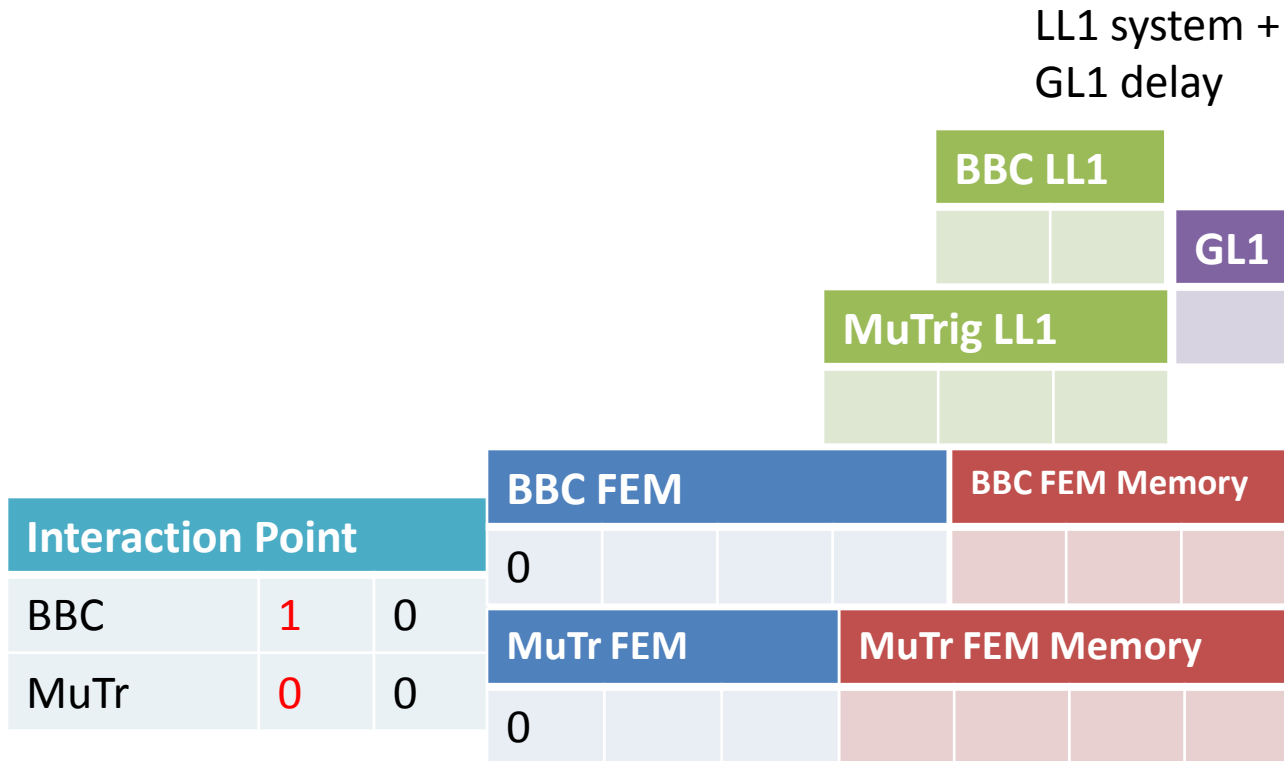


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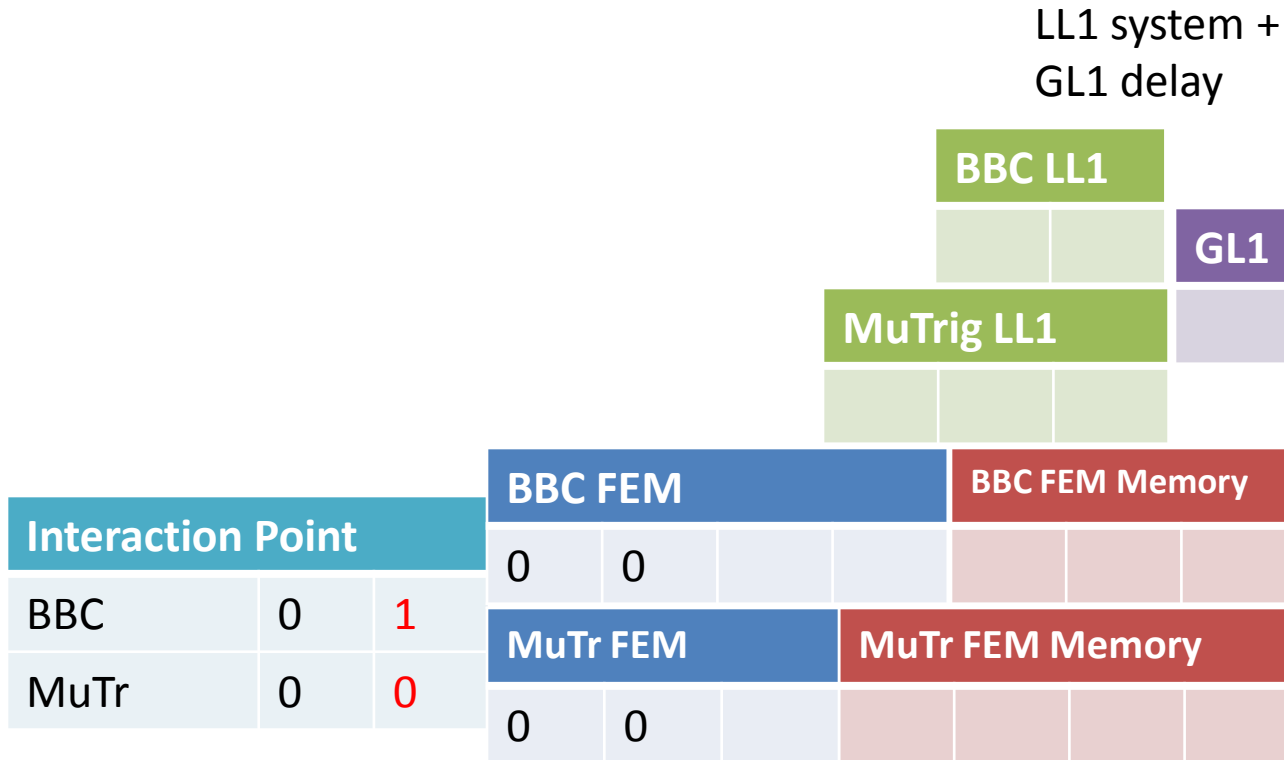




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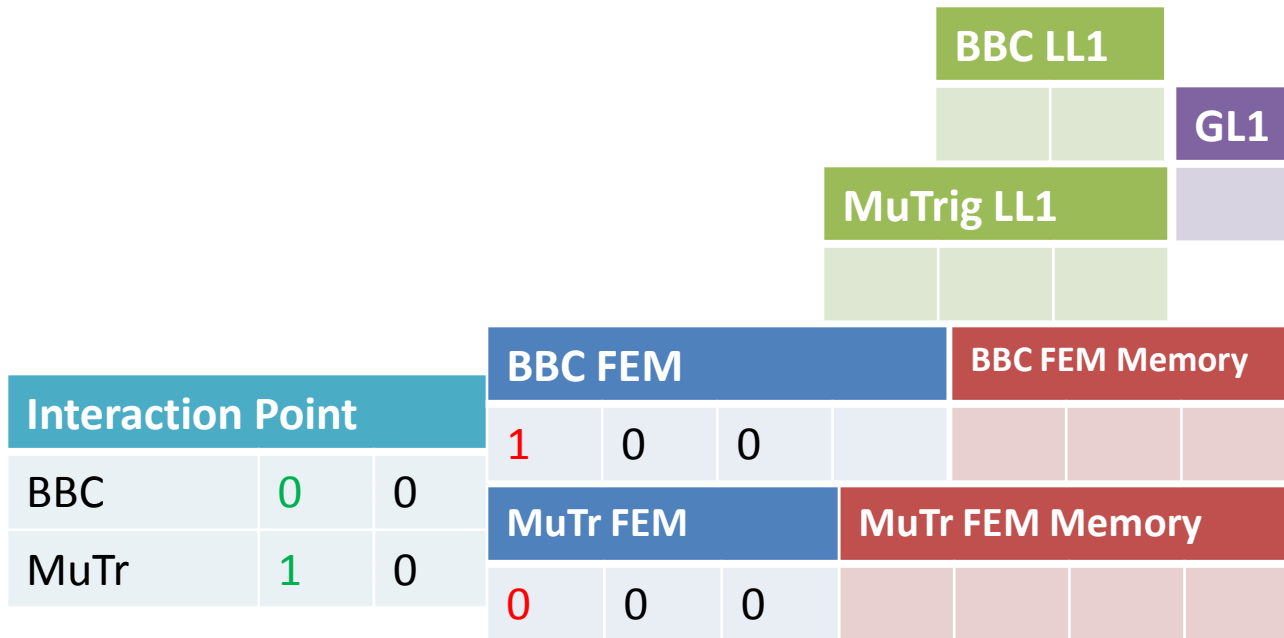


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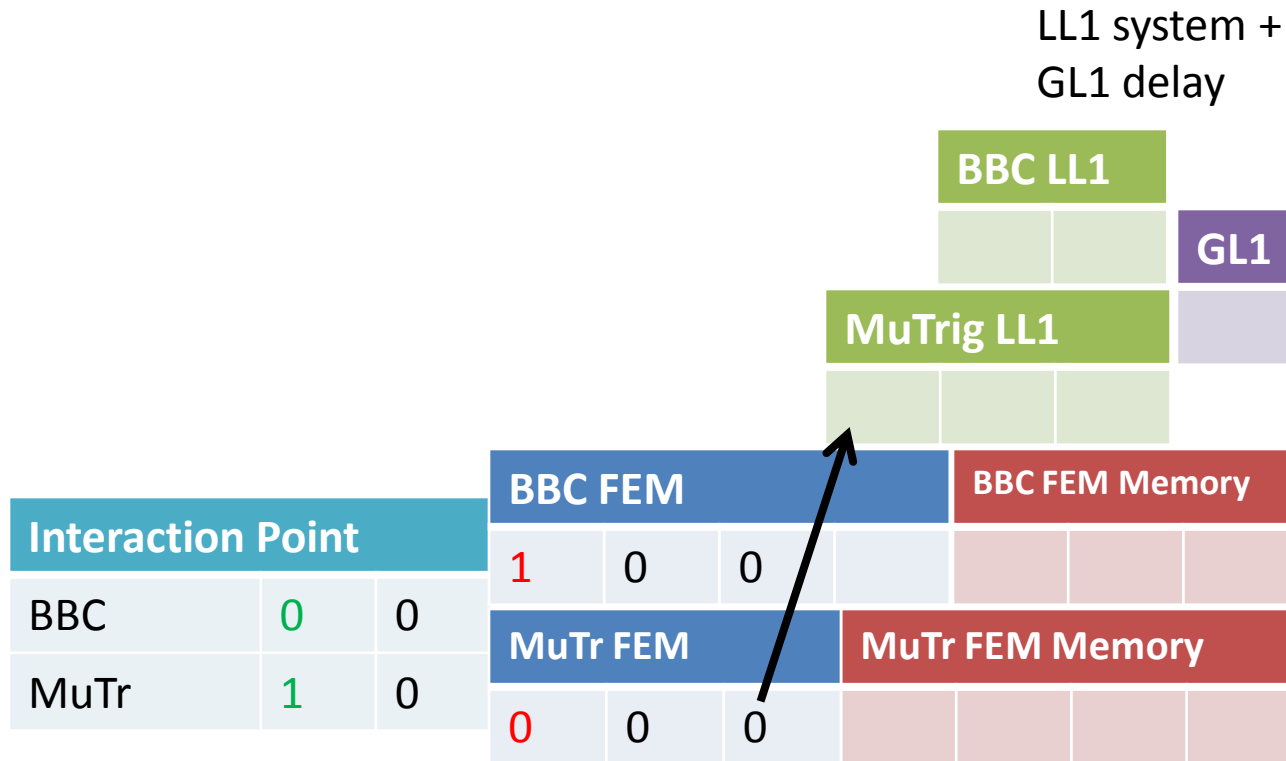


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LL1 system +  
GL1 delay

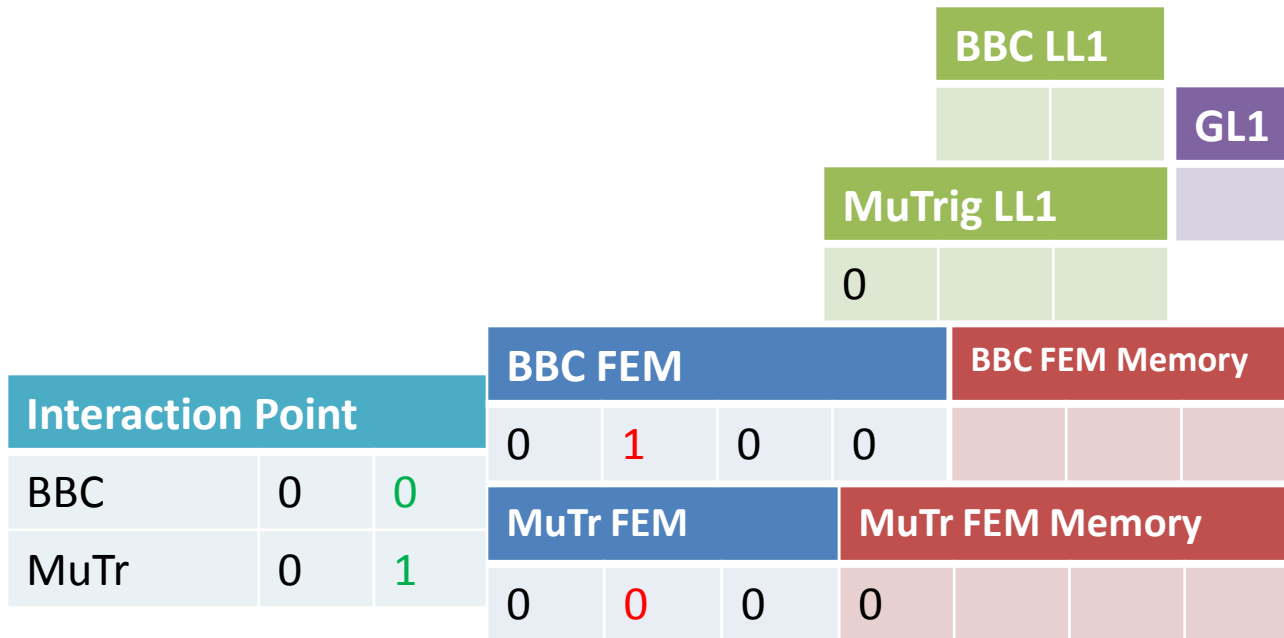


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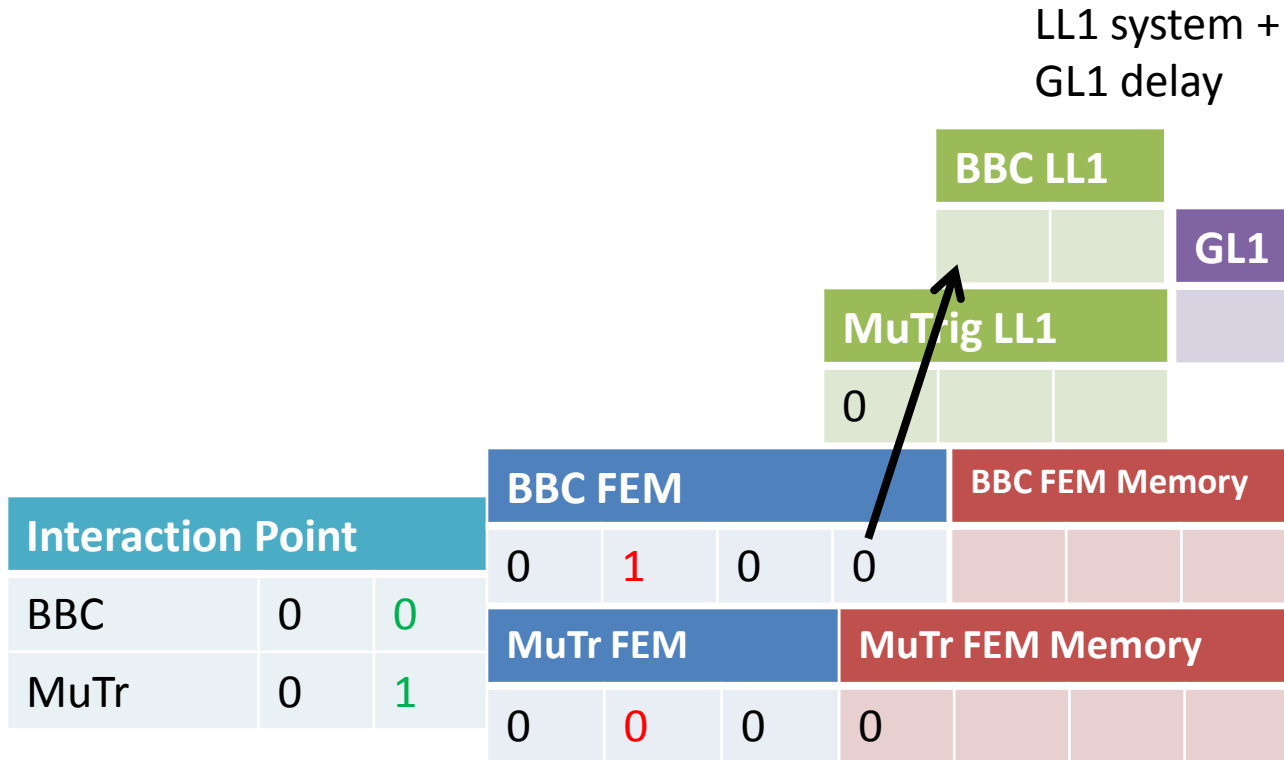


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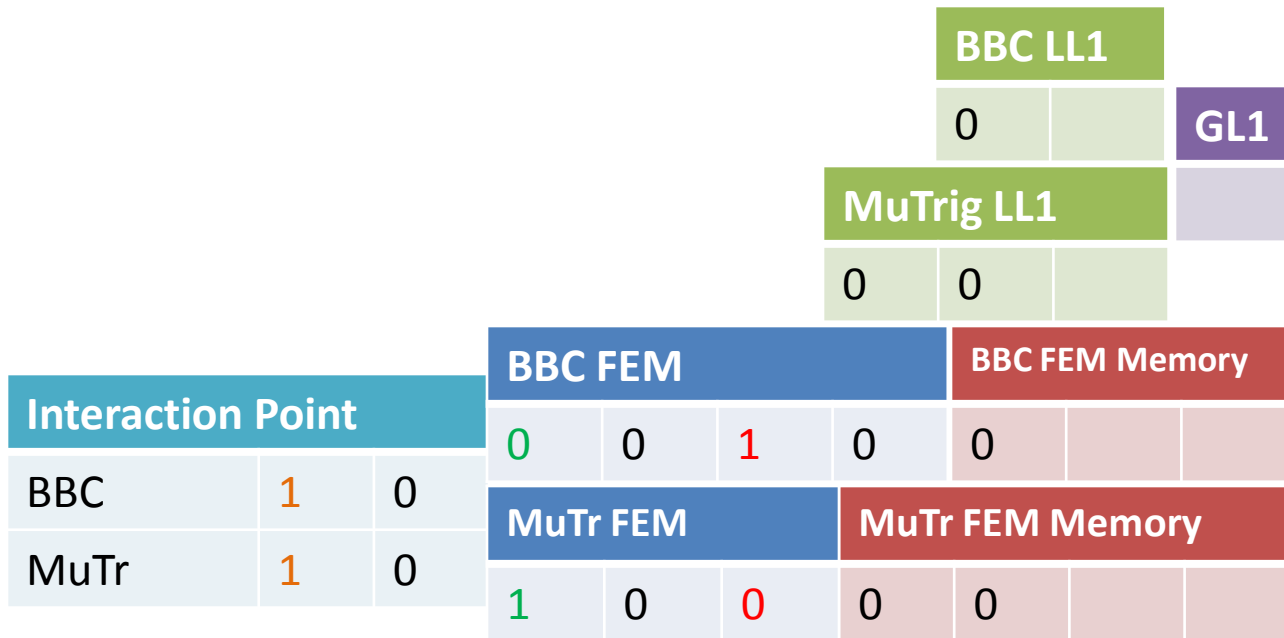


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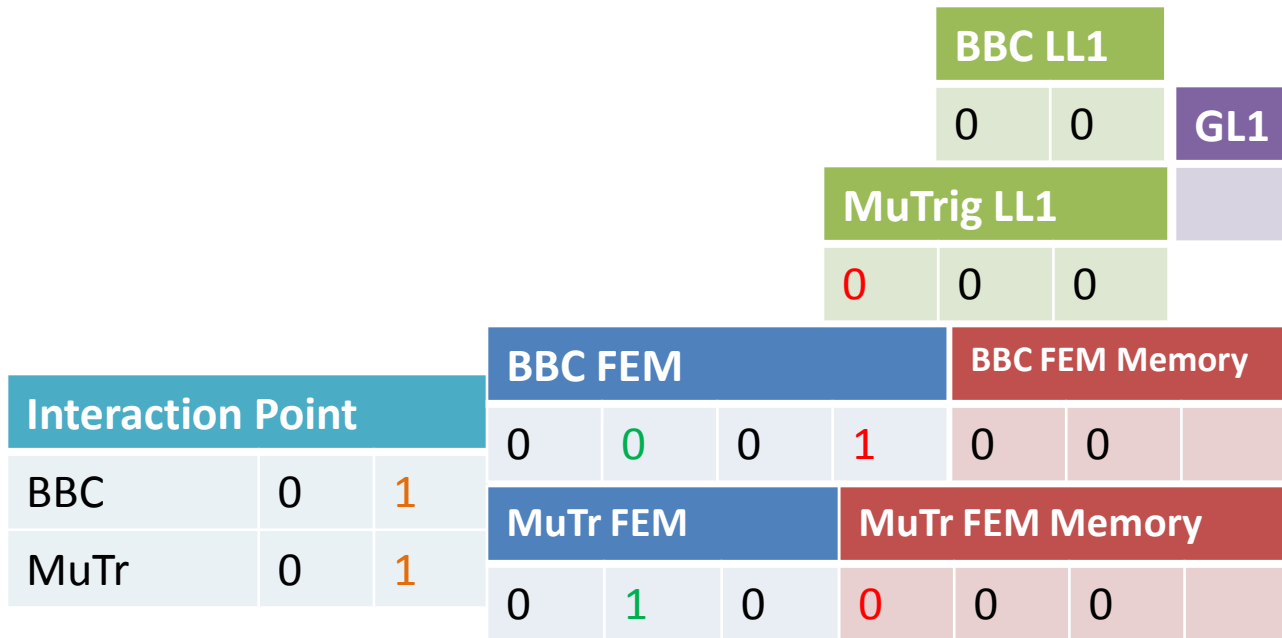
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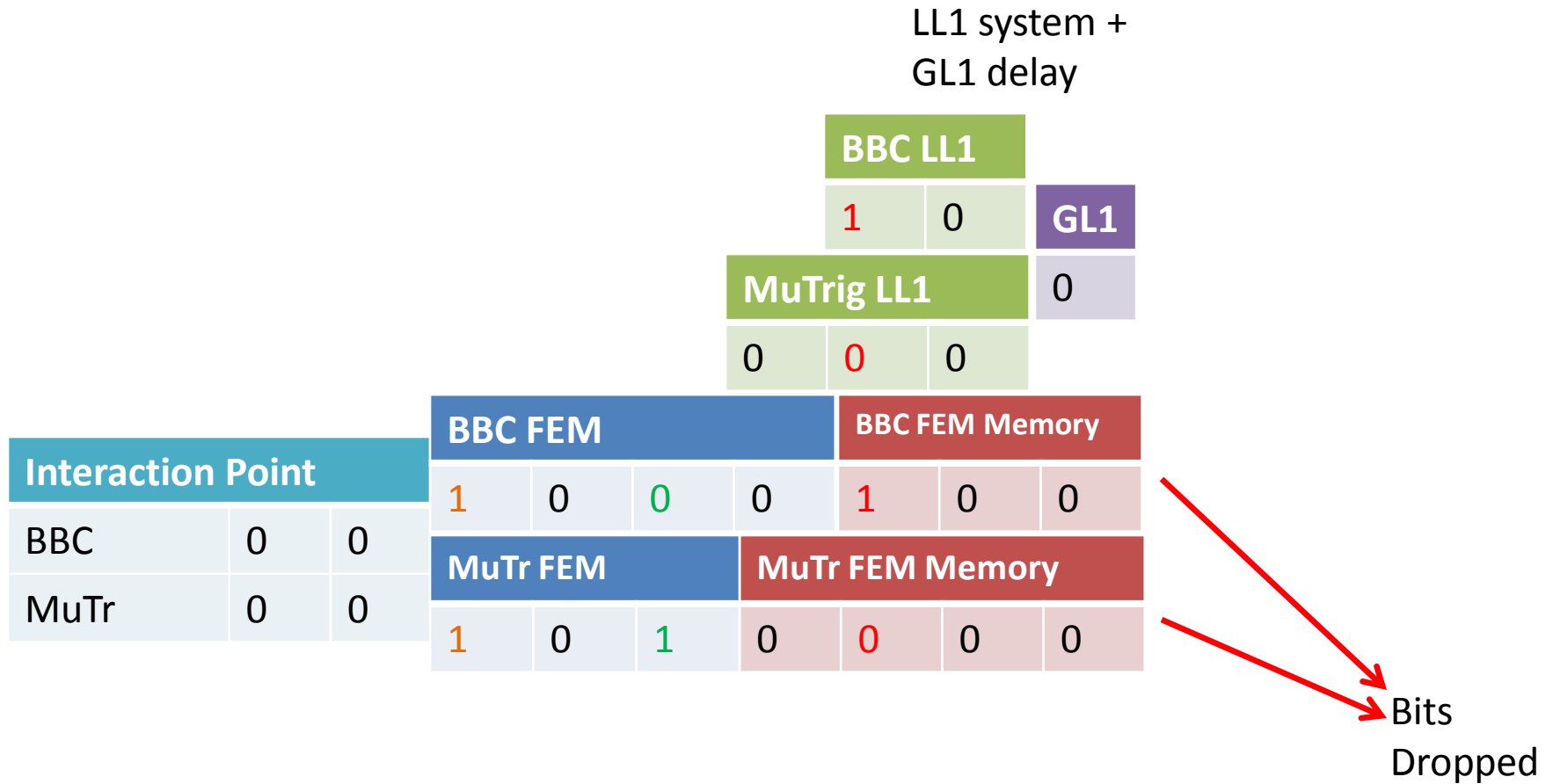
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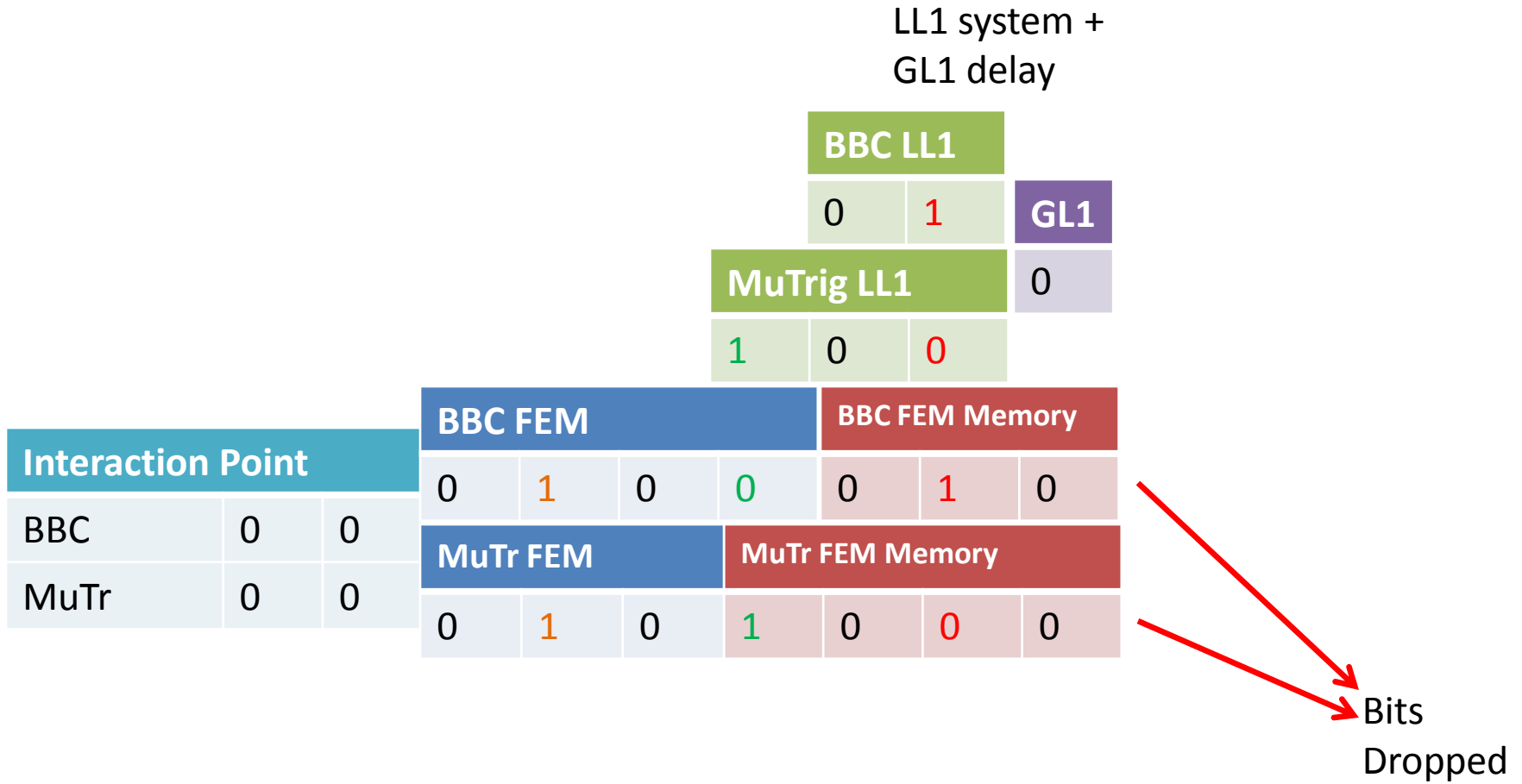




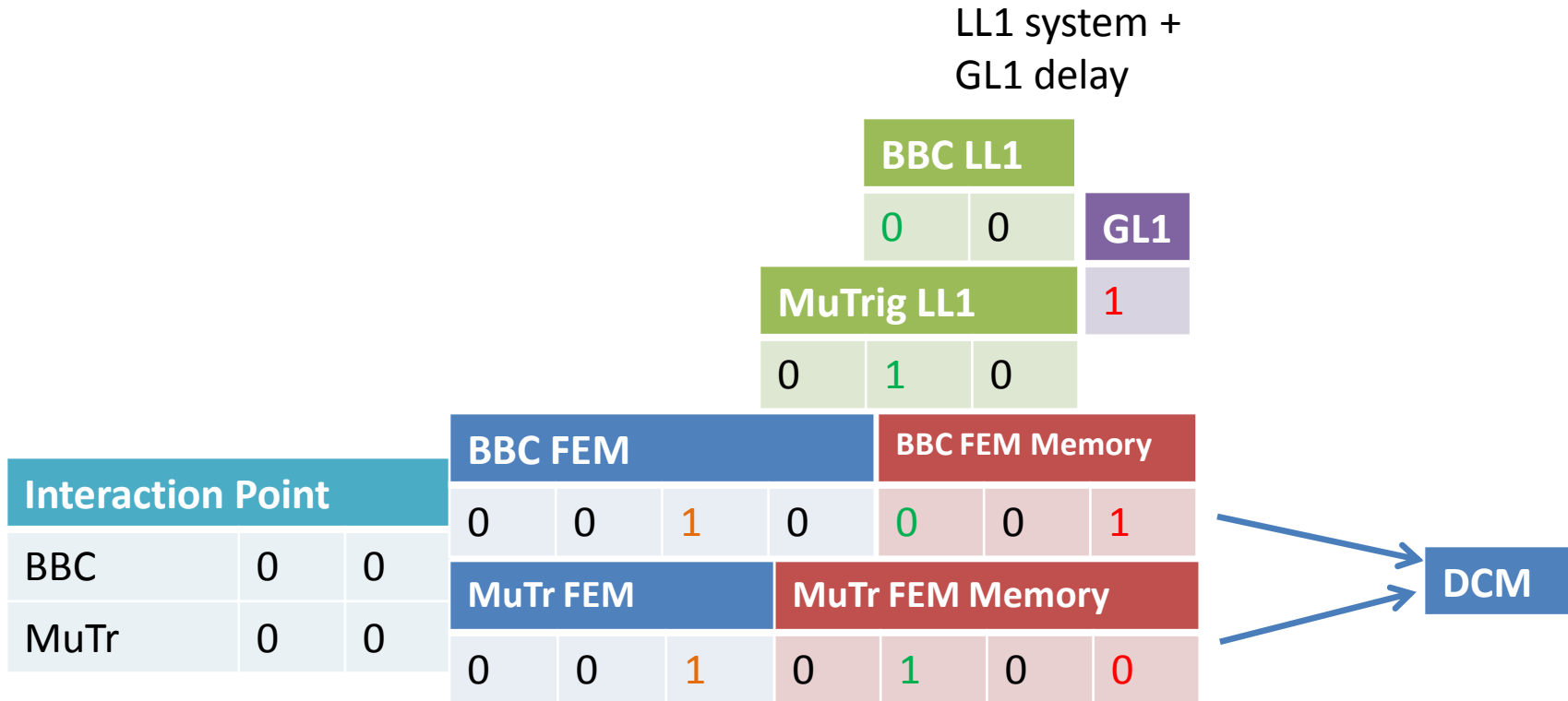
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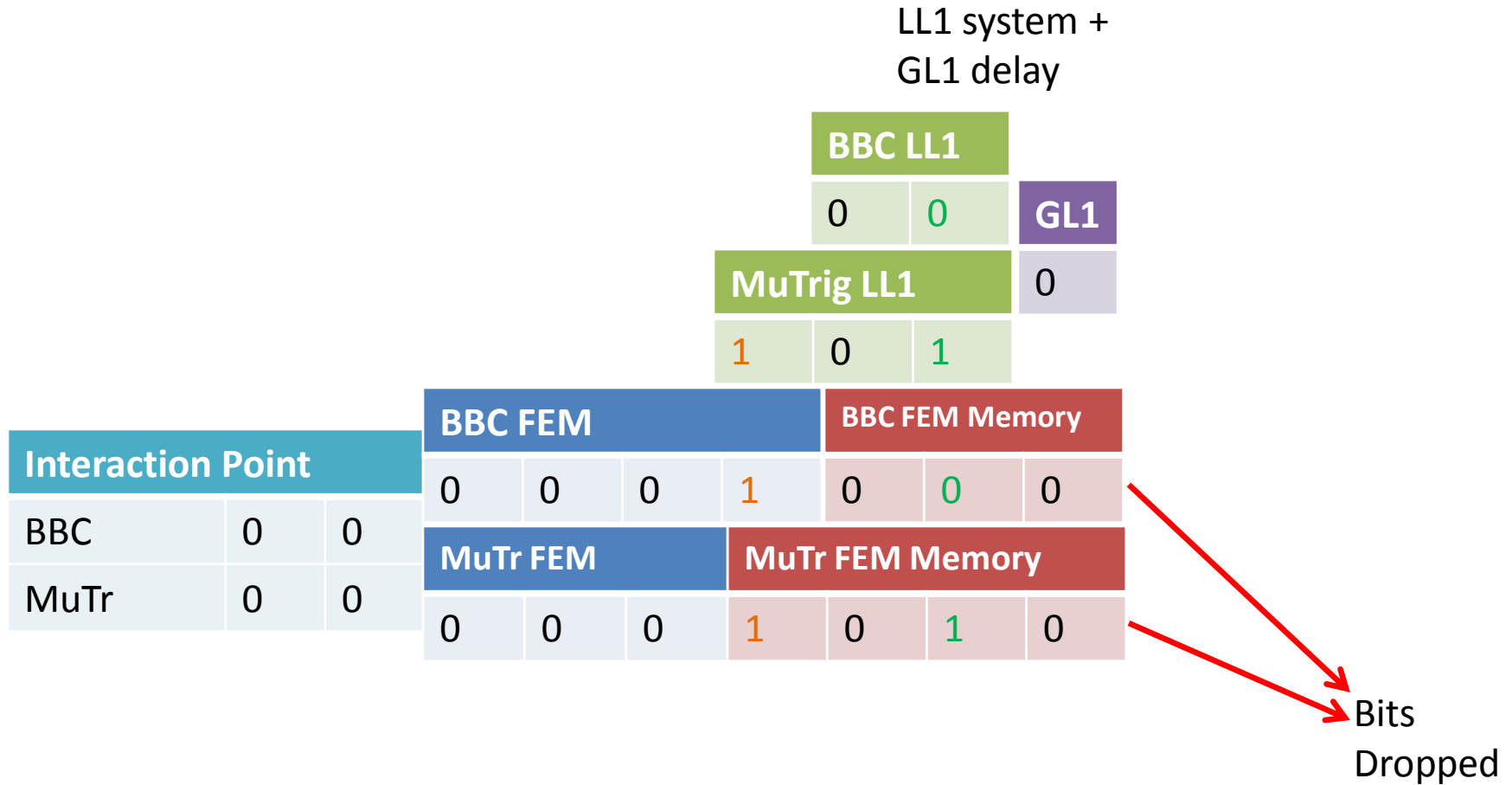
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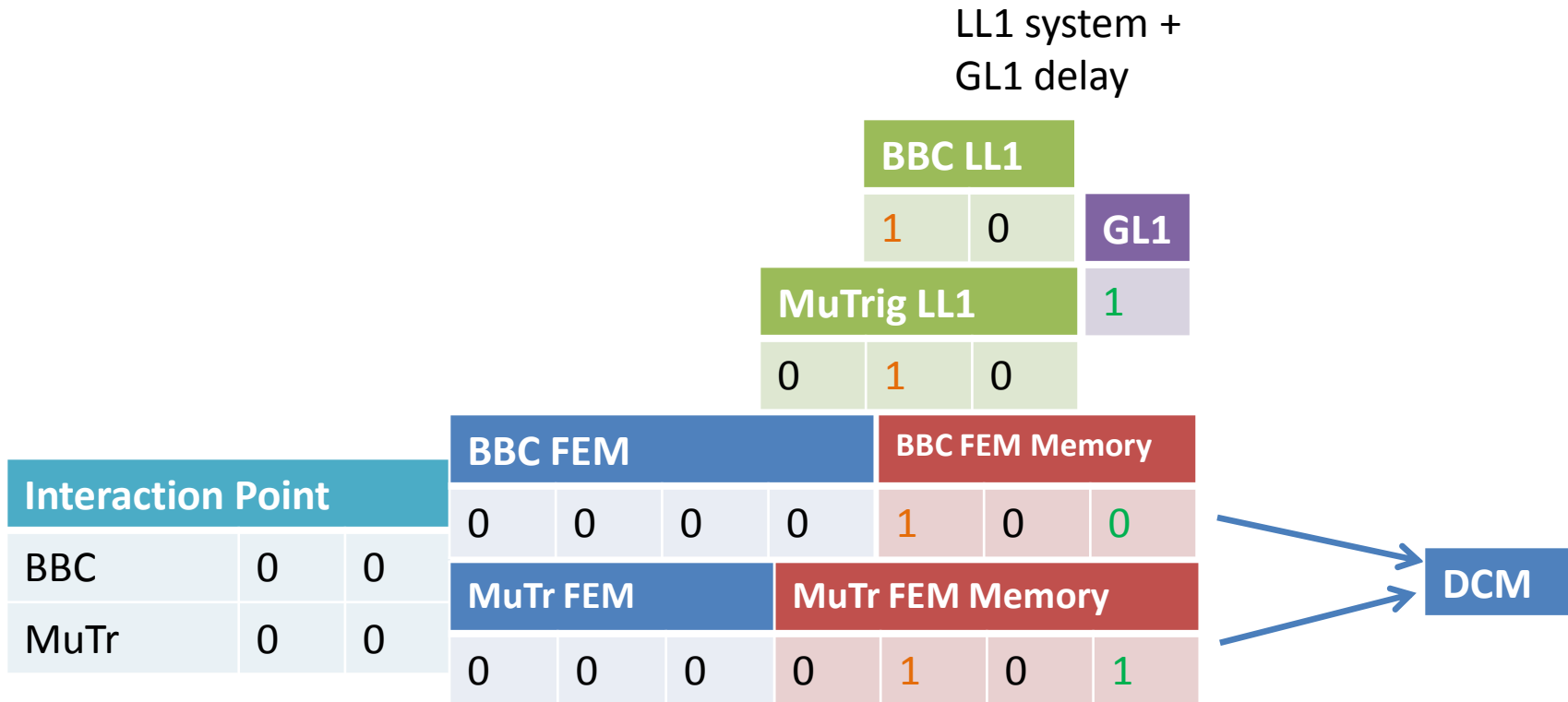
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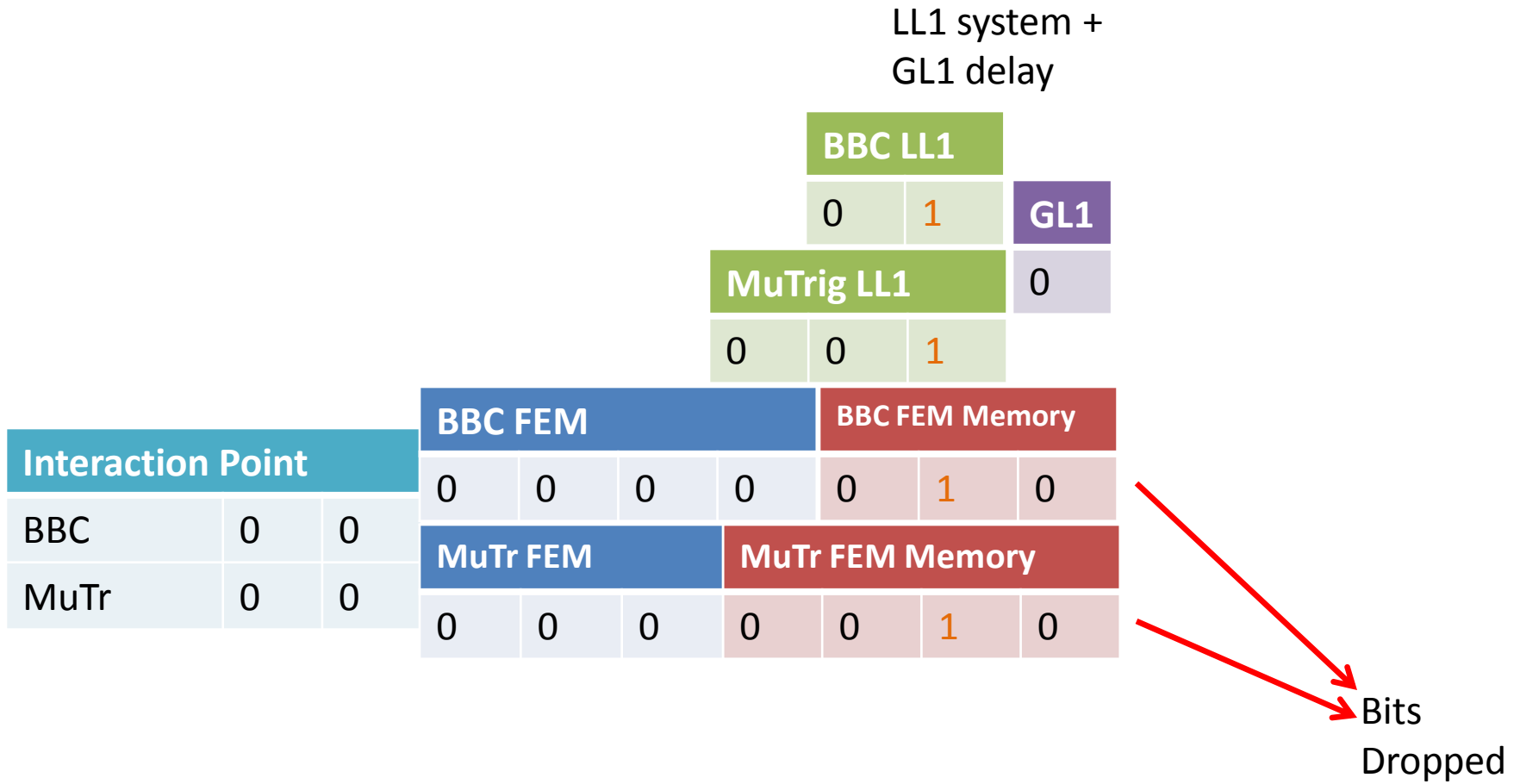
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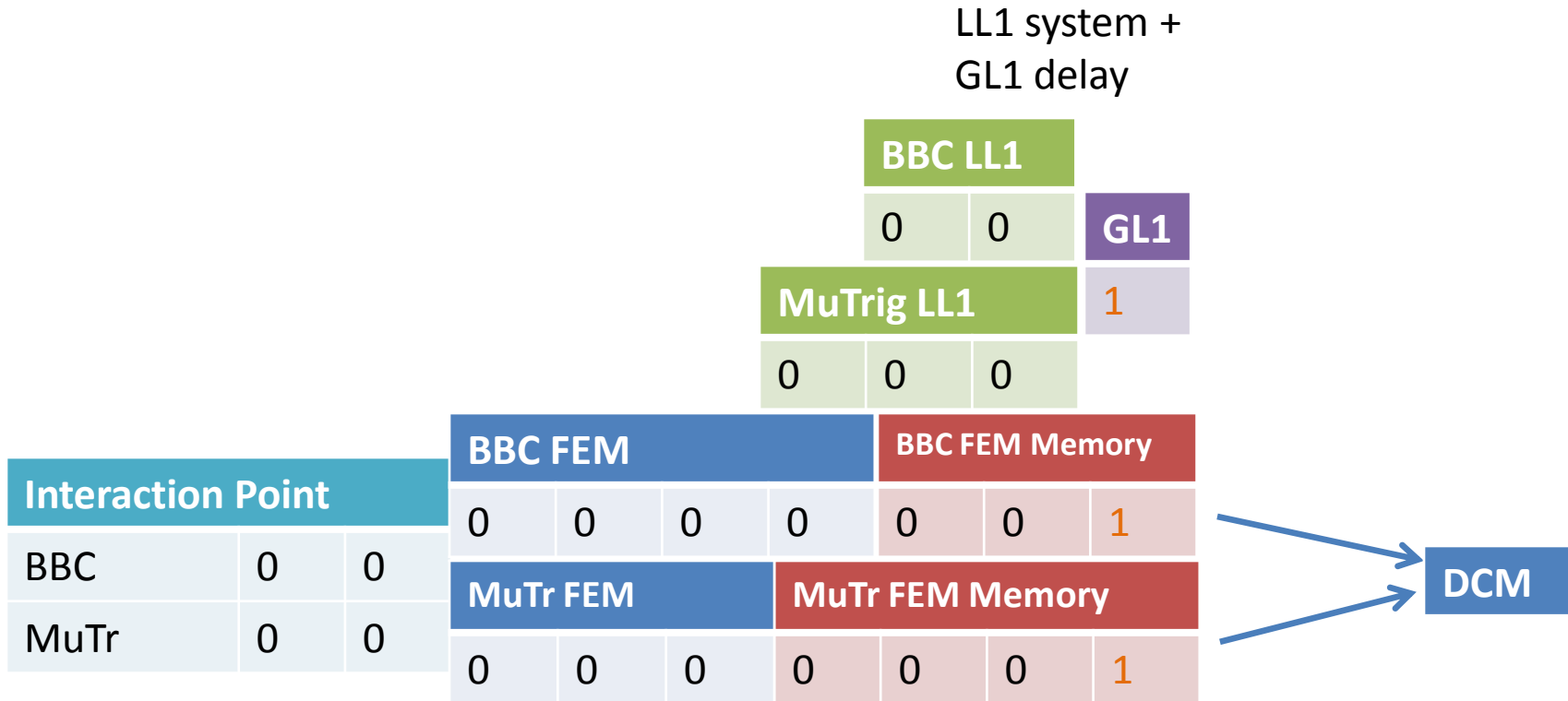
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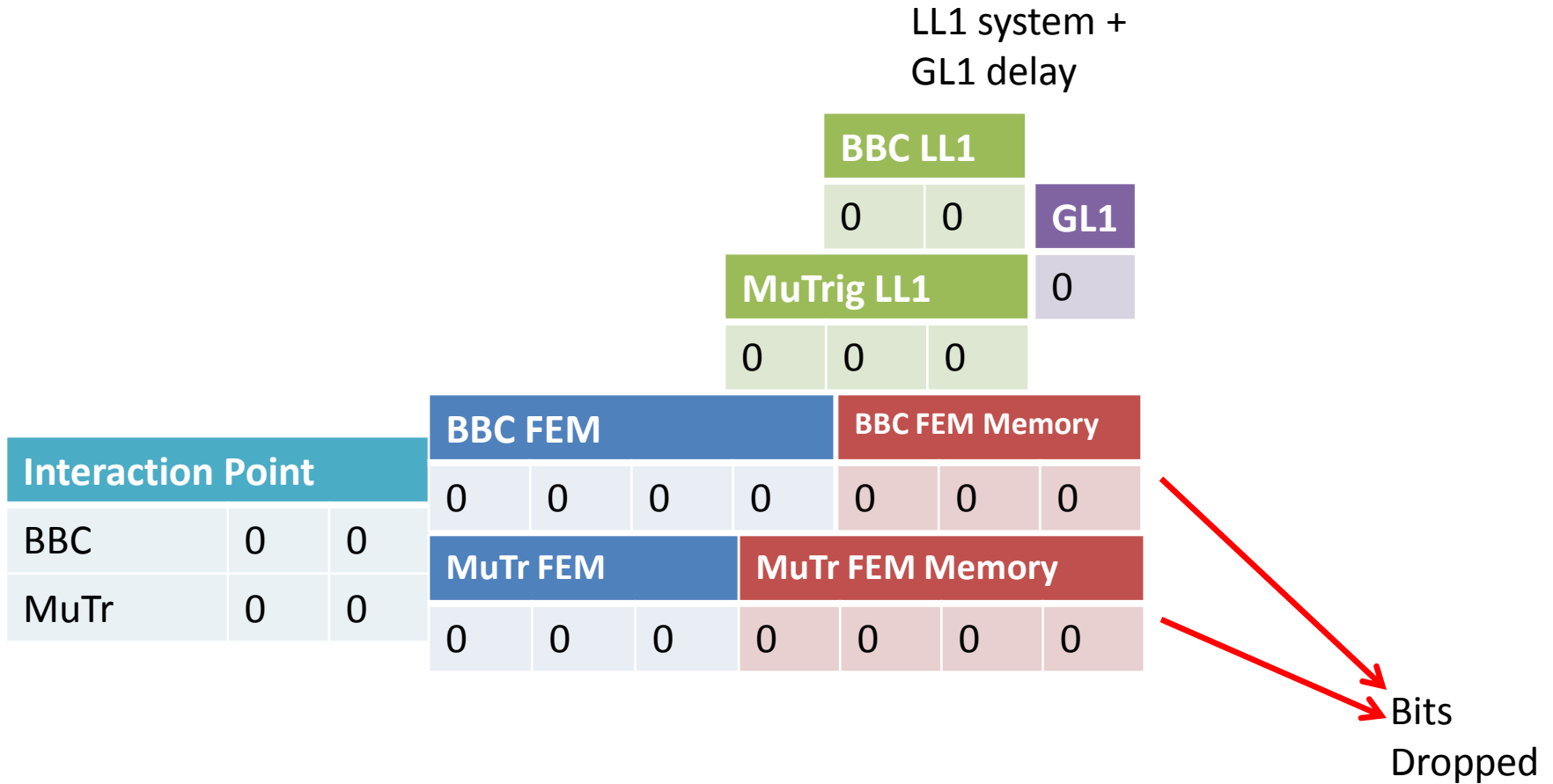
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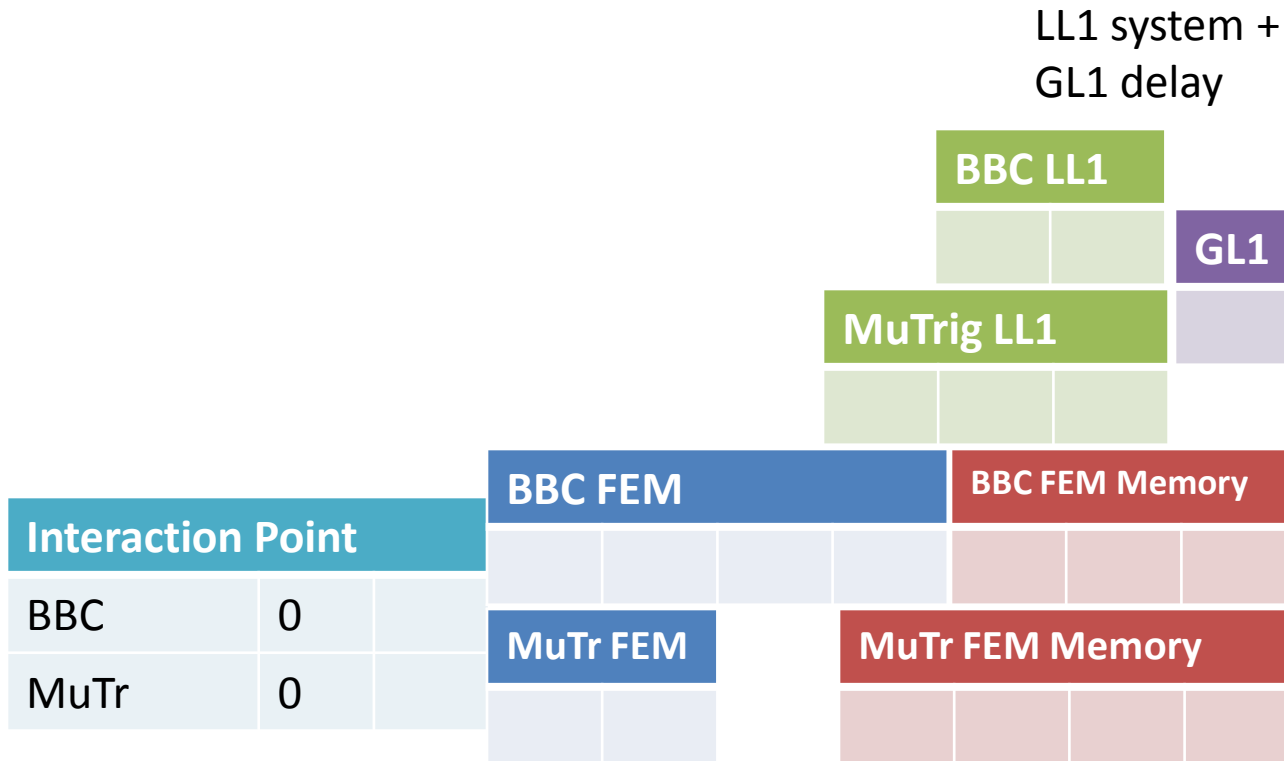


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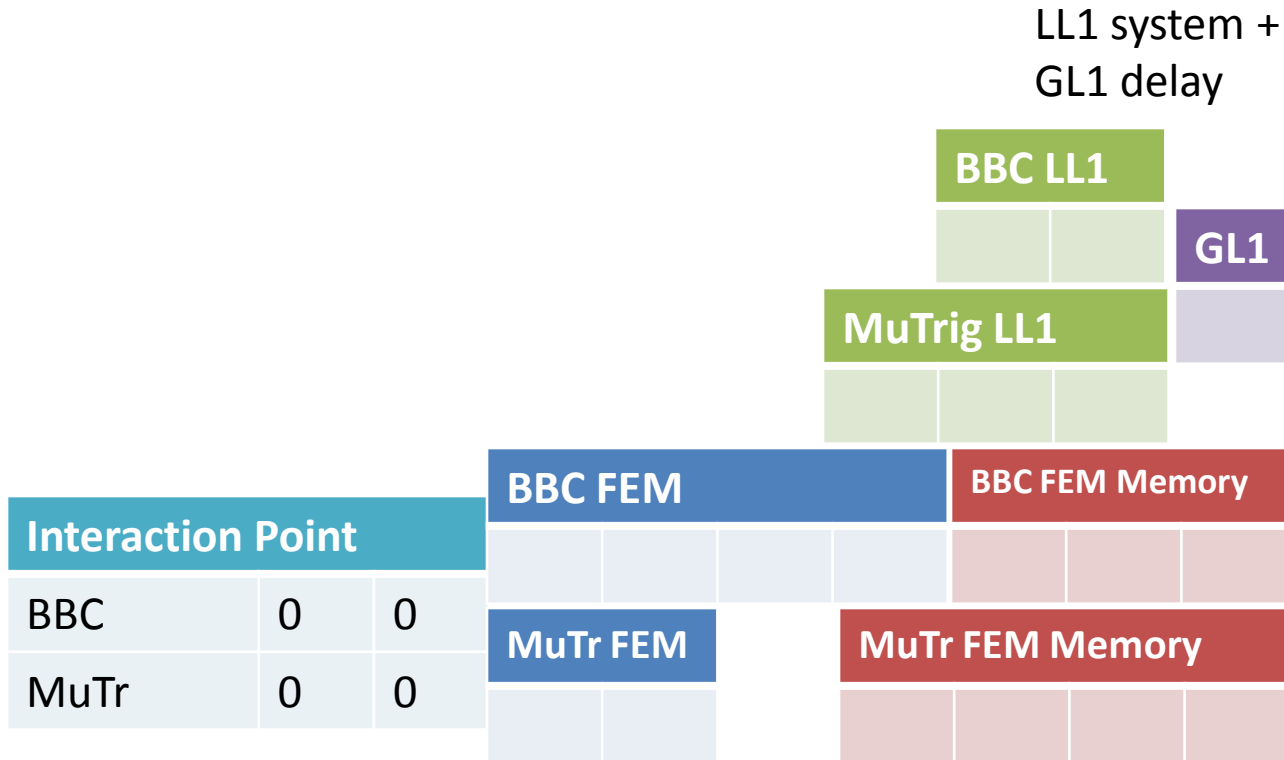


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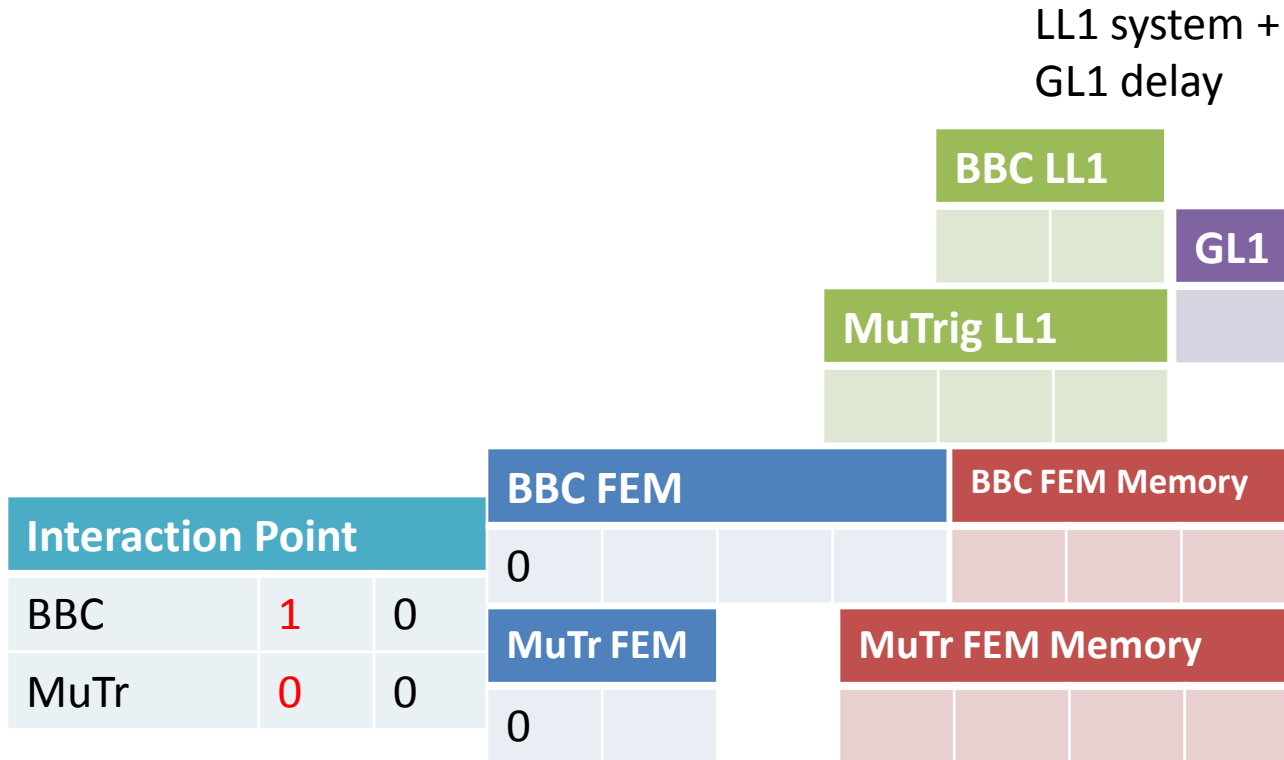


MuTr FEM is  
faster than we  
think it is!

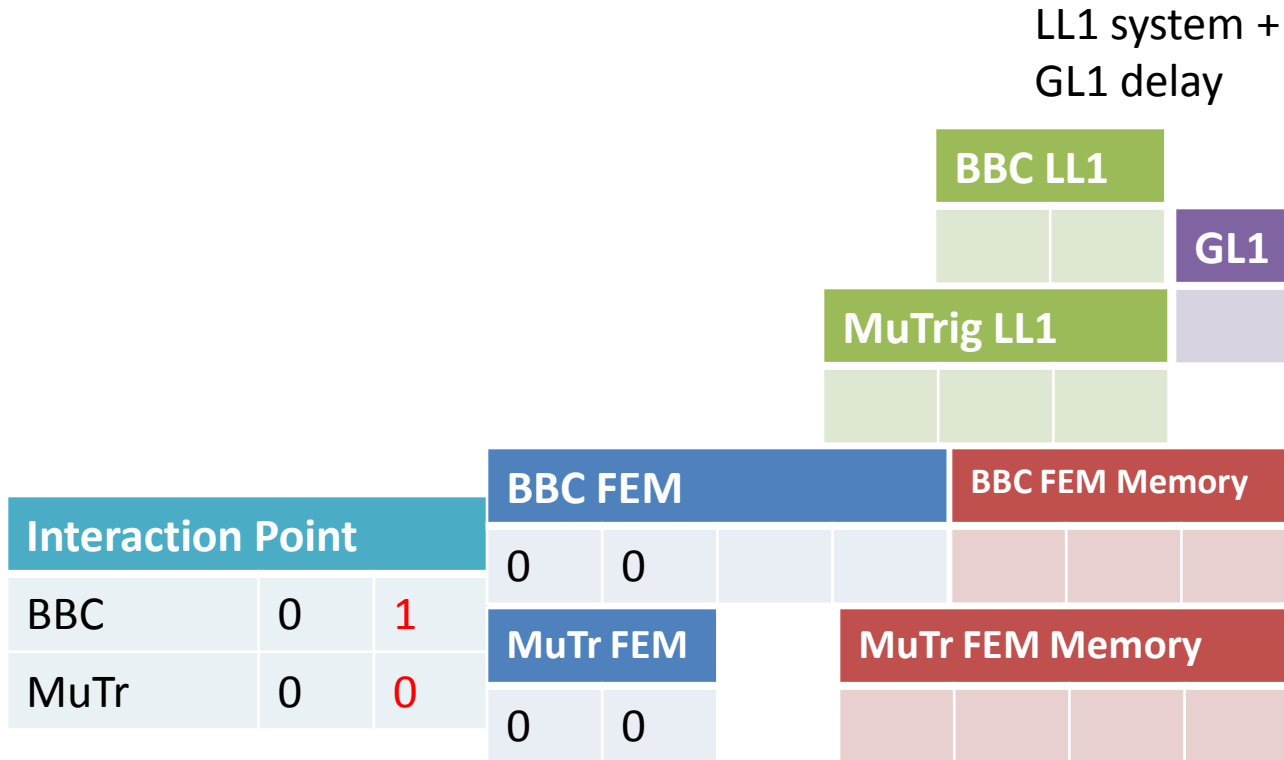
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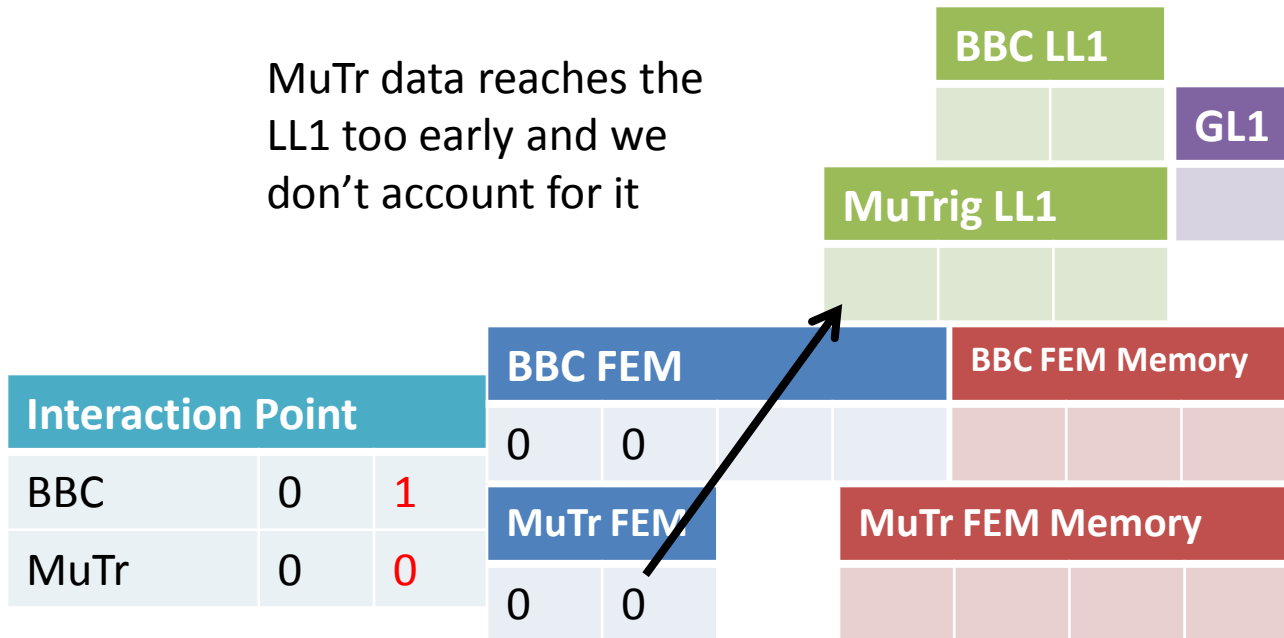
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MuTr data reaches the LL1 too early and we don't account for it

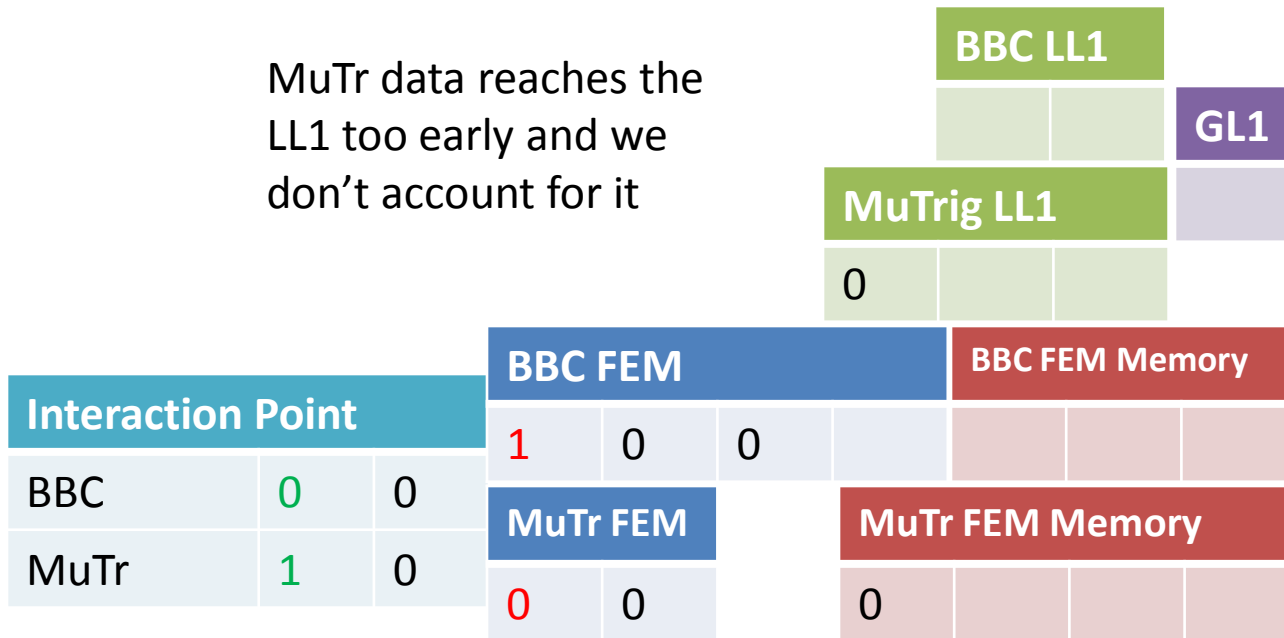
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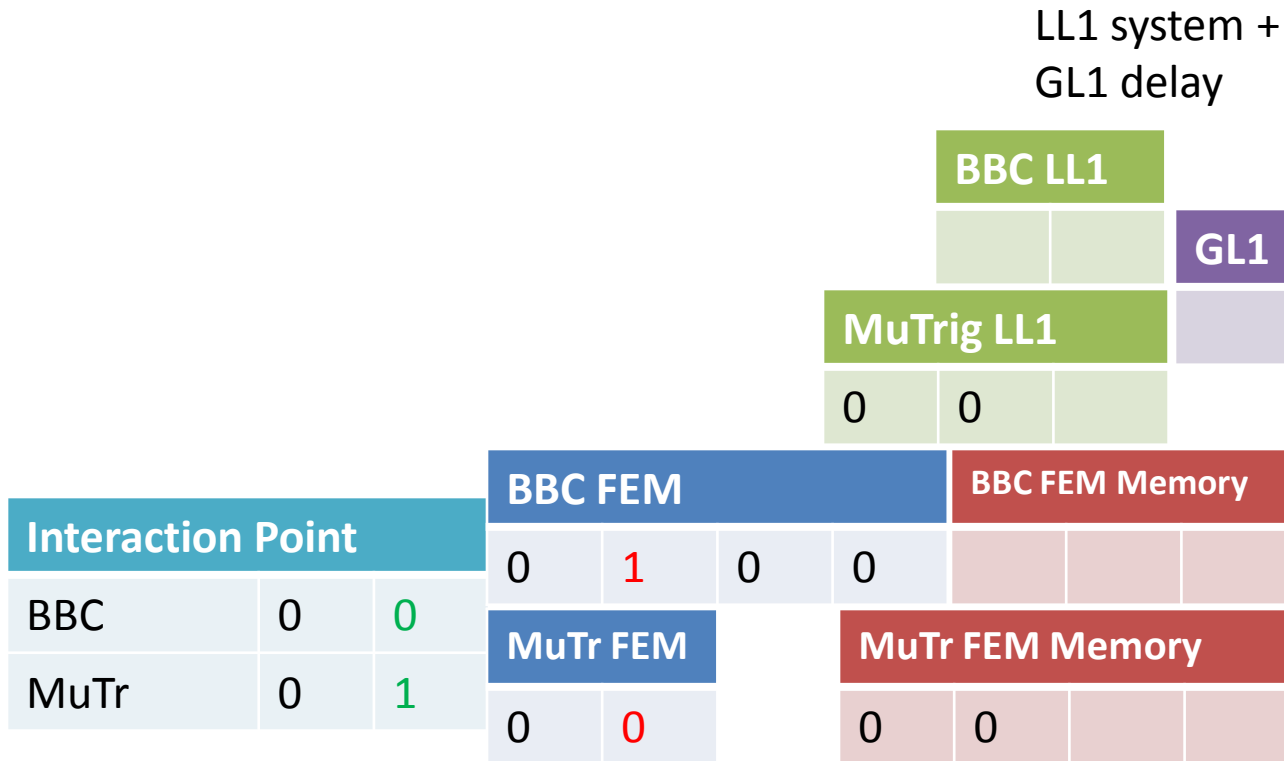
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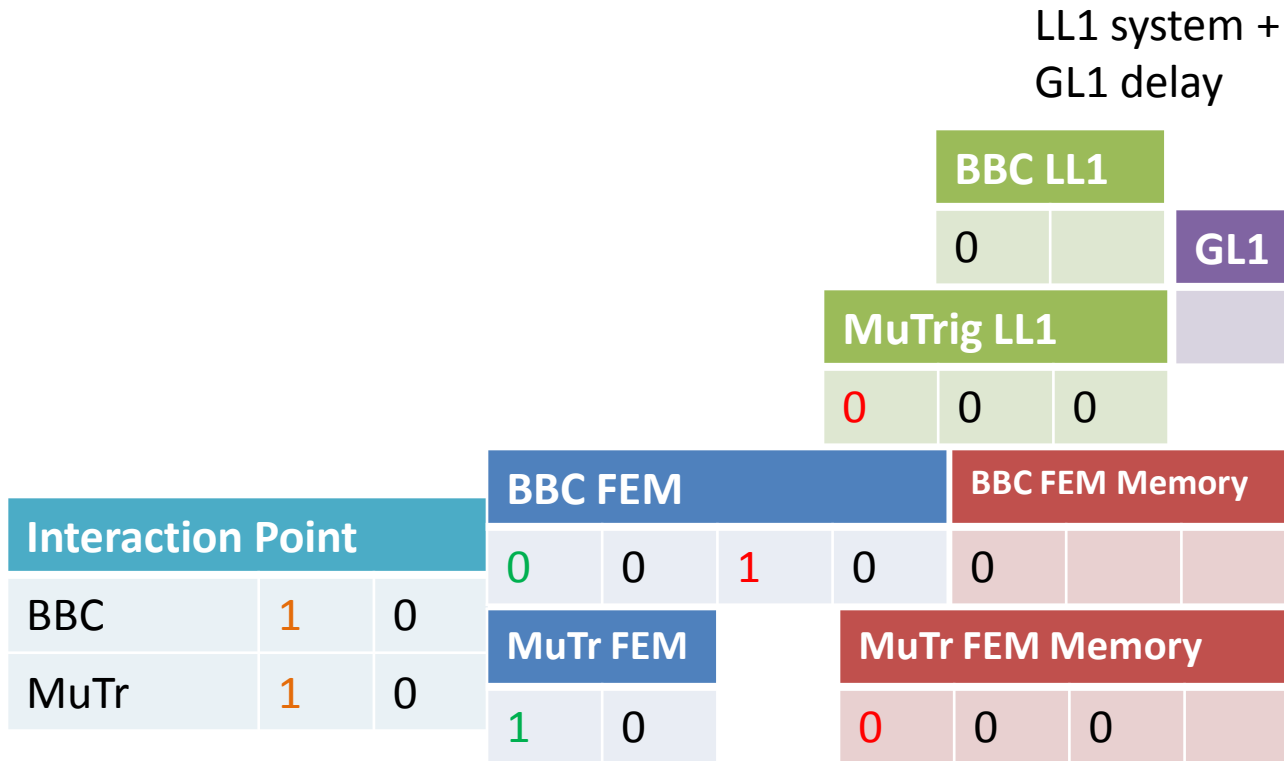
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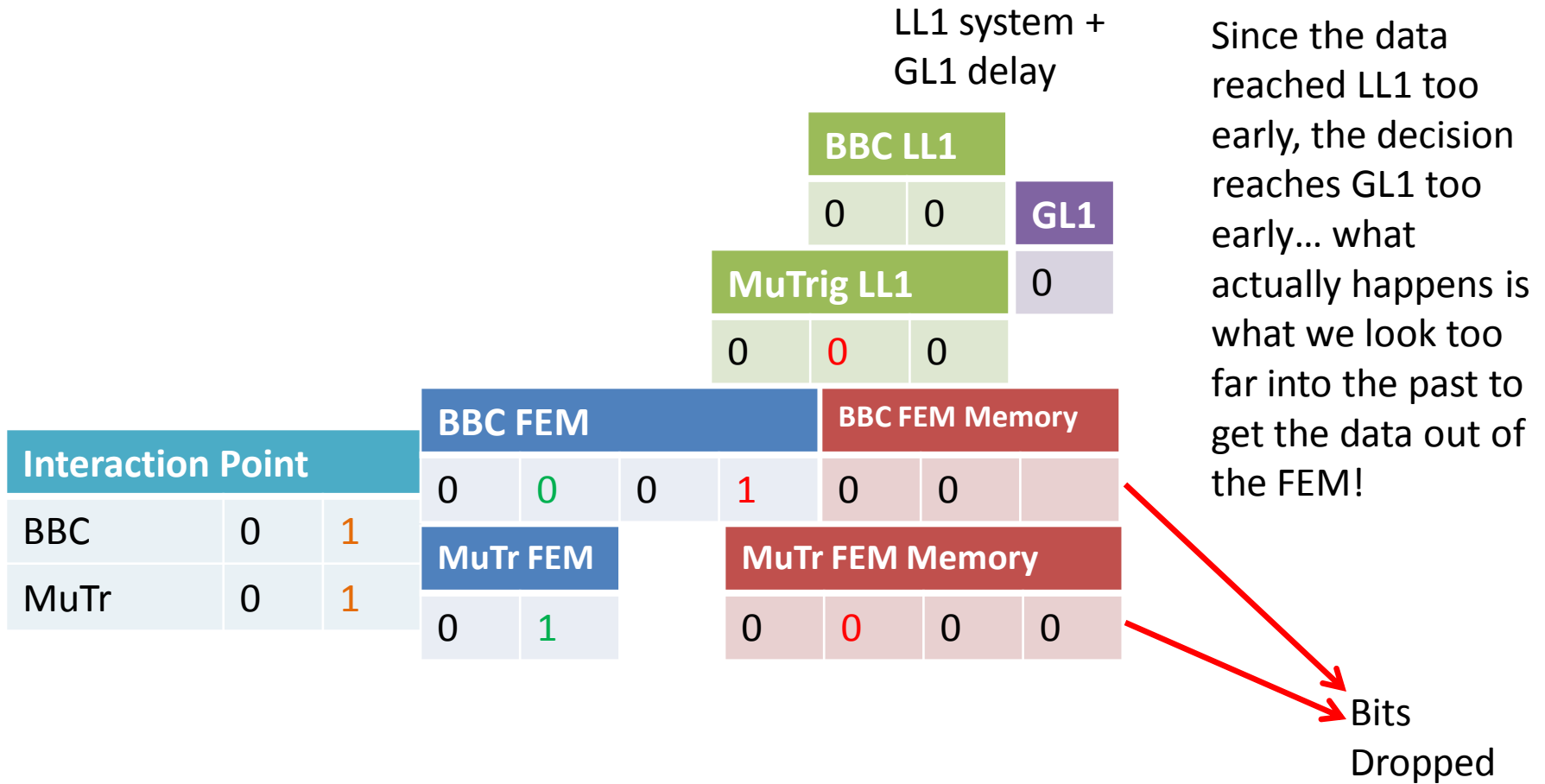


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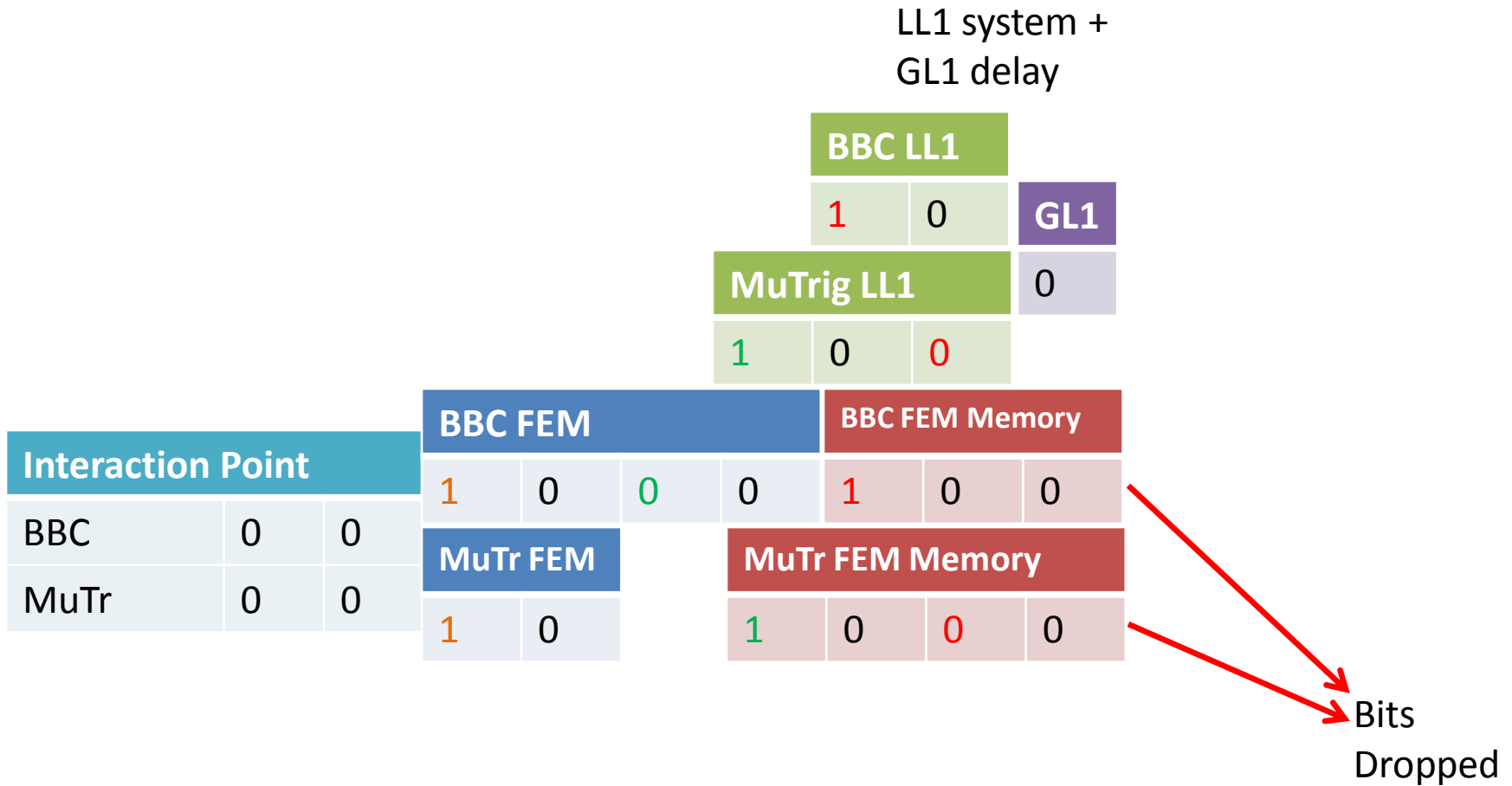




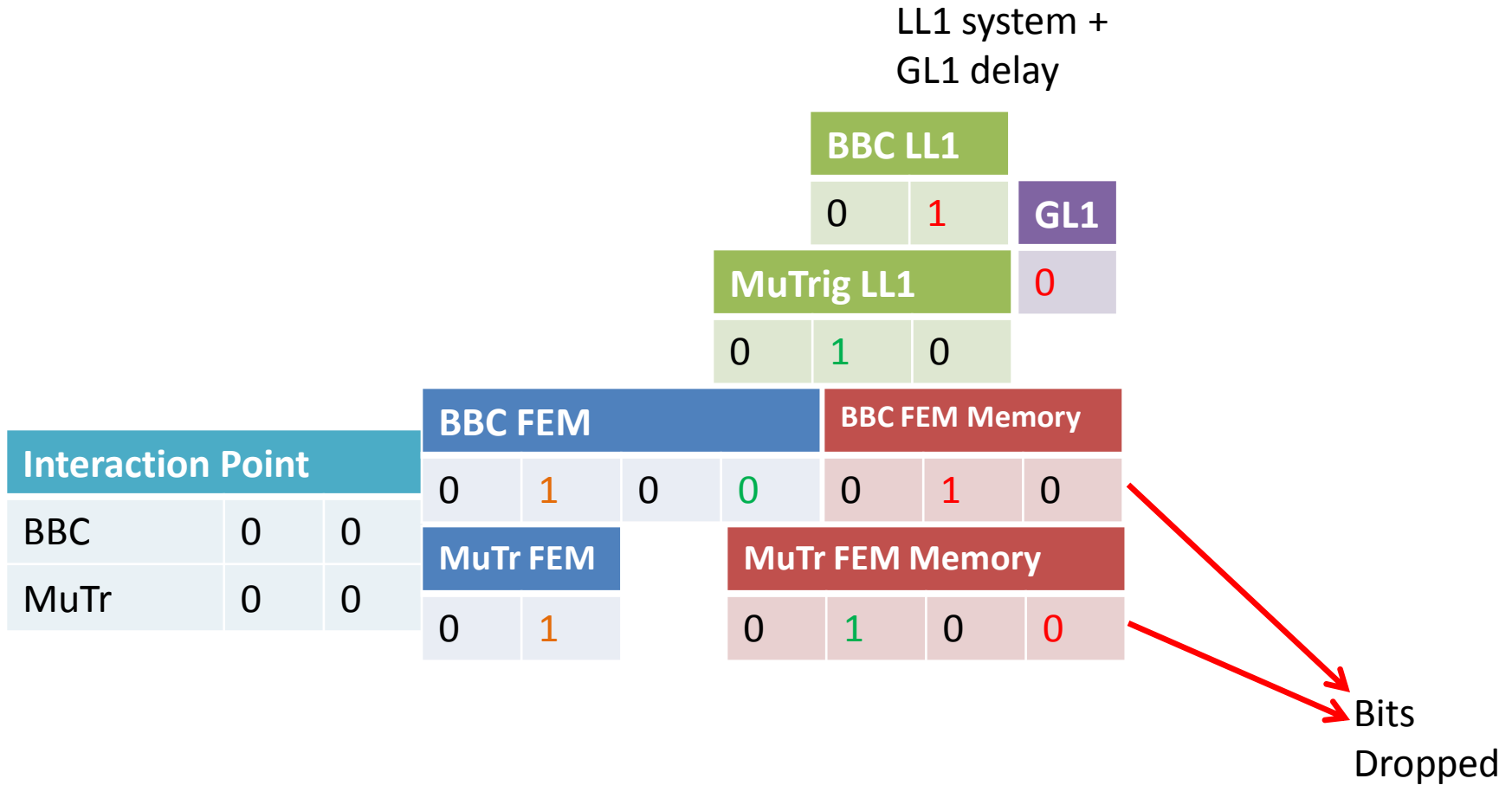
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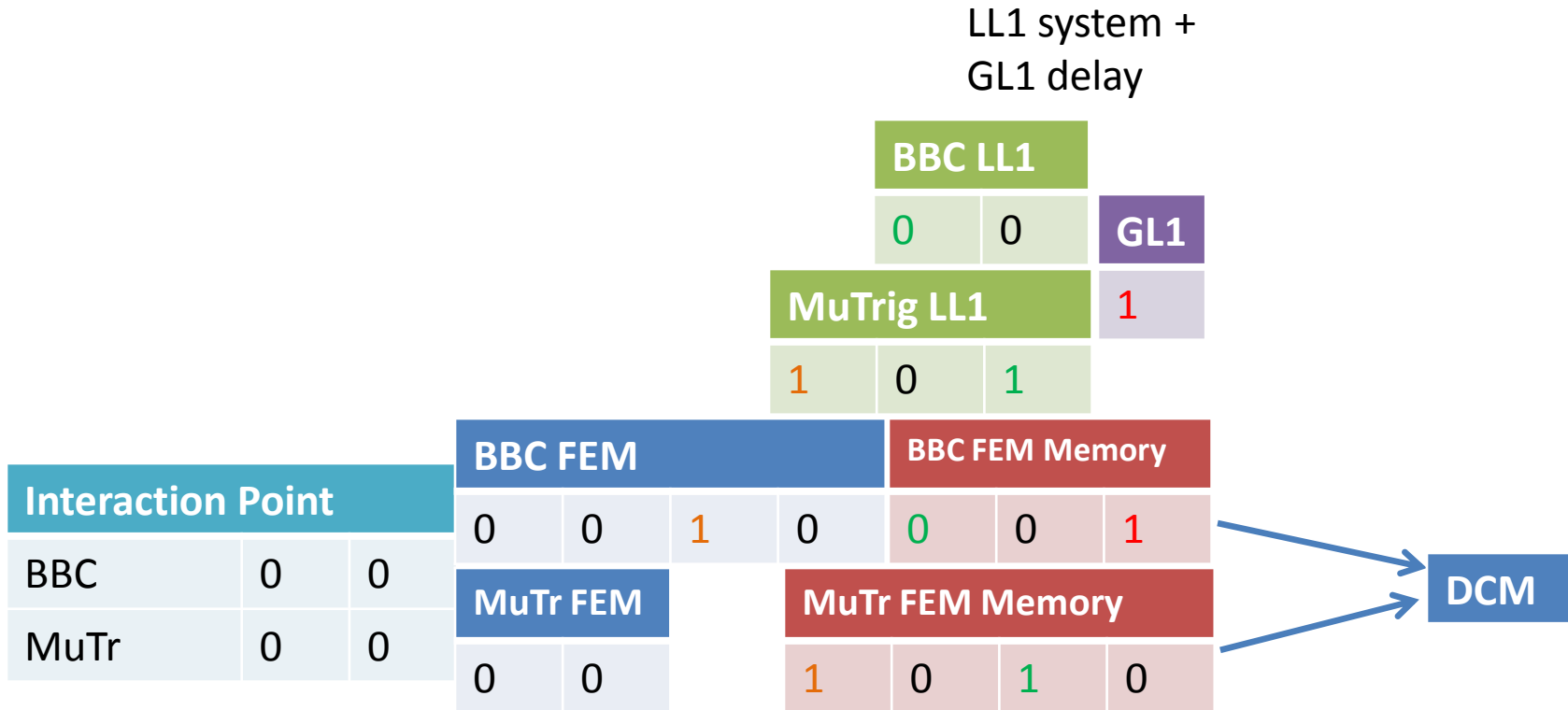
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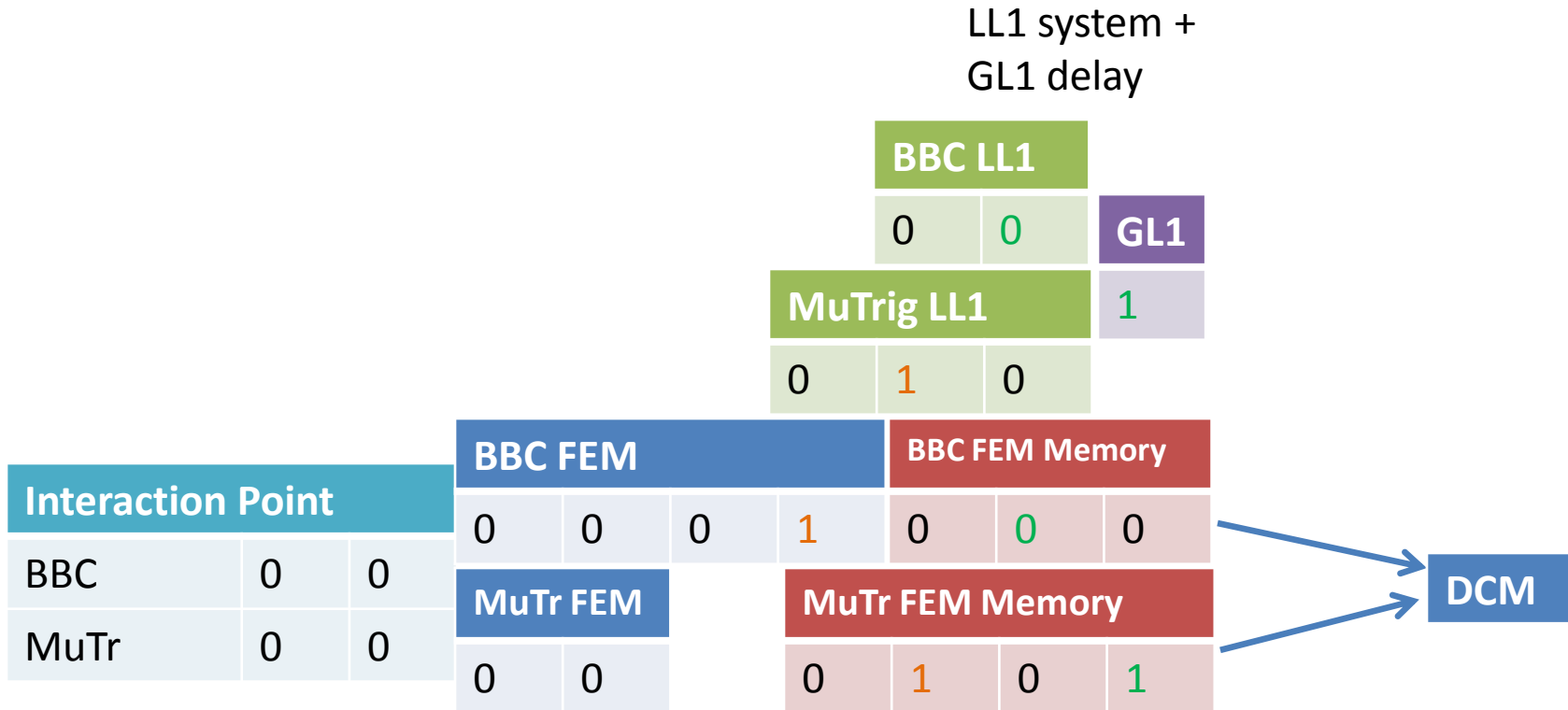
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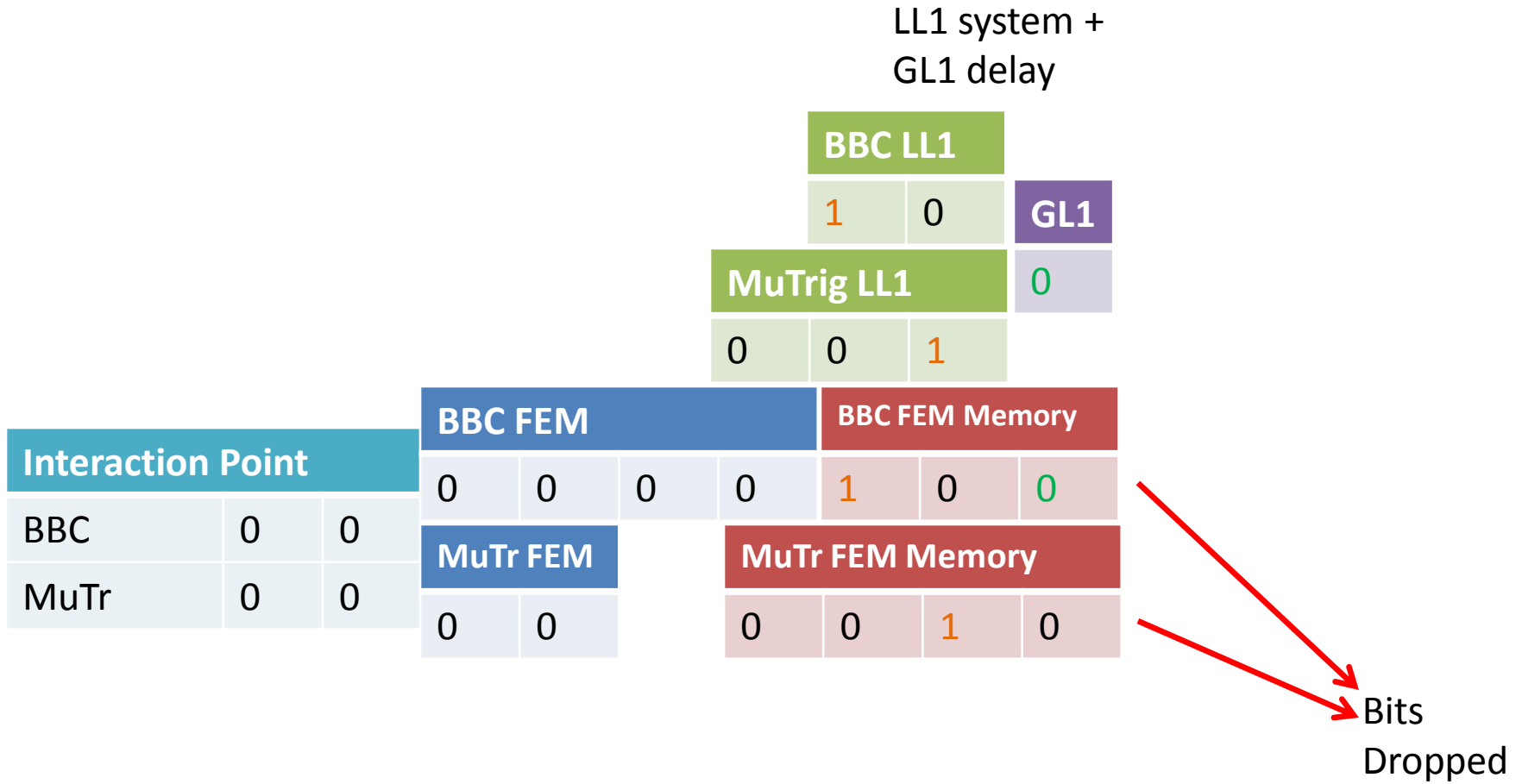
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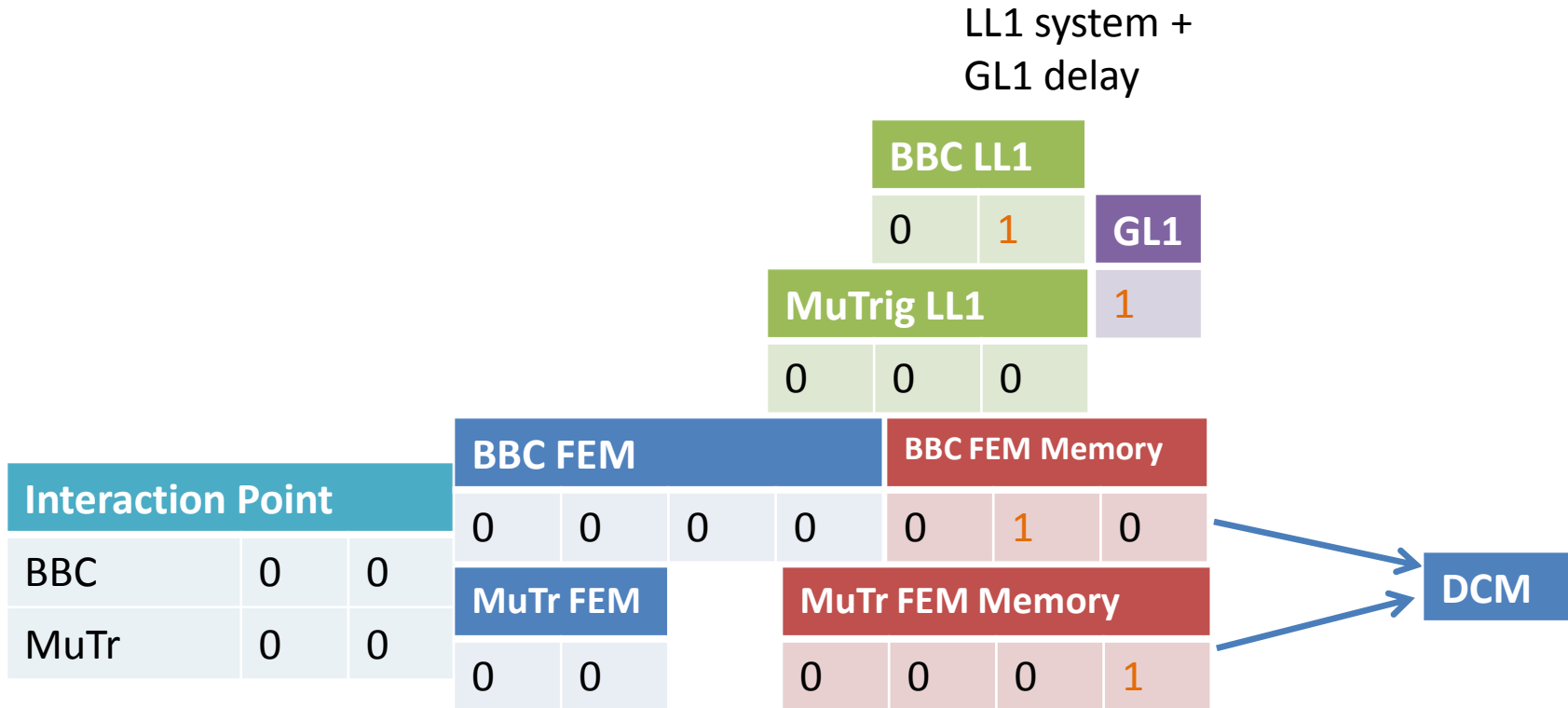
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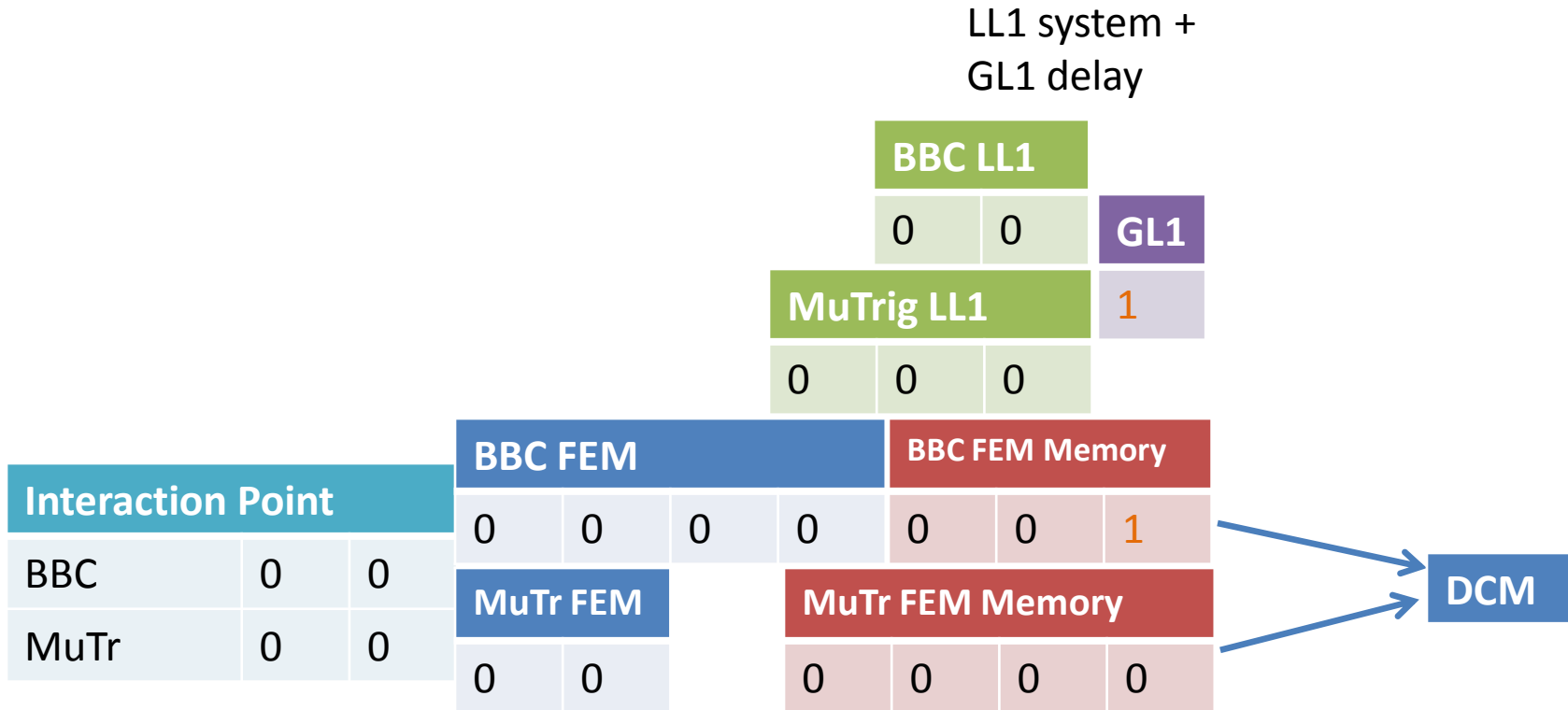
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