sPHENIX Electronics

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PHENIX Workshop

RIKEN

July 30, 2013

Electronics Concept

- Use what we have learned from PHENIX
- Maintain as much of the PHENIX DAQ as reasonable
  - DCM2, Event Builder
  - Slow control infrastructure
  - Monitoring and Data logging infrastructure
- Compact design for EMCal and HCal
  - Same basic design for both detectors.
  - Mount front-end electronics on the detector: Minimize connections.
  - Commercial components where possible existing custom ASICS if necessary .
  - Consider multiple approaches

Front End Analog Electronics

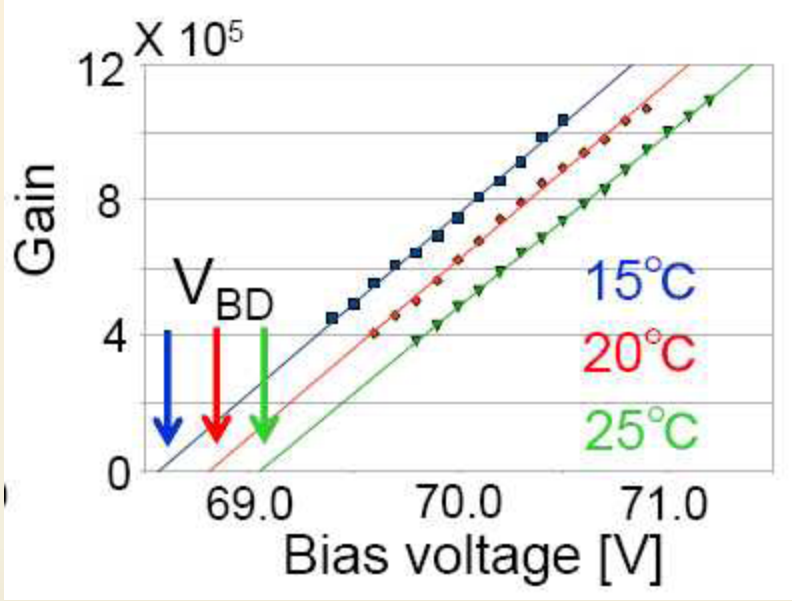
Sensors

- Silicon Photo-multipliers (SiPMs)
  - Compact device: Active area 3mm x 3mm.
  - Immune to magnetic fields:
  - Large gain: 3 x 10^5
  - Large dynamic range: 1 x 10^3
  - Inexpensive in large quantities: > $17/channel
  - Gain is temperature (10%/^{0}C)
  - Large number of new devices coming on the market every day
  - Primary choice
- Avalanche Photo-Diodes (APDs)
  - Compact device: Active area 5mm x 5mm
  - Lower gain: 50-100
  - Less temperature dependence (2%/^{0}C)

SiPM Voltage Dependence

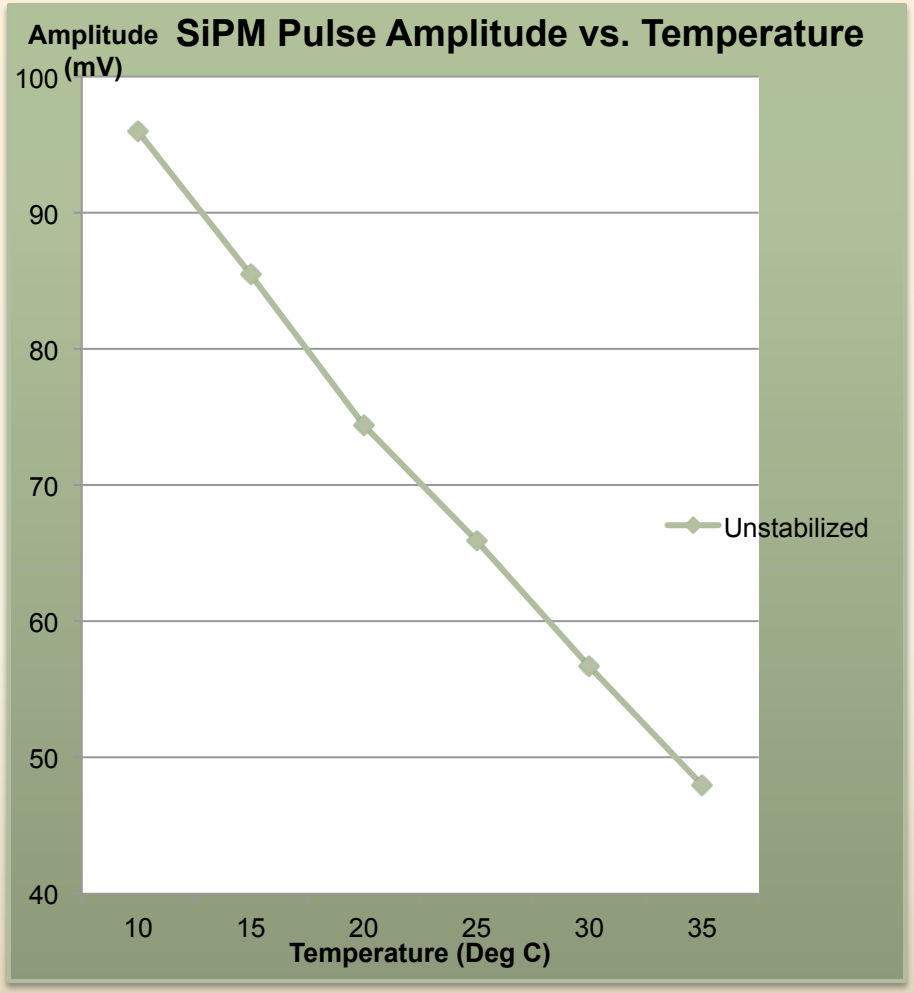
- Reverse breakdown voltage: V_{BD} ~ 70V
- Overvoltage range:

  V_{OV} ~ 2V
- V_{BD} increases linearly with temperature: 56mV/^{0}C
- Gain increase: x2/Volt



Minamino, Akihiro at al.
"T2K experiment: Neutrino Detectors

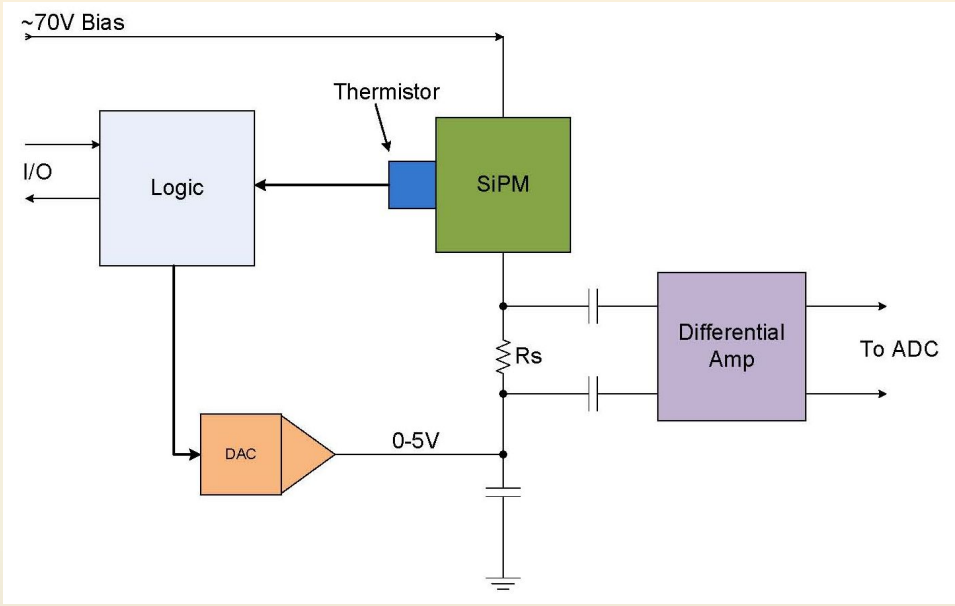
SiPM Temperature Dependence



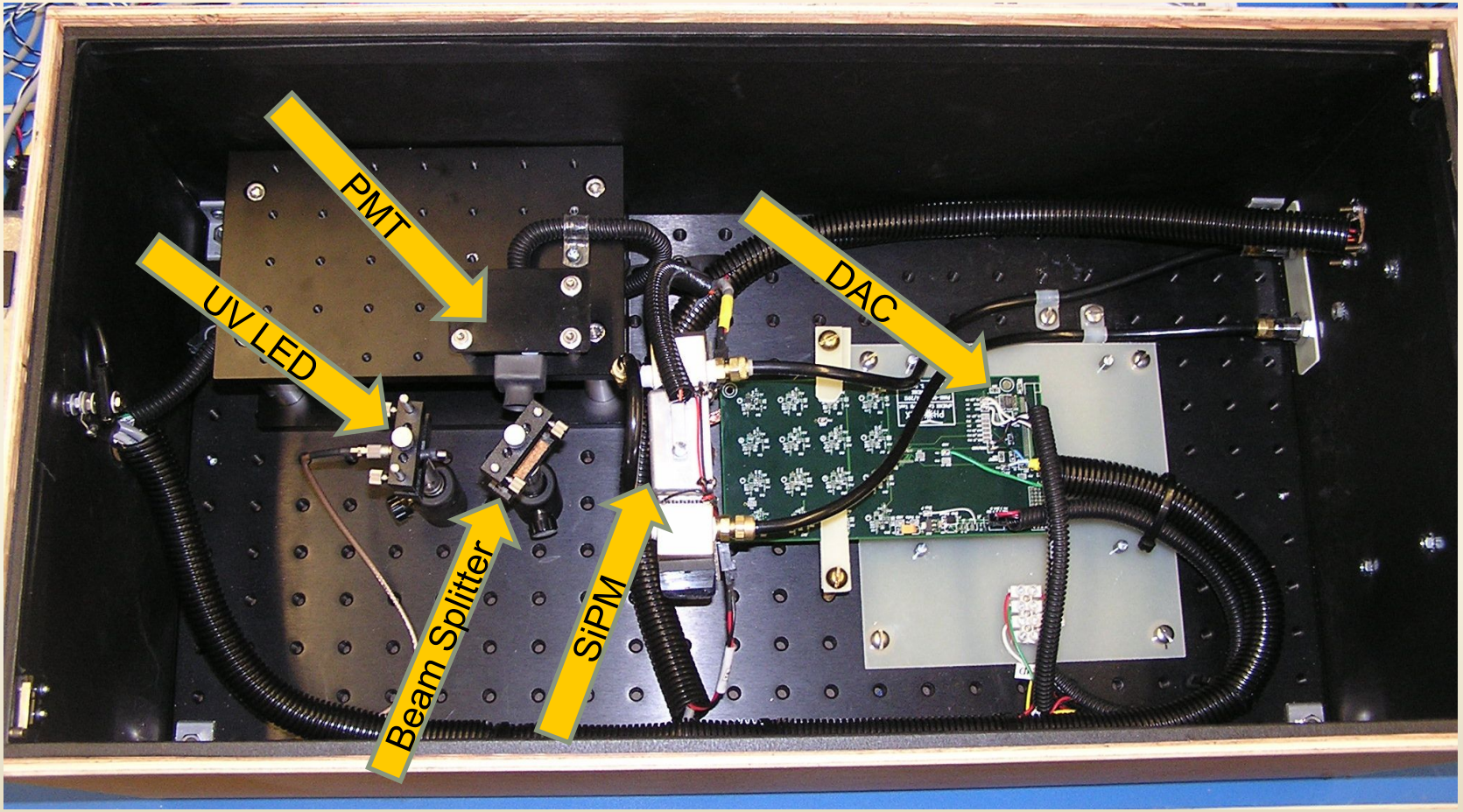
- SiPM Gain is highly temperature dependent. Measured pulse amplitude varies by a factor of 2 between 10^{o}C and 35^{o}C.
- Gain dependence is caused by a shift in the operating voltage (V_{op}) that is nearly linear in range of interest.
- A closed loop control system has been designed and tested to stabilize the gain. (Steve Boose/Sal Polizzo)

Prototype Temperature Compensation Circuit

- Temperature compensation using closed feedback loop
  - Thermistor
  - Logic control
  - 10 bit ADC
  - 12 bit DAC
- Logic unit computes DAC setting based on linear relationship between gain and temperature
- DAC reduces V_{BD} providing full range of gain control

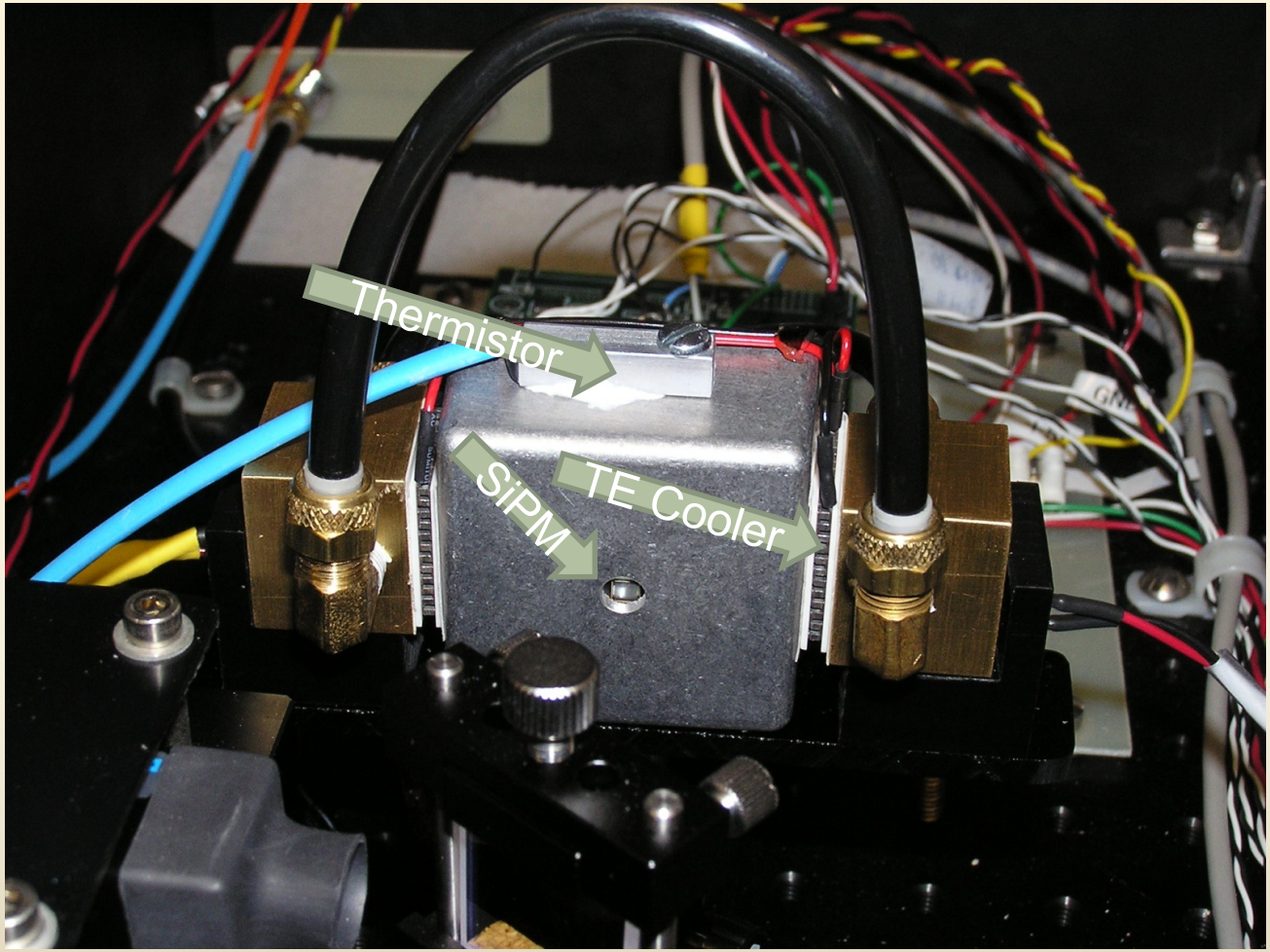


Evaluation Stand



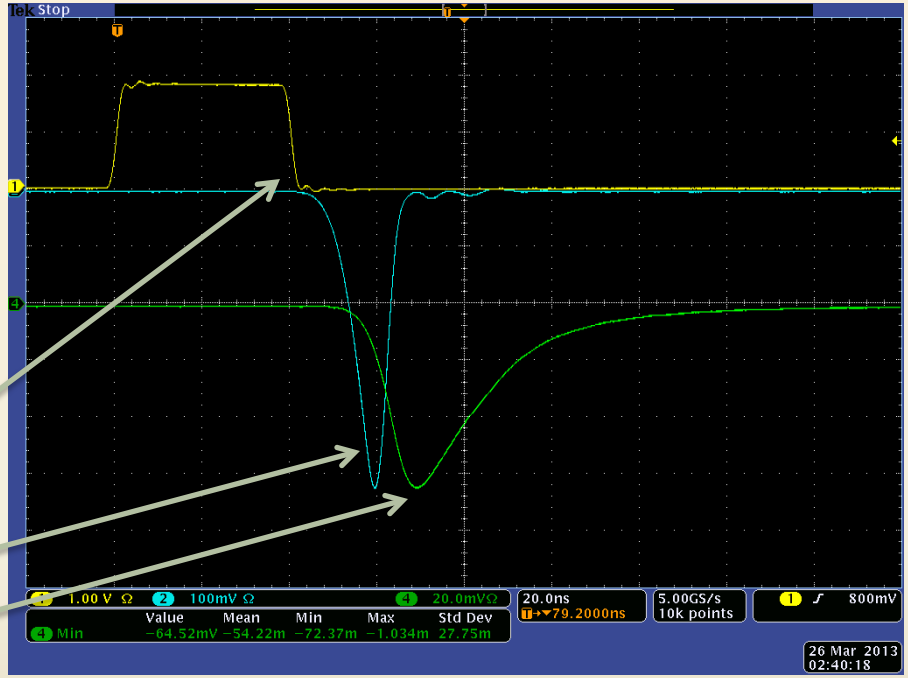
Temperature controlled SiPM Housing

- SiPM is contained in a temperature controlled housing
- Two 5W heaters inside housing
- Two TE coolers mounted with thermistors for monitoring
- External temperature controller
- Water cooled blocks to remove heat from TE coolers

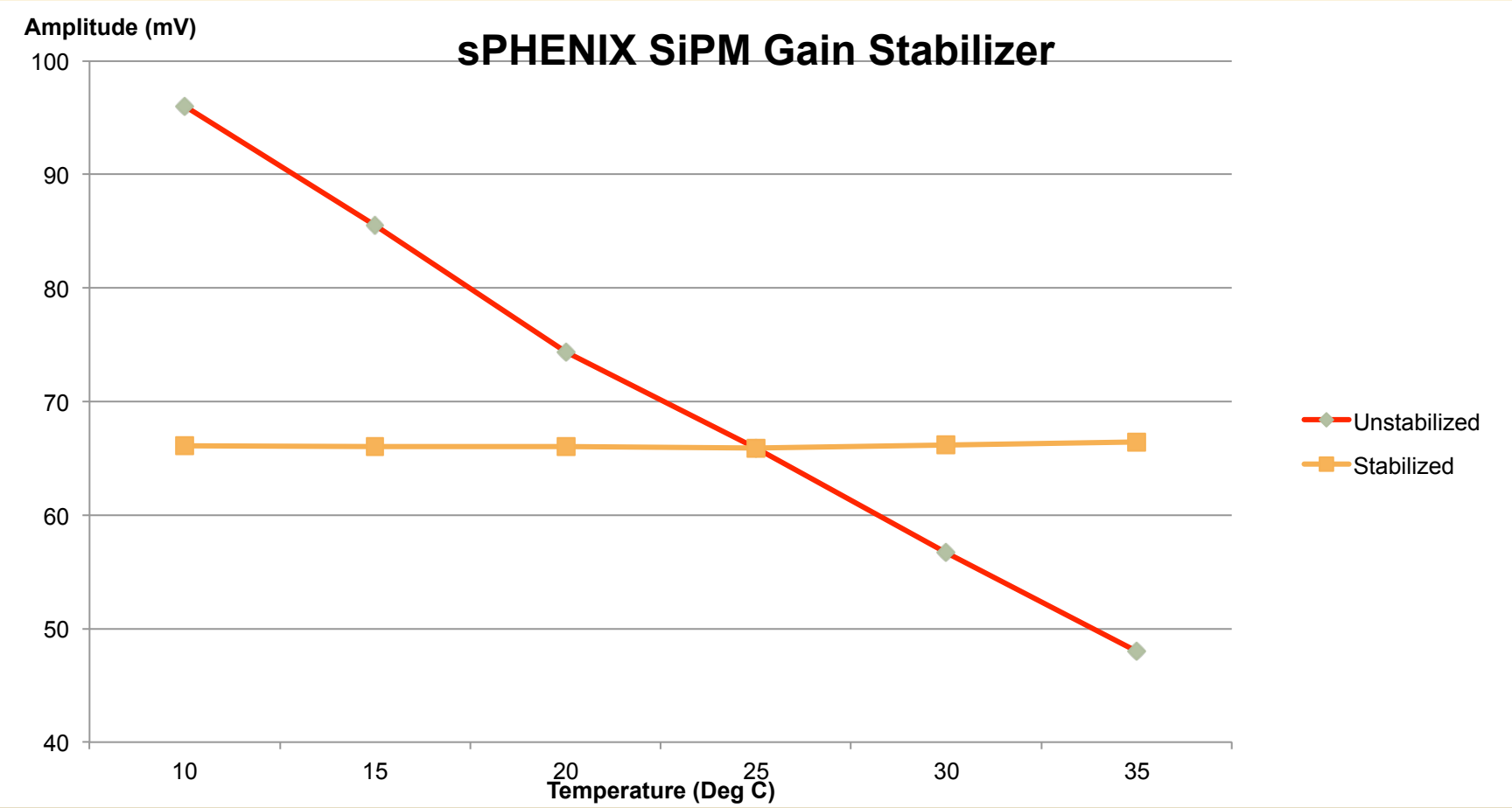


Temperature Compensation Measurements

- Measure the SiPM pulse amplitude as a function of temperature.
- PMT is used to monitor the LED output.
- Use closed-feedback circuit to adjust SiPM bias voltage as a function of temperature: 10.7 counts/^{0}C for DAC bias control.
  - LED Pulse signal
  - PMT output
  - SiPM output



Temperature Correction Results



ORNL Buffer Chip

- ORNL Group is working on new buffer/preamp chip
  - High bandwidth
  - Radiation hard
  - Differential drive (LVDS output)
  - Low power
  - Designed for ALICE FOCAL, but applicable to sPHENIX
- Prototype chip has been fabricated (April 2013)
- Testing in progress at ORNL/BNL
- Optimizing a design for sPHENIX that may be available for T-1044 Test Beam Run in Feb. 2014

Readout Electronics

Conceptual Design for EMCal/Hcal Electronics

- 2 Approaches being considered:
  - All Digital Mode DAQ
    - Continuous digitization of analog signals (60MHz).
    - Digital pipeline delay for LVL-1 accept.
    - Detailed discussion by C-Y Chi (next talk).
  - Mixed Mode DAQ
    - Beetle Chip front end with SRS based readout
    - Design work by ORNL/CNS-Tokyo for proposed ALICE FoCal Upgrade
- Both systems:
  - Mount SiPMs and compensation circuitry directly on detector.
  - Mount analog/digital electronics “nearby” to minimize analog cable lengths.

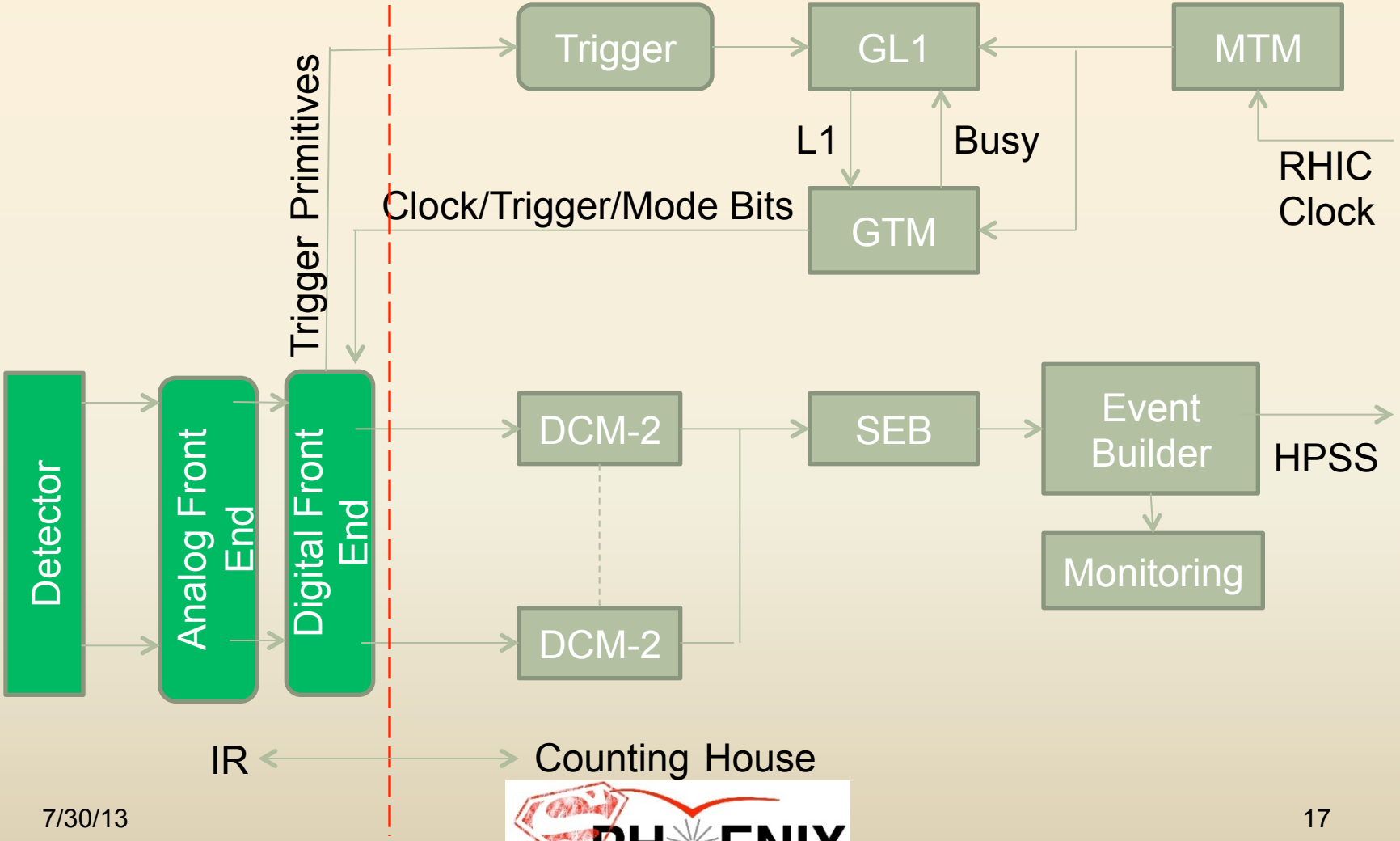
Conceptual Design for EMCal/HCal Electronics

- 96 x 256 (~24K) EMCal Channels
- 64 x 22 x 2 (~3K) HCal Channels
- 10 Khz Trigger Rate
- Level 1 Triggering
  - Trigger primitives every crossing
  - Issue Level 1 in 4μSec (40 clock ticks)
  - Dead for 1.6μSec (16 clock ticks)
  - Buffer 4 consecutive Level 1 accepts

All Digital Mode Readout

- Readout EMCAL and HCAL analog signal through direct digitizing method
  - Digitize the analog pulse with fast Analog Digital Converter
  - Provide both charge and time measurements.
  - Provide Level 1 trigger decision delay buffer and multiple accepted Level 1 event buffers
  - Simplify the analog signal processing, fully commercial solution.
  - Use up-to-date fast digital signal processing to process the data.
    - Use Multiplier, Adder etc.
    - Trigger primitives can be generated from digitized data.
- PHENIX has built 60 MHz 12 bit direct digitized electronics for Hadron Blind Detector (HBD).

sPHENIX Digital DAQ Design



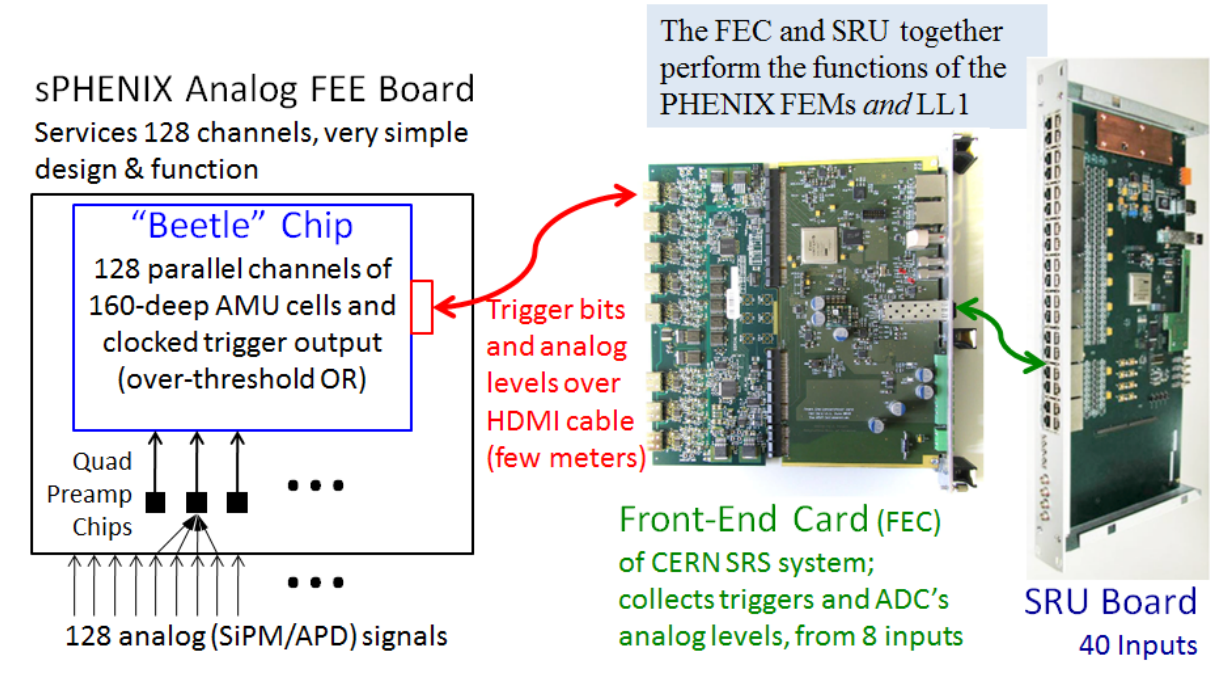
sPHENIX Digital DAQ Design

- 48 SiPM channels readout by FEM channel
  - EMCal: 512 FEM Channels
  - HCal: 59 FEM Channels
- DCM-2s:
  - 4 FEM channels per DCM-2 channel
  - 8 DCM-2 channels per DCM-2 module
  - EMCal: 16 DCM-2 modules
  - HCal: 2 DCM-2 modules
- Rack Room
  - 2 EMCal DCM-2 crates
  - 1 HCal DCM-2 crate
  - 1 Rack
- Modest extension of current PHENIX electronics

sPHENIX Mixed-Mode Design

- Based on ORNL design for ALICE FOCAL
- Analog pipeline of SiPM signals
- Uses BEETLE CHIP
  - Developed at CERN
  - 128 Channels
  - Analog pipeline, 160 cells deep/channel
  - Trigger capability, limited
- Takes advantage of CERN Scalable Readout System (SRS)
- ORNL is currently designing a BEETLE based FEE card- Prototype expected fall 2013.

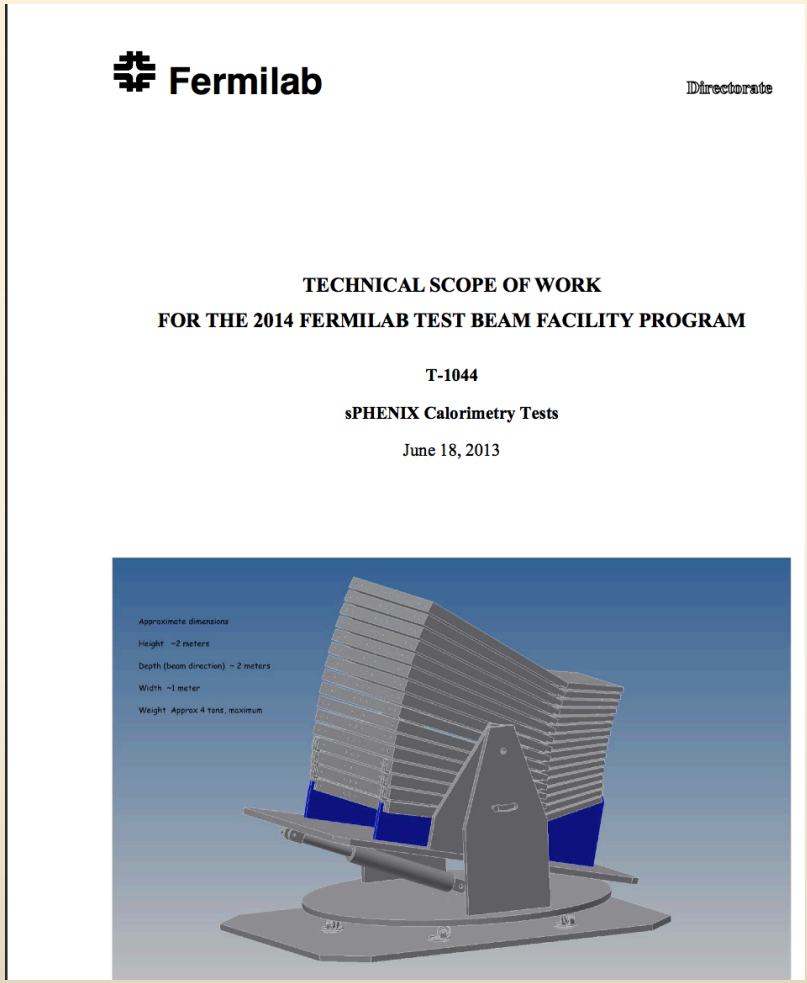
sPHENIX Mixed Mode DAQ Design



- Design is based on proposed ALICE FoCal Upgrade
- PHENIX Collaborators working on this: ORNL, CNS/Tokyo
- sPHENIX would require 220 FEE, 27 FEC boards, 1 SRU/ Crate

T-1044 Test Beam

- Proposal was submitted June 18, 2014
- Currently under reviewed.
- Goals are to evaluate:
  - HCal module
  - EMCal module
  - SiPM front-end electronics
    - Commercial premaps
    - ORNL buffer/amp
    - Temperature compensation
  - Digital backend readout: PHENIX HBD Readout
  - SRS system with BEETLE Chip FEE (ORNL is developing)



Fermilab Directorate

TECHNICAL SCOPE OF WORK

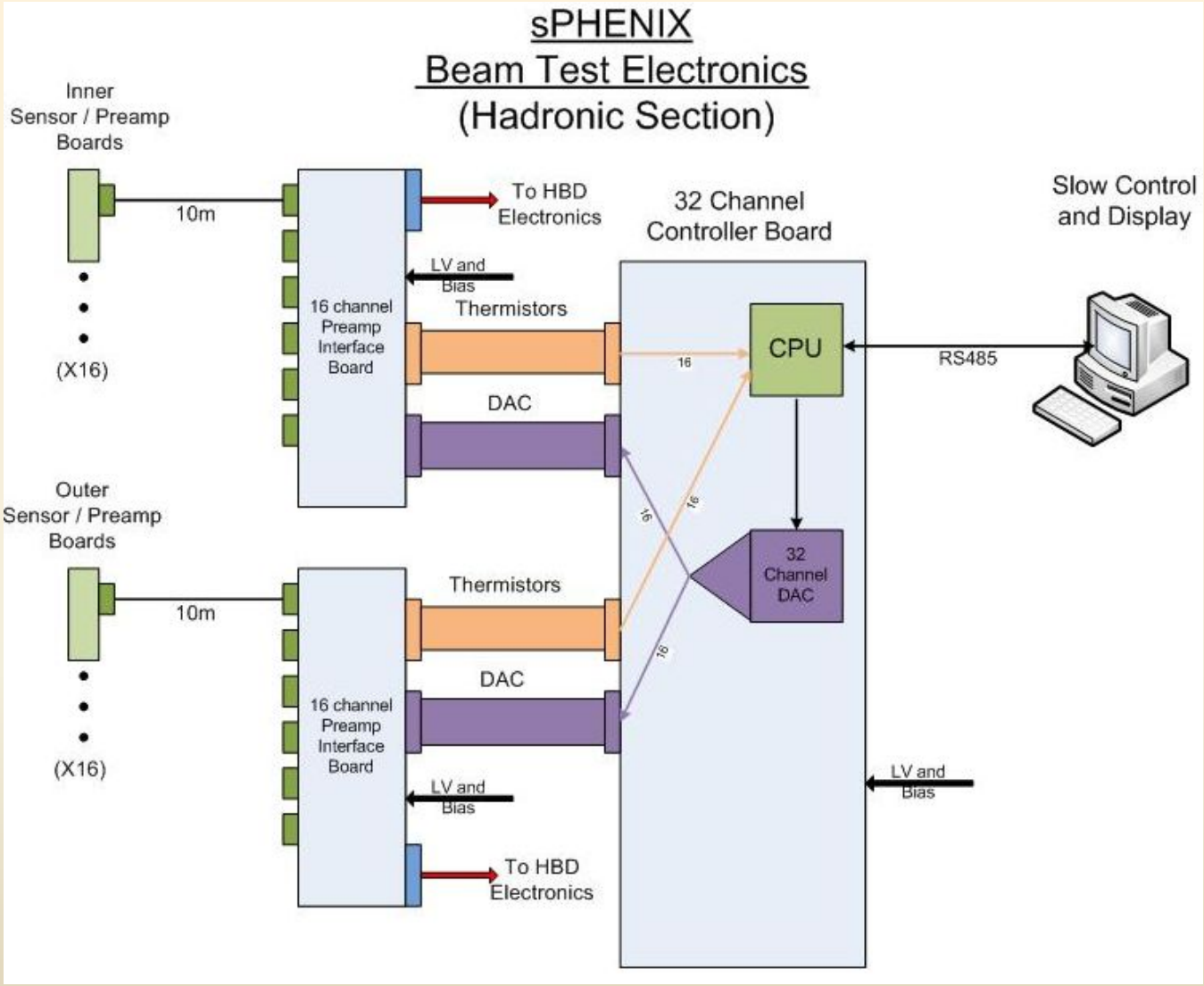
FOR THE 2014 FERMILAB TEST BEAM FACILITY PROGRAM

T-1044

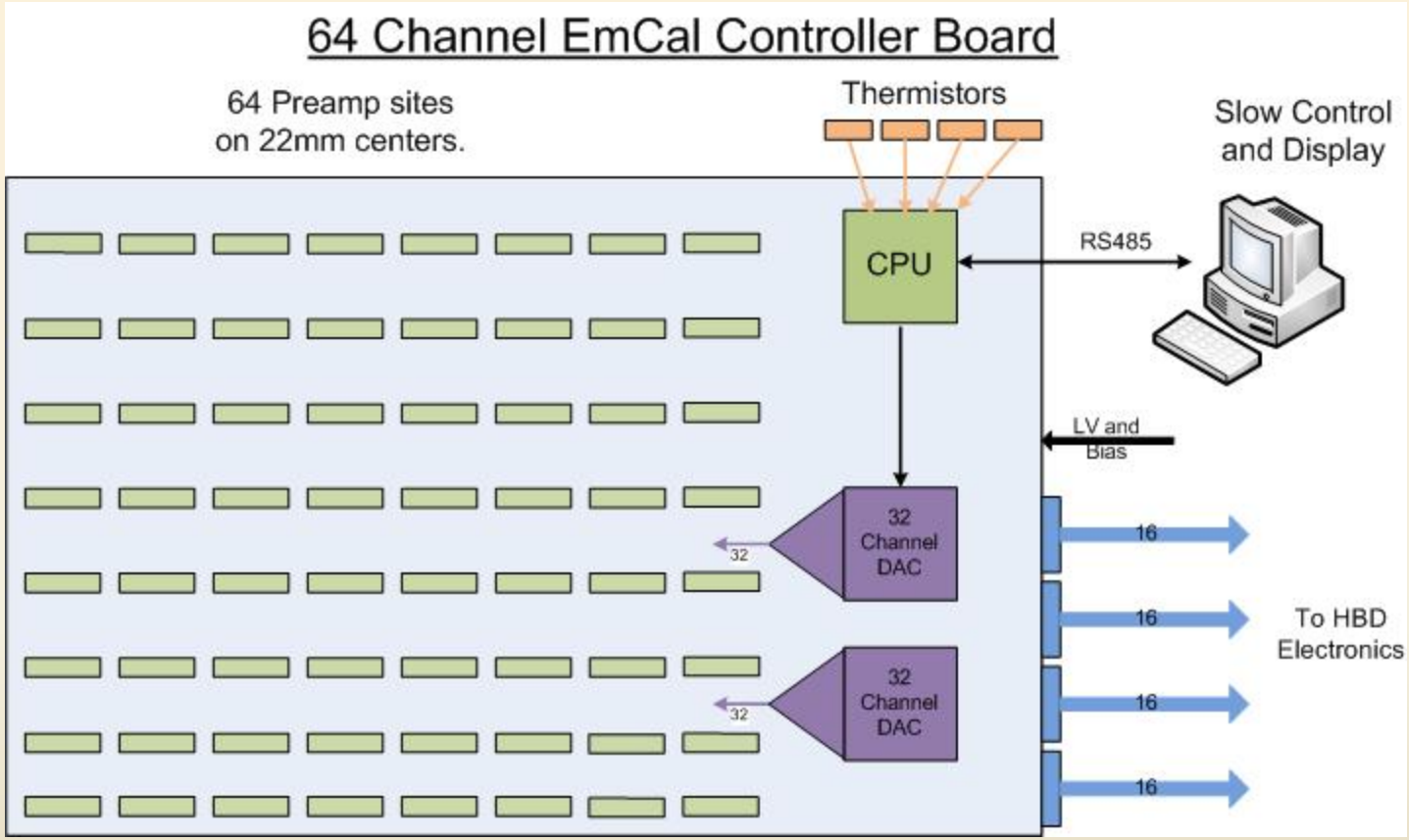
sPHENIX Calorimetry Tests

June 18, 2013

Test Beam Electronics: HCal

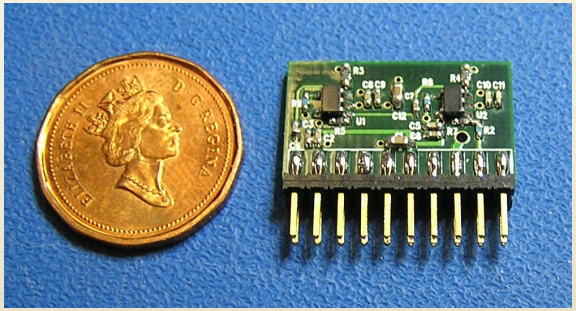


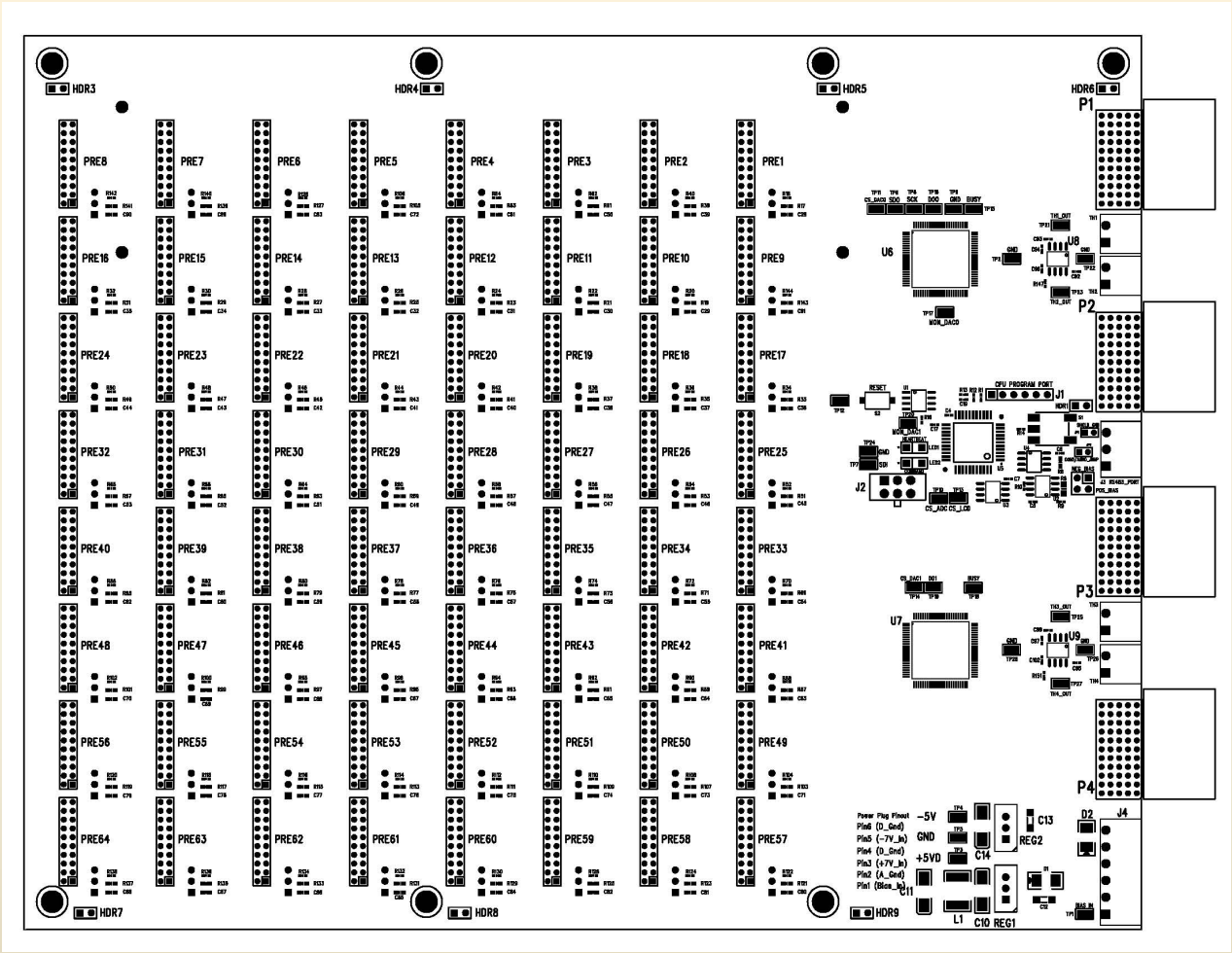
Test Beam Electronics: EMCal



Test Beam Electronics: EMCal

- Board allows for 64 SiPM connections on back
- Plug in Pre-Amp modules allow for testing different preamps easily.
- Mounts to back of EMCal “Egg Carton”





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Conclusions

- SiPM sensor looking vary promising and meet requirements of sPHENIX:
  - Dynamic range
  - Immune to magnetic fields,
  - High gain
  - Low cost
  - New devices coming to market every day.
- Two readout schemes under active consideration
  - All digital, similar to PHENIX HBD system
  - Mix mode based on BEETLE Chip and SRS system
- T-1044 effort at FNAL will give us a lot of experience with SiPMs and readout electronics.
- Still lots of work to be done to select and finalize readout electronics.