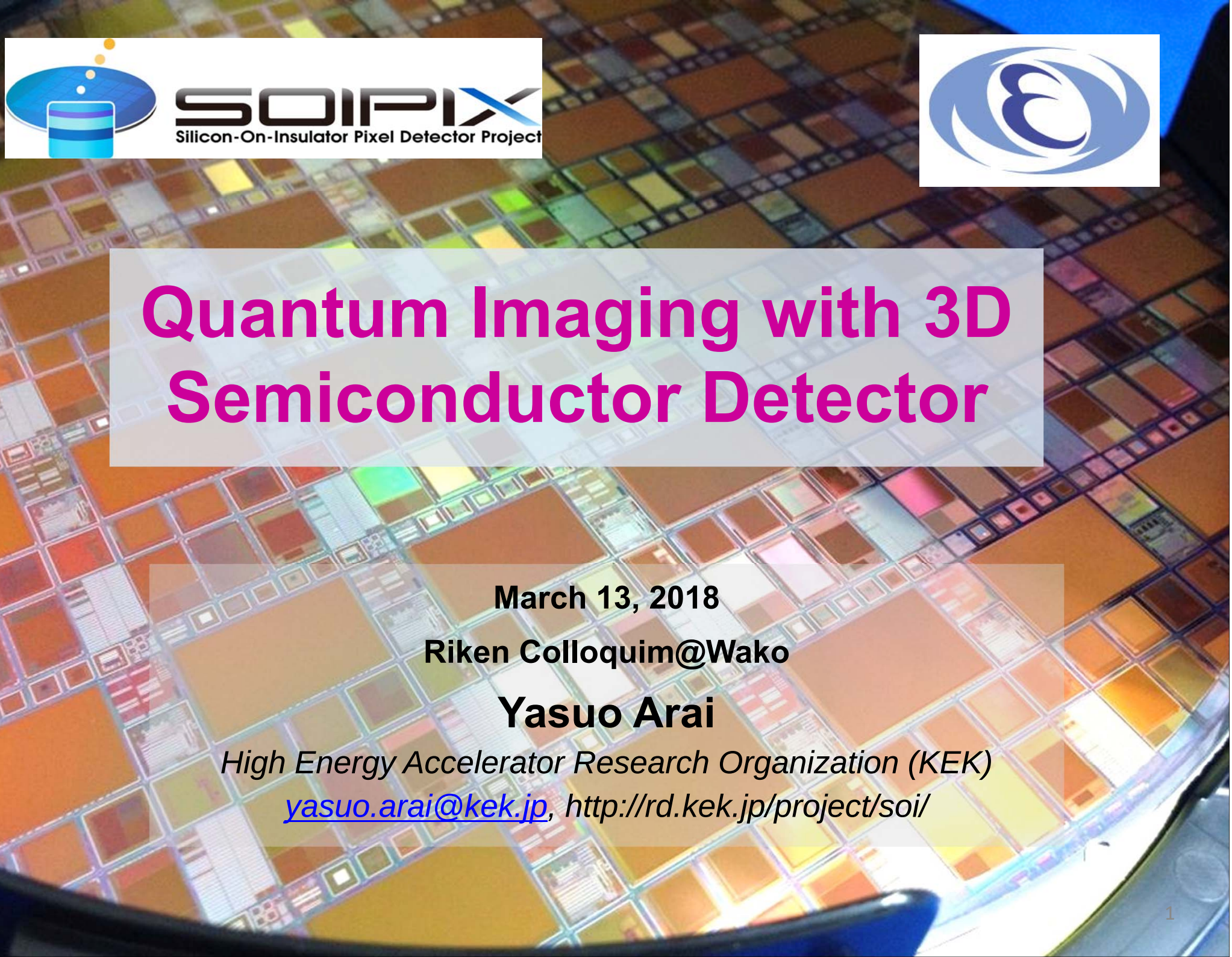

Quantum Imaging with 3D Semiconductor Detector

March 13, 2018

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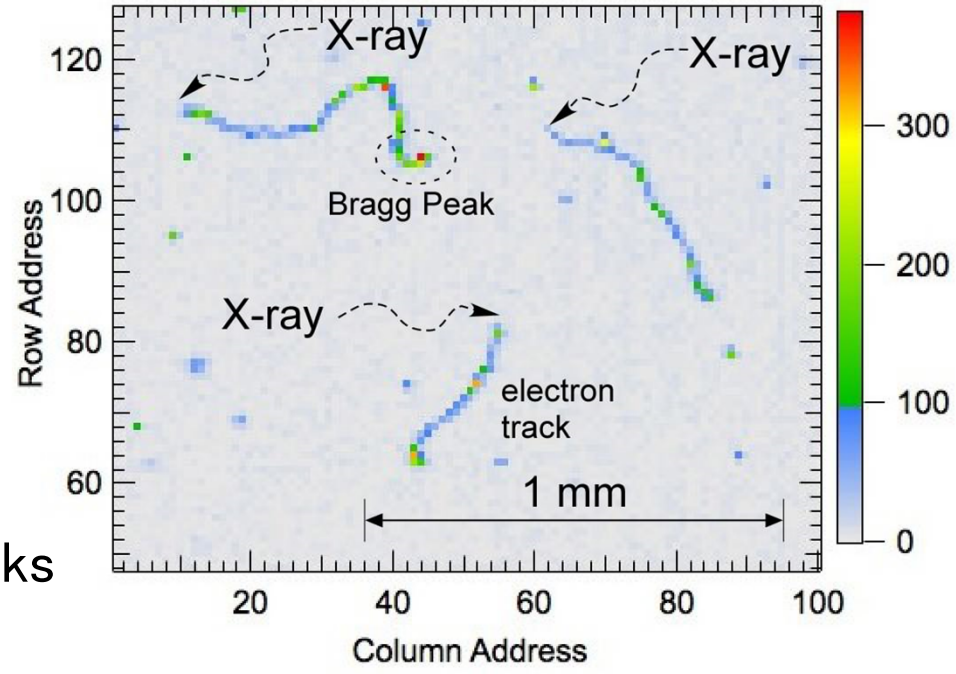
Outline

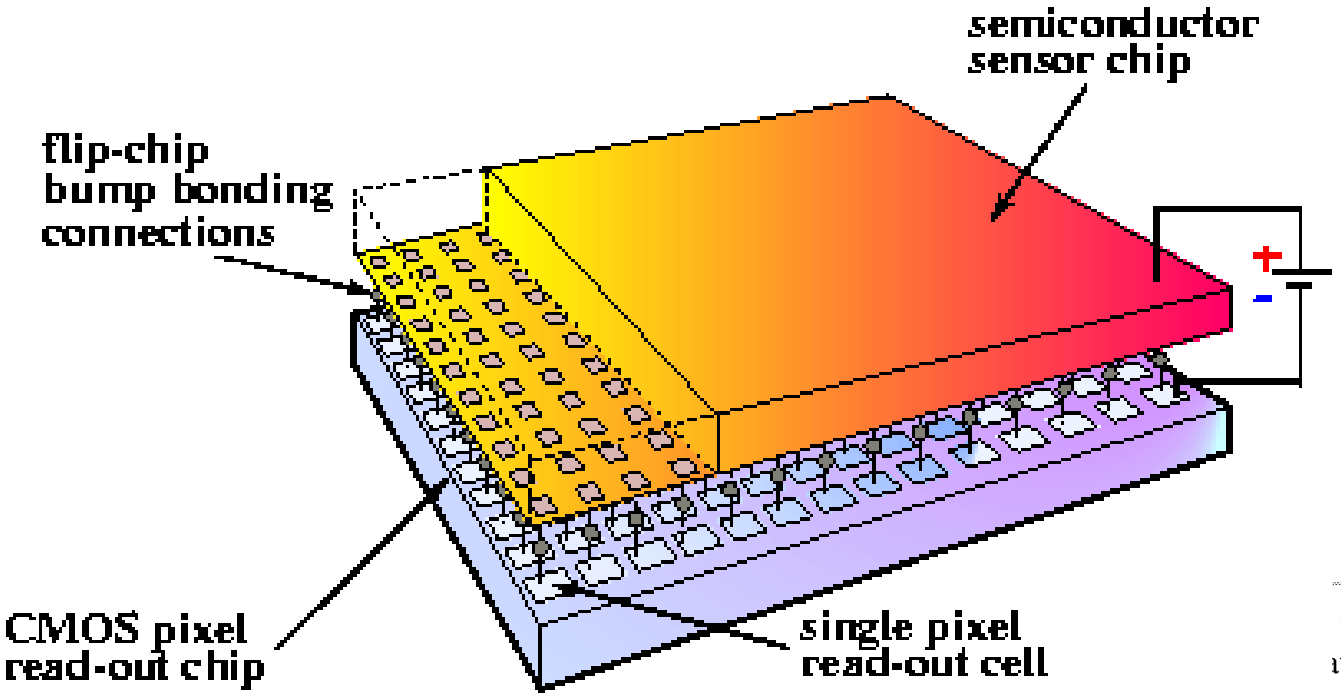
I. Introduction
II. SOI Pixel Process
III. Detector Examples
IV. Summary

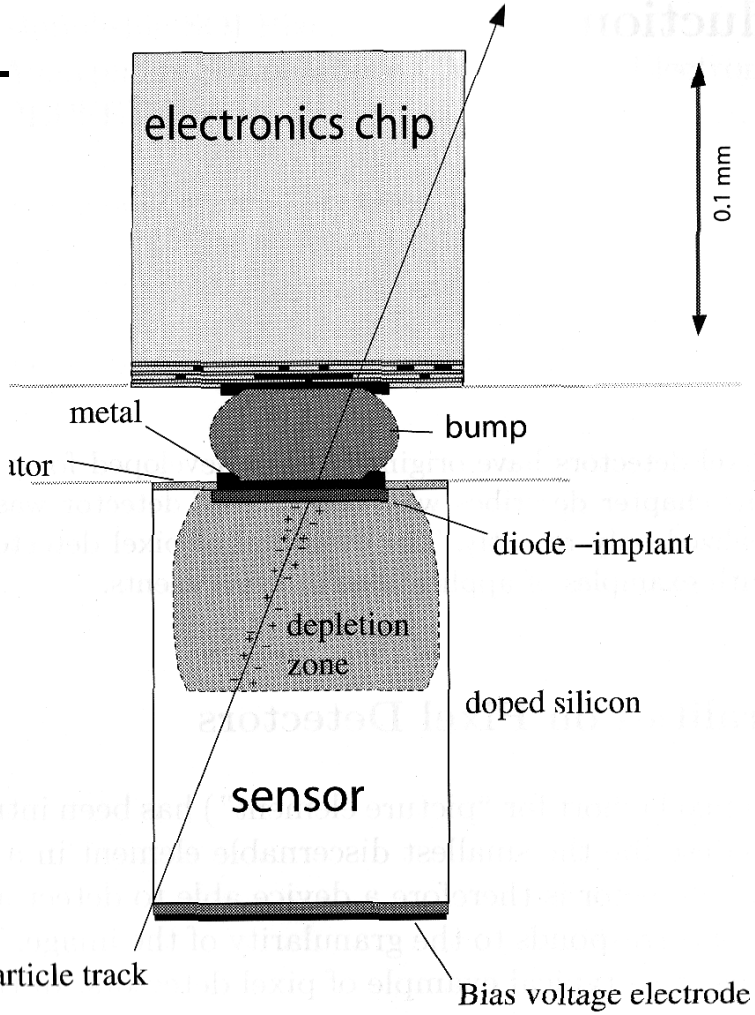


Compton Electrons Tracks

I. Introduction

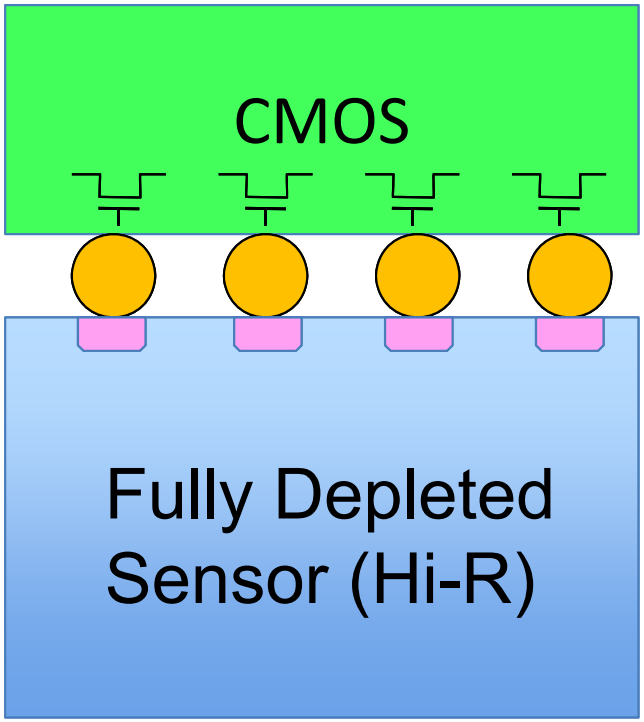
Pixel Detector used in CERN LHC (Hybrid Pixel)





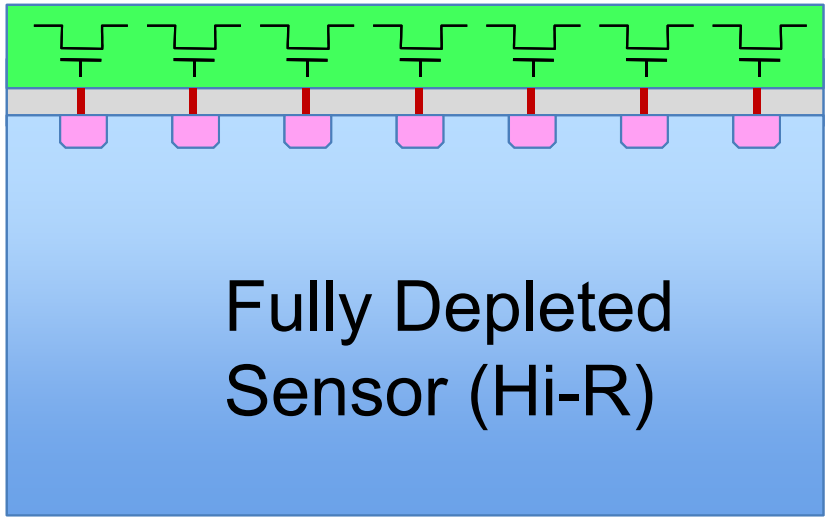
- Large number of metal bump bondings.
  → Low Yield and High Cost
- Performances are limited by the bump size.

Hybrid Detector



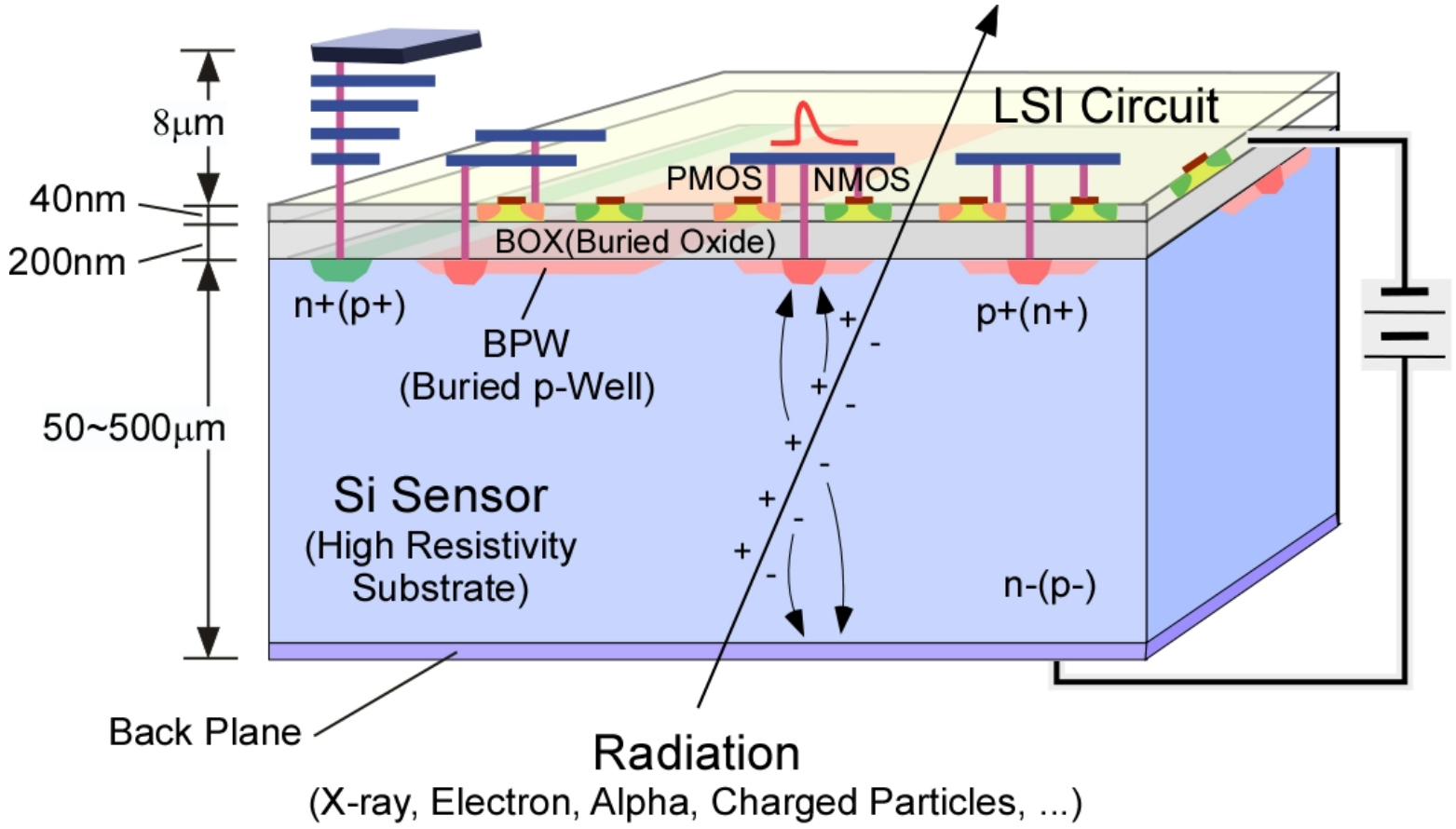
Monolithic

Silicon-On-Insulator (SOI)



SOI technology is a natural solution in the evolution of radiation pixel sensor.

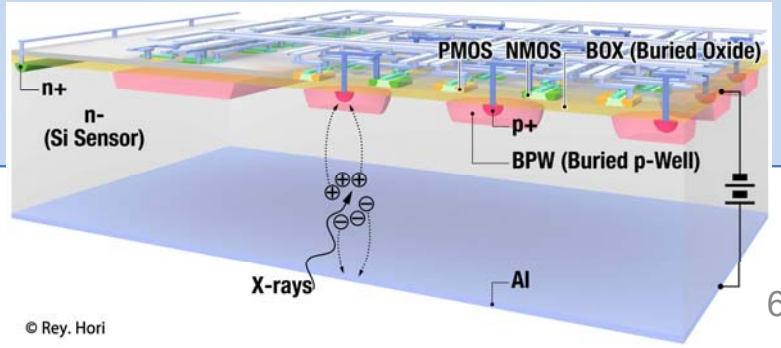
Silicon-On-Insulator Pixel Detector (SOIPIX)



Monolithic Detector having fine resolution of silicon process and high functionality of CMOS LSI by using a SOI Pixel Technology.

Features of SOI Pixel Detector

- Monolithic device. No mechanical bonding.
- Fabricated with semiconductor process only.
  → High reliability and Low Cost.
- High Resistive fully depleted sensor (50um~700um thick) with Low sense node capacitance. → Large S/N.
- On Pixel processing with CMOS circuits.
- No Latch up and very low Single Event cross section.
- Can be operated in wide temperature (1K-570K) range.
- Based on Industry Standard Technology.



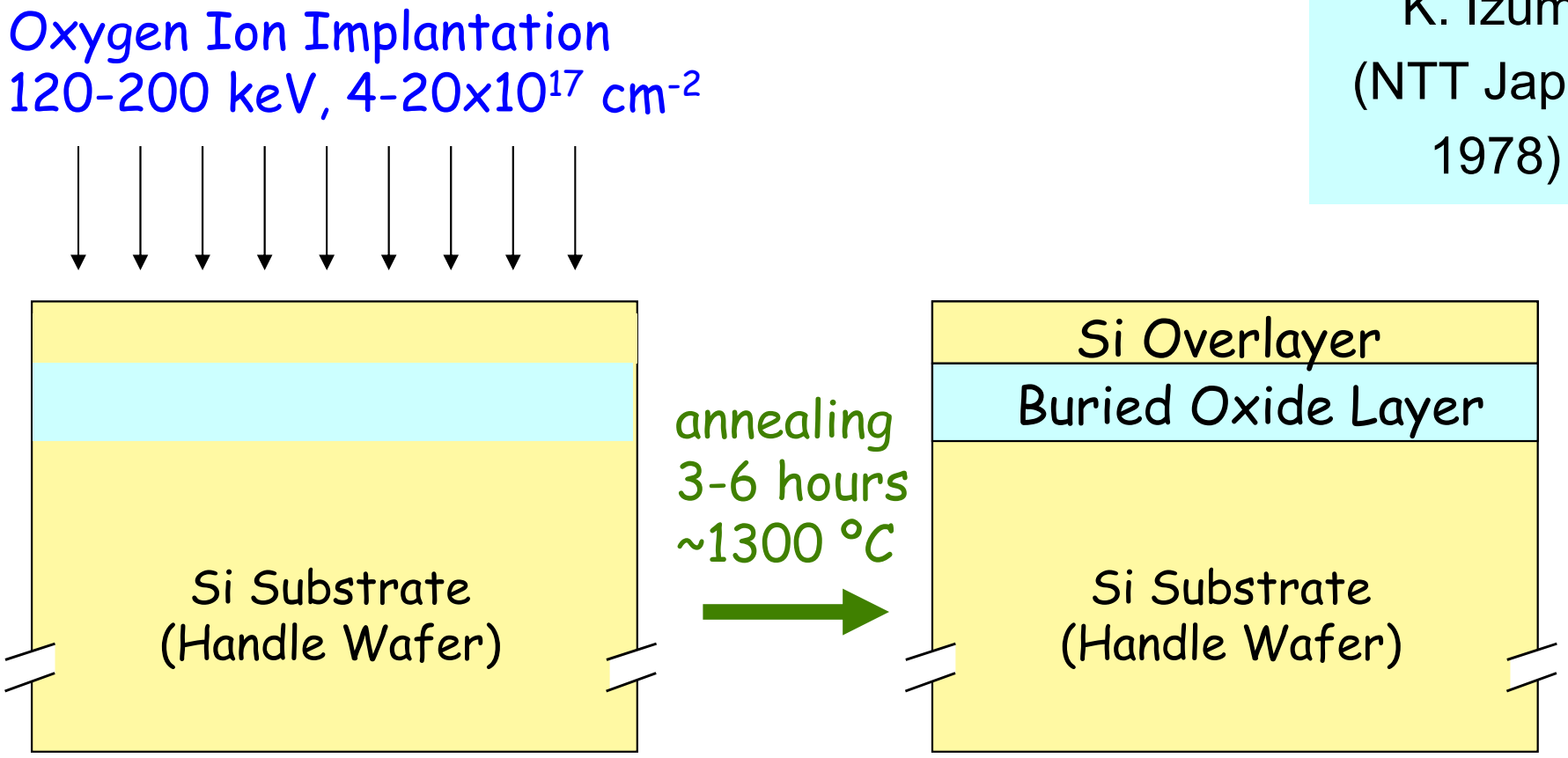
First SOI Wafer (SIMOX)

First good quality SOI wafer

SIMOX (Separation by Implanted Oxygen)

This took long implantation time of Oxygen, so the production cost was very high and applications are limited.

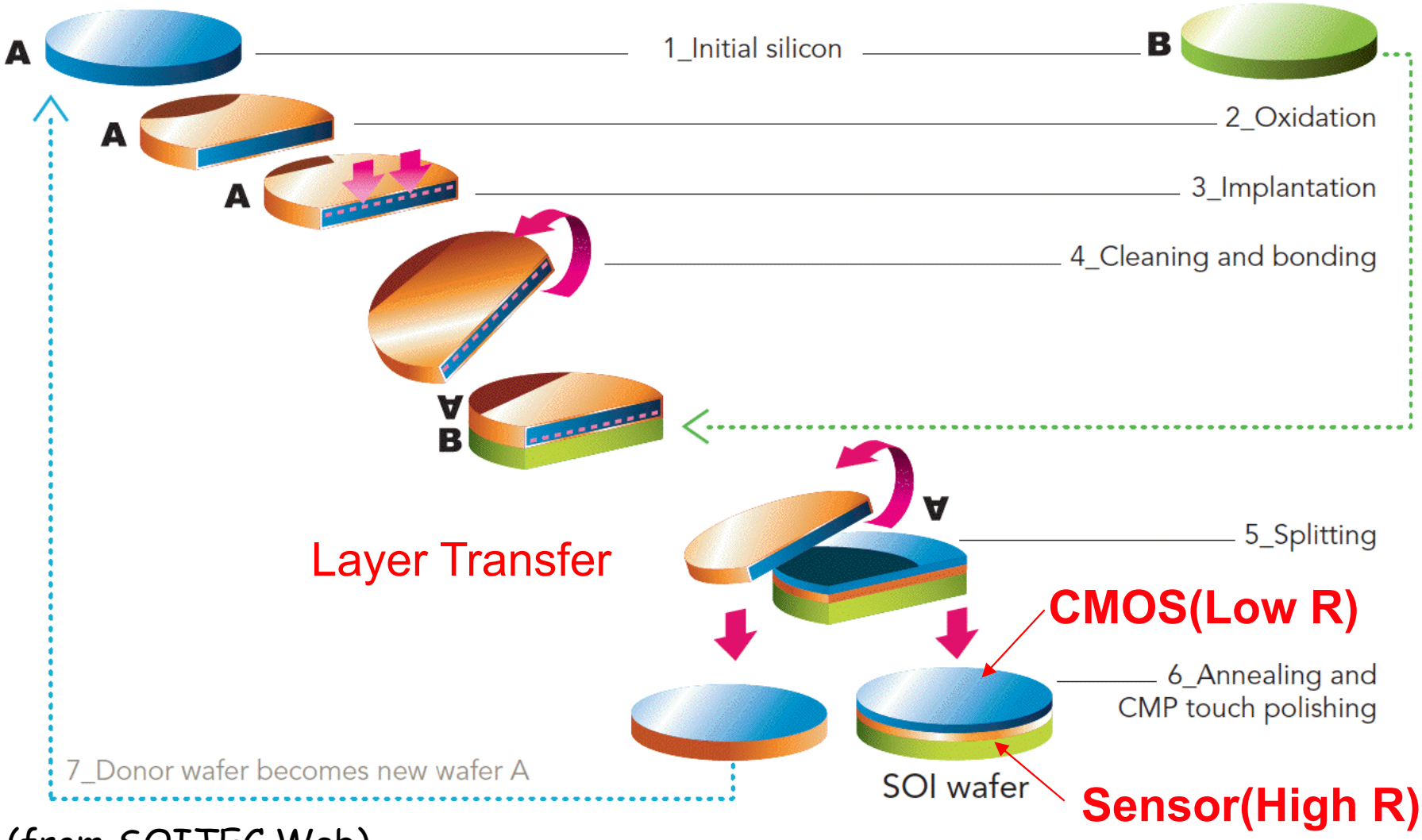
K. Izumi
(NTT Japan, 1978)



Pesent SOI Wafer (SmartCut™)

Michel. Bruel (Leti, 1991)

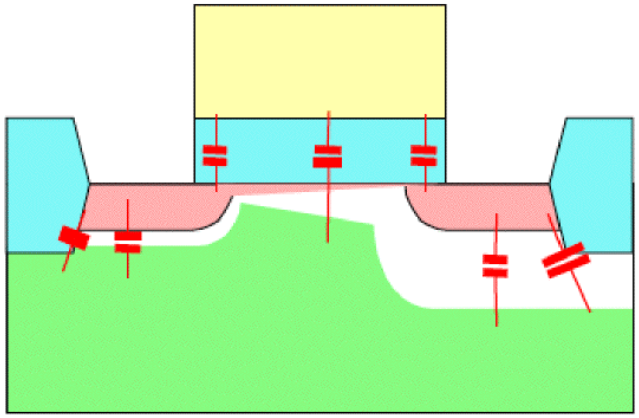
Become popular after 2000. soitec



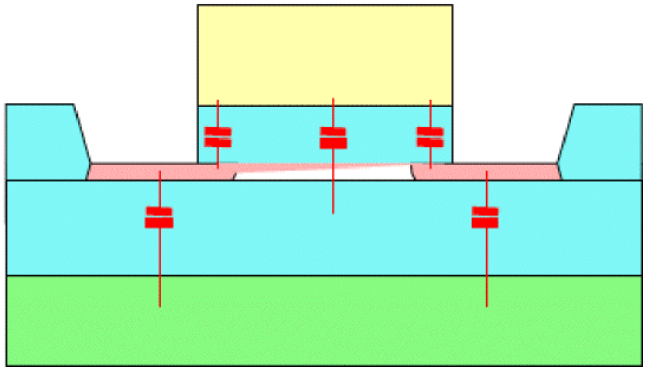
(from SOITEC Web)

SOI Performance : Smaller Junction Capacitance

Bulk



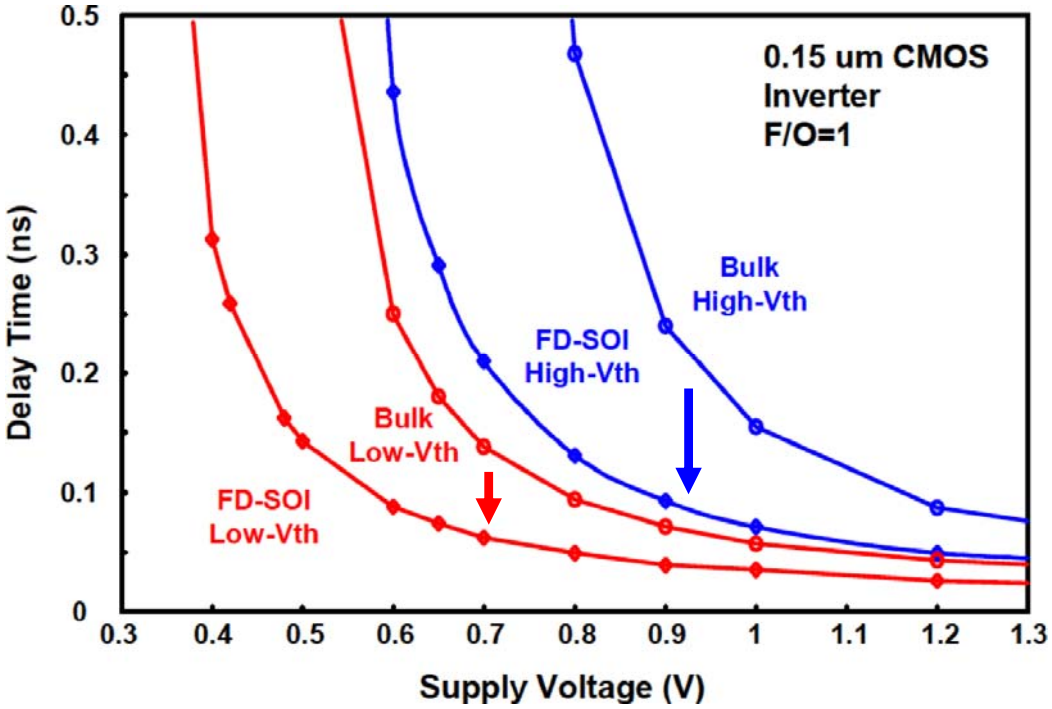
SOI



Cj is 1/10 of Bulk technology.

Gate Capacitance is 30-40% Lower.

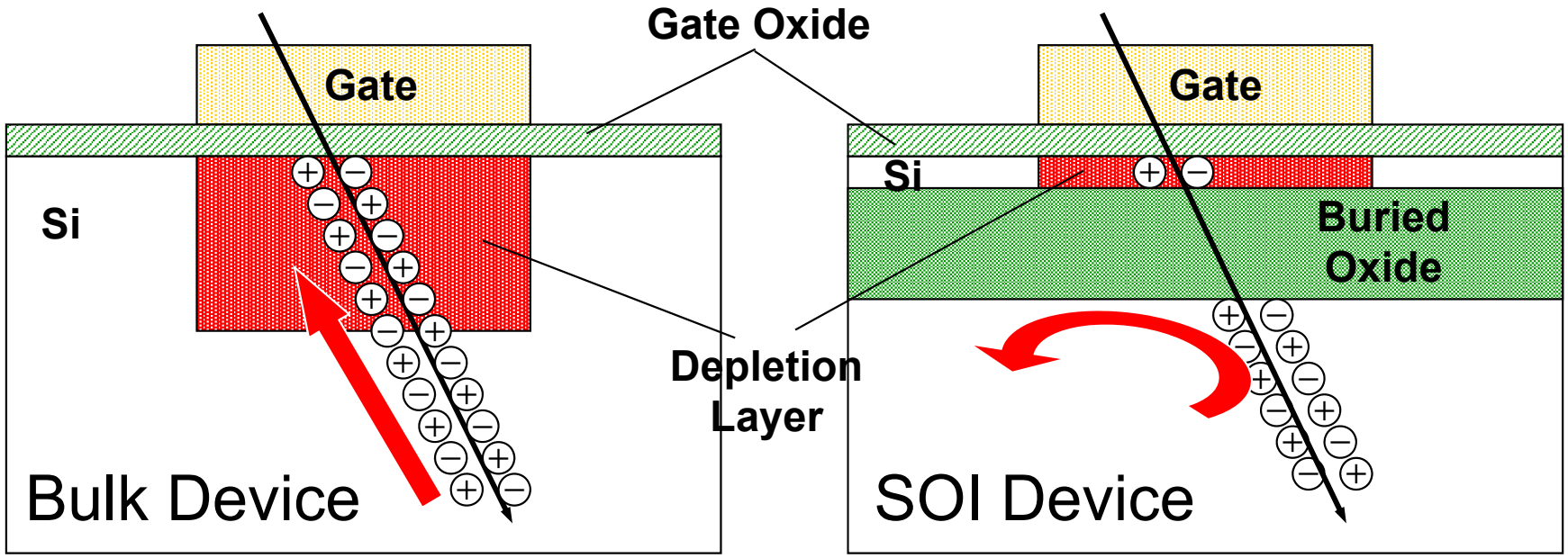
High Speed / Low Power



9

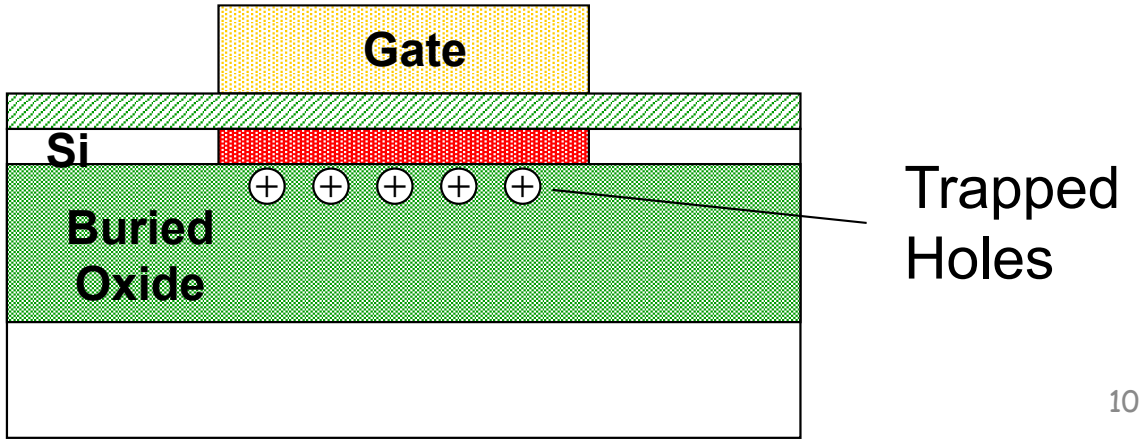
Radiation Tolerance

SOI is Immune to Single Event Effect



But not necessary strong to Total Ionization Dose due to thick BOX layer

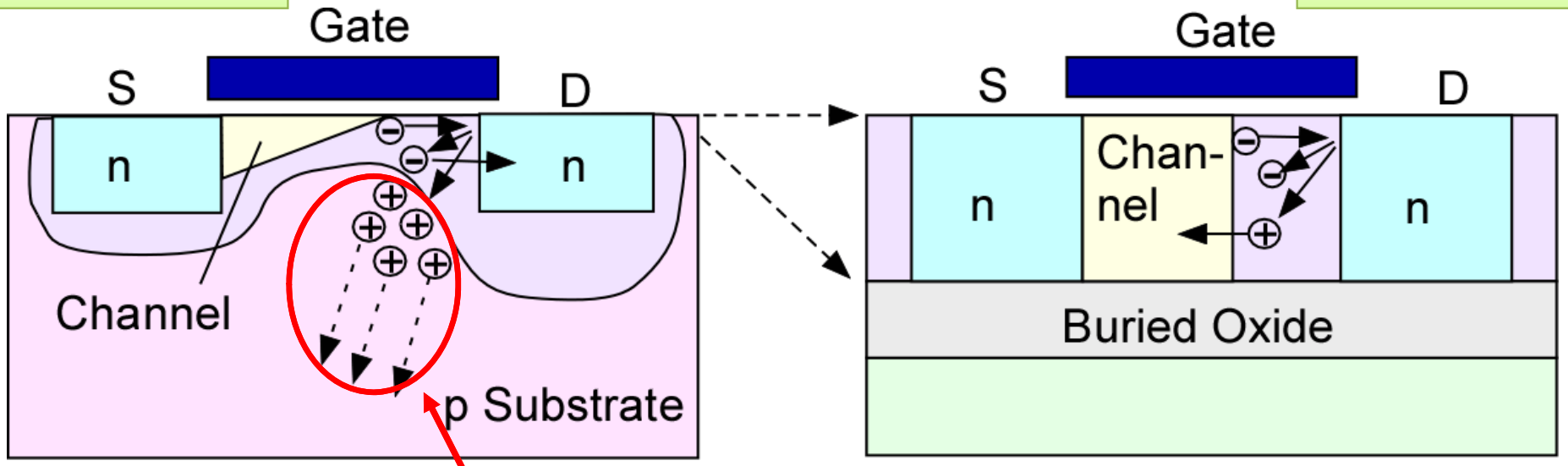
This must be remedy for the application under high radiation environment.



Operation at Cryogenic Temperature

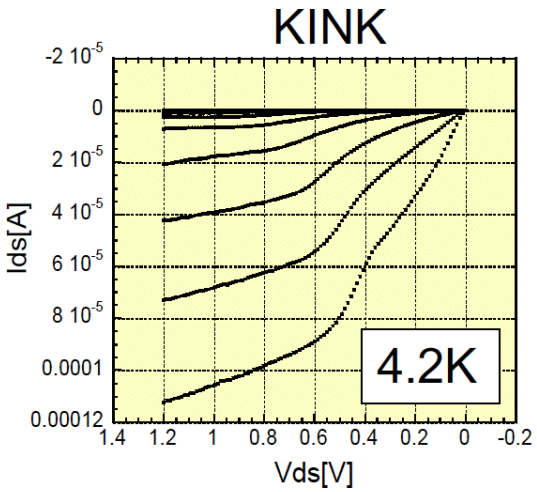
Bulk MOS

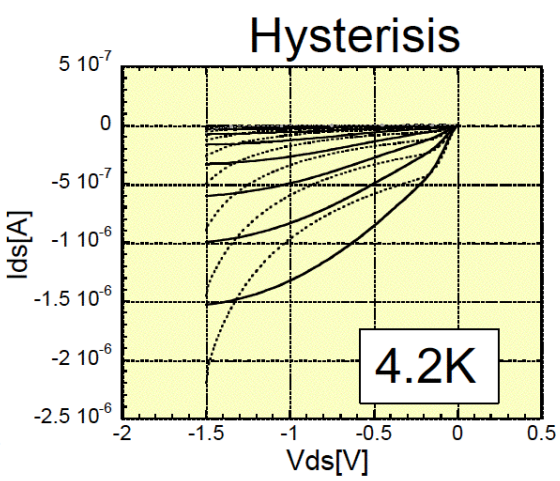
SOI MOS

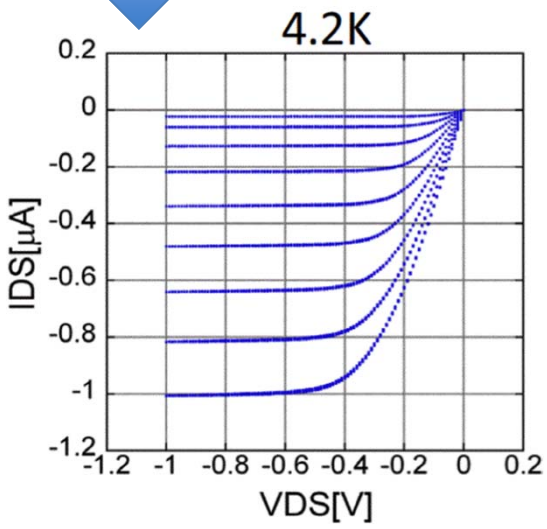


Carrier Freeze

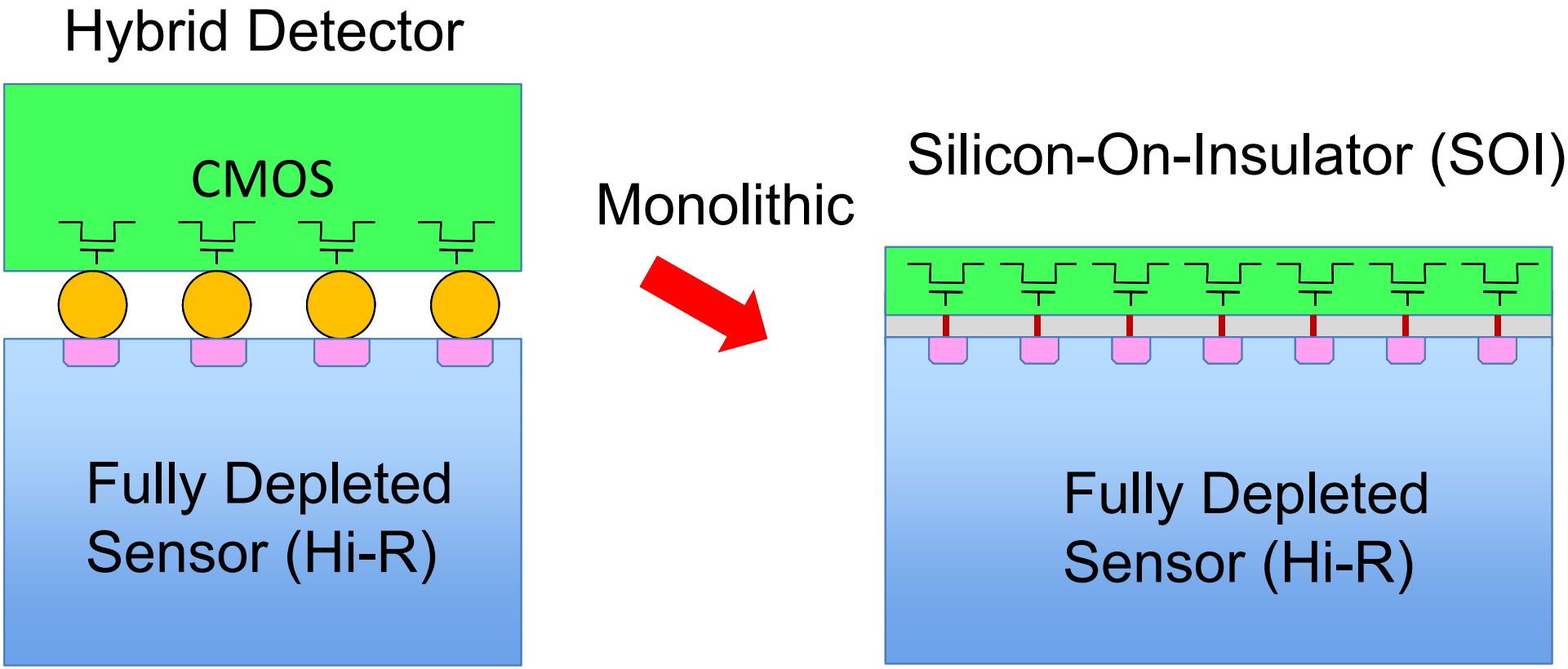
< 4.2K







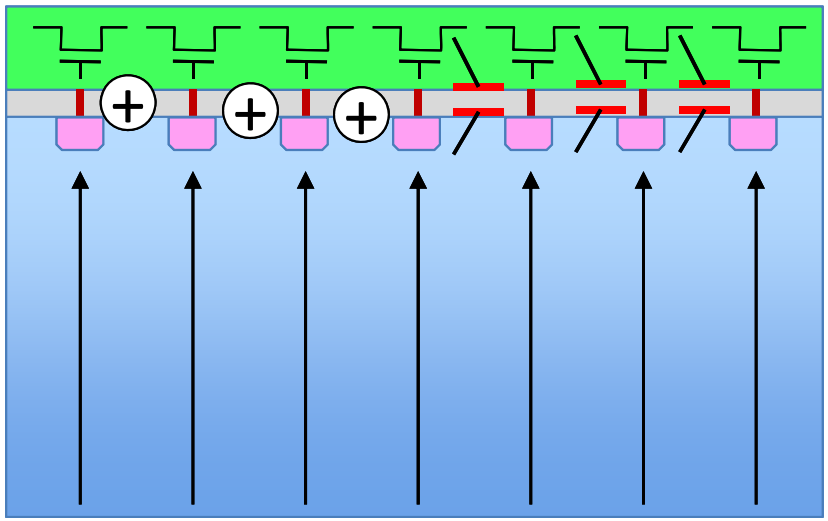
II. SOI Pixel Process



To use SOI technology for pixel detector is already discussed in 1990(*).

(*) Jean-Pierre Colinge, 'An overview of CMOS-SOI technology and its potential use in particle detection systems', NIM A305 (1991) 615-619.

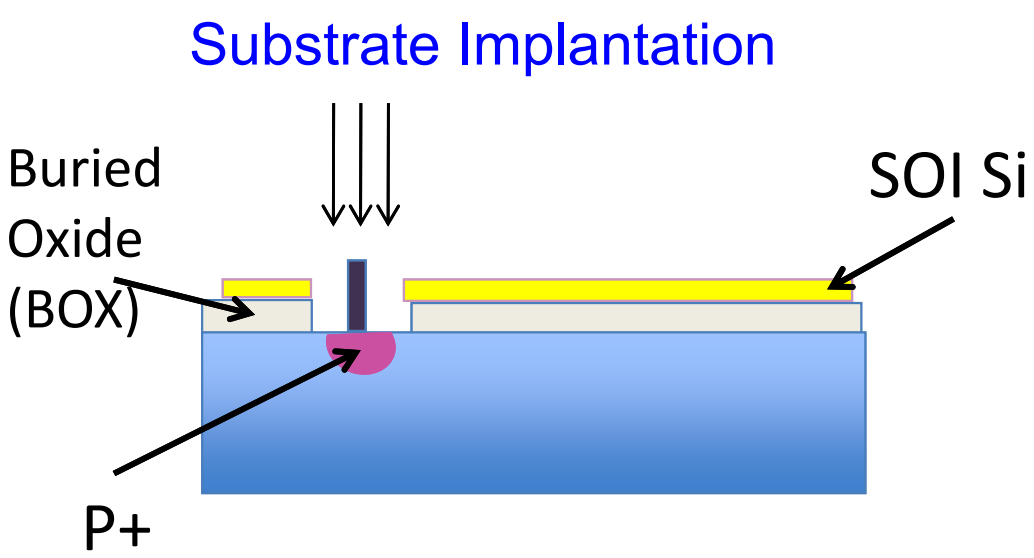
Issues in SOI Pixel

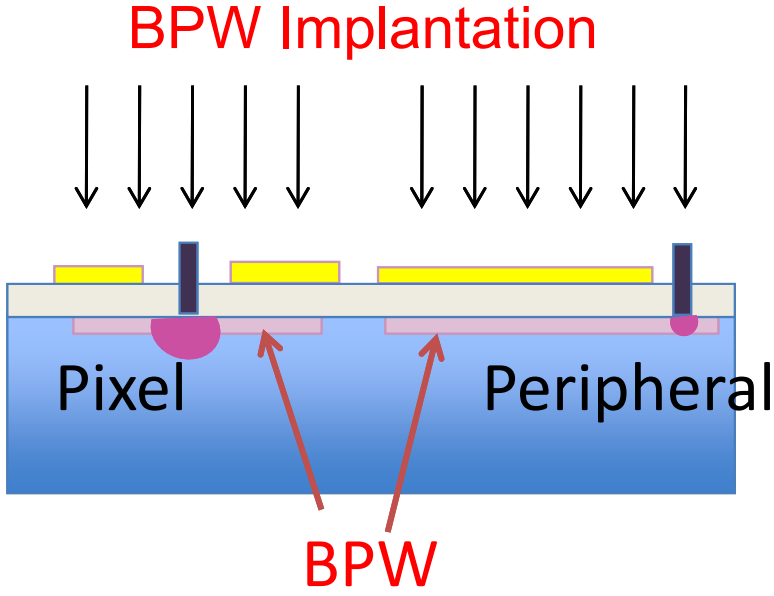


- Transistors does not work with Detector High Voltage. (Back-Gate Effect)
- Circuit signal and sense node couples. (Signal Cross Talk)
- Oxide trapped hole induced by radiation will shift transistor threshold voltage. (Radiation Tolerance)

Unfortunately, in 1990s, due to immature process technology, no good high-resistivity SOI wafer etc. , many SOI sensor R&D projects were stopped.

Buried p-Well (BPW)





- Cut Top Si and BOX
- High Dose

- Keep Top Si not affected
- Low Dose

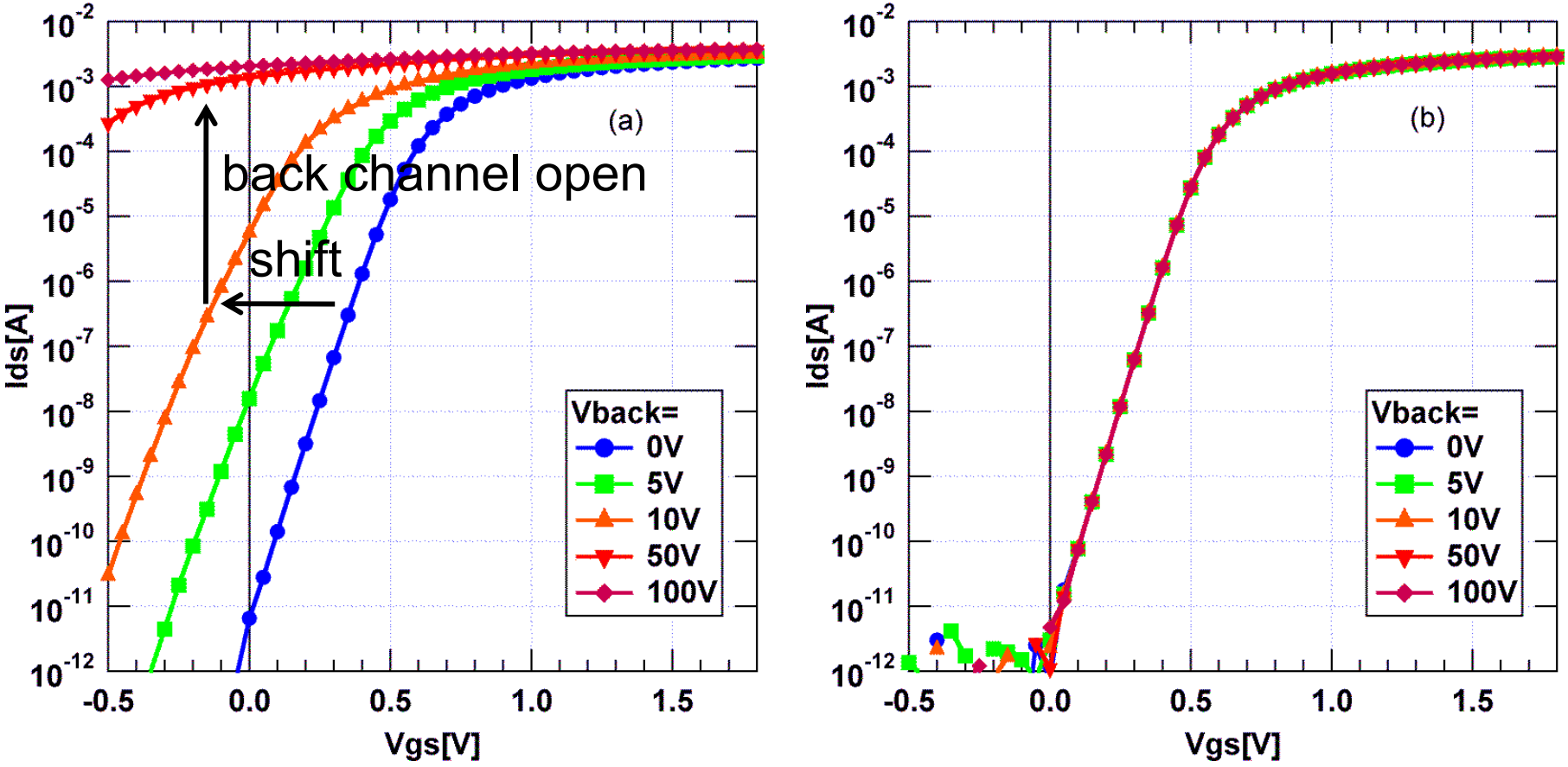
- Suppress the **Back Gate Effect**.
- Shrink pixel size without loosing sensitive area.
- Increase break down voltage with low dose region.
- Reduce electric field in the BOX which improve radiation hardness.

I_{ds}-V_{gs} and BPW

w/o BPW

with BPW=0V

NMOS



Back-gate effect is completely suppressed by the BPW.

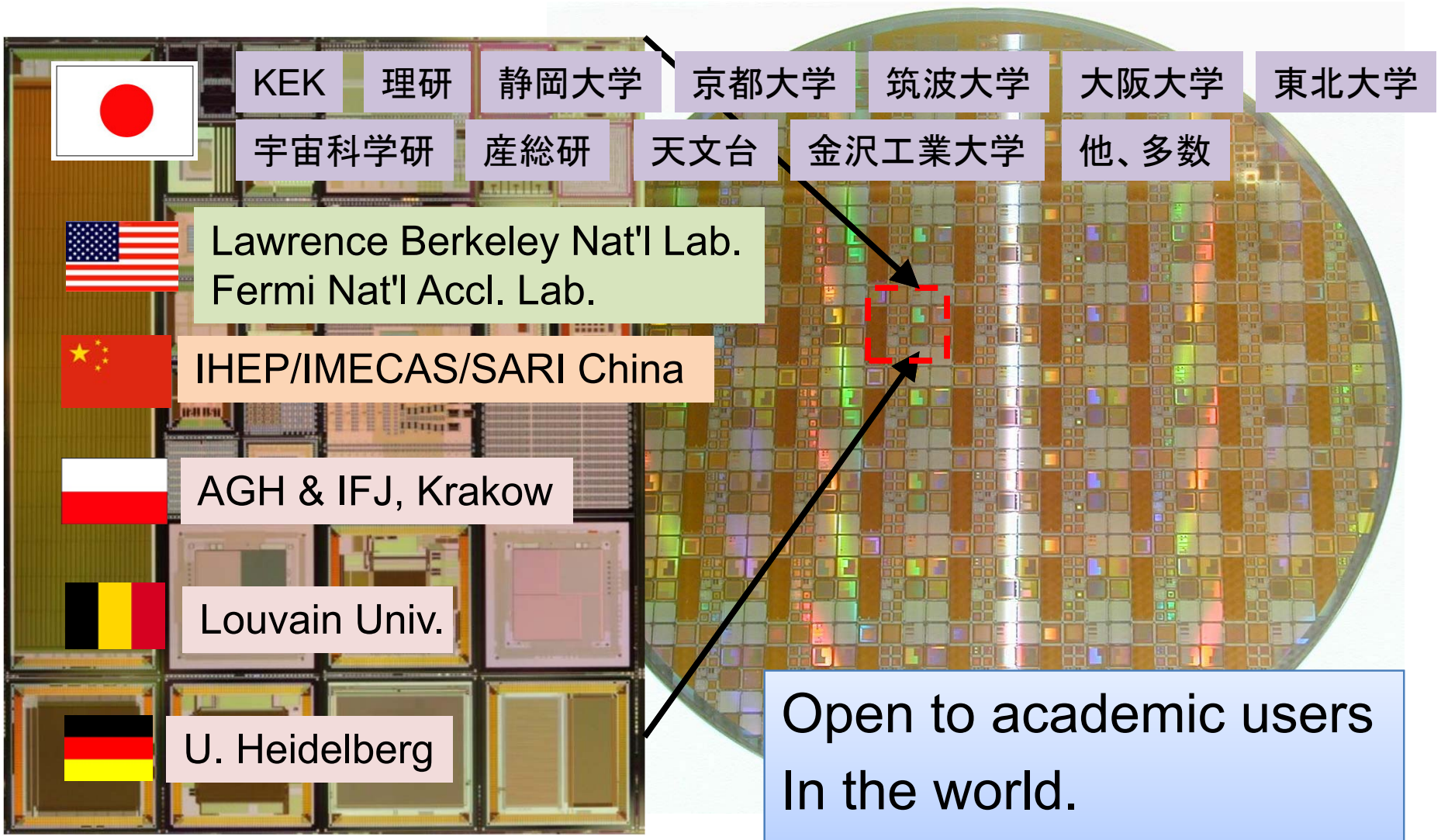
Lapis Semi.(*) 0.2 μm FD-SOI Pixel Process

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS 1 Poly, 5 Metal layers. MIM Capacitor (1.5 fF/um^2), DMOS Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer (single)	Diameter: 200 mmϕ, 720 μm thick Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz (n) ~700 Ω-cm, FZ(n) > 2k Ω-cm, FZ(p) ~25 k Ω-cm etc.
Backside process	Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating

(*) Former OKI Semiconductor Co. Ltd.

Multi-Project Wafer (MPW) run (1~2 times / year)

0.2 μm SOI-CMOS Pixel Process

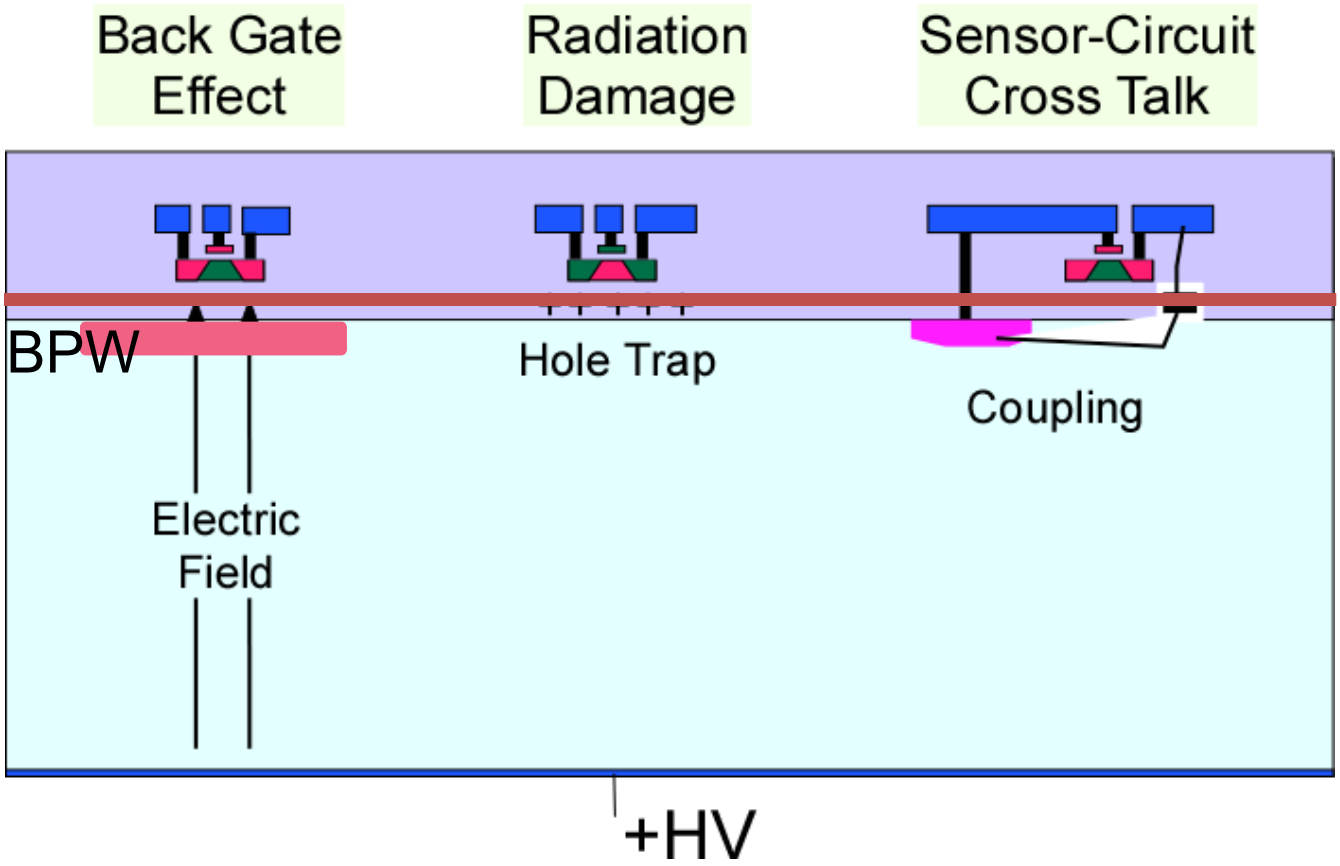


Mask Size 24.6 x 30.8 mm^2

Open to academic users
In the world.
Very unique process!

Issues in SOI detector

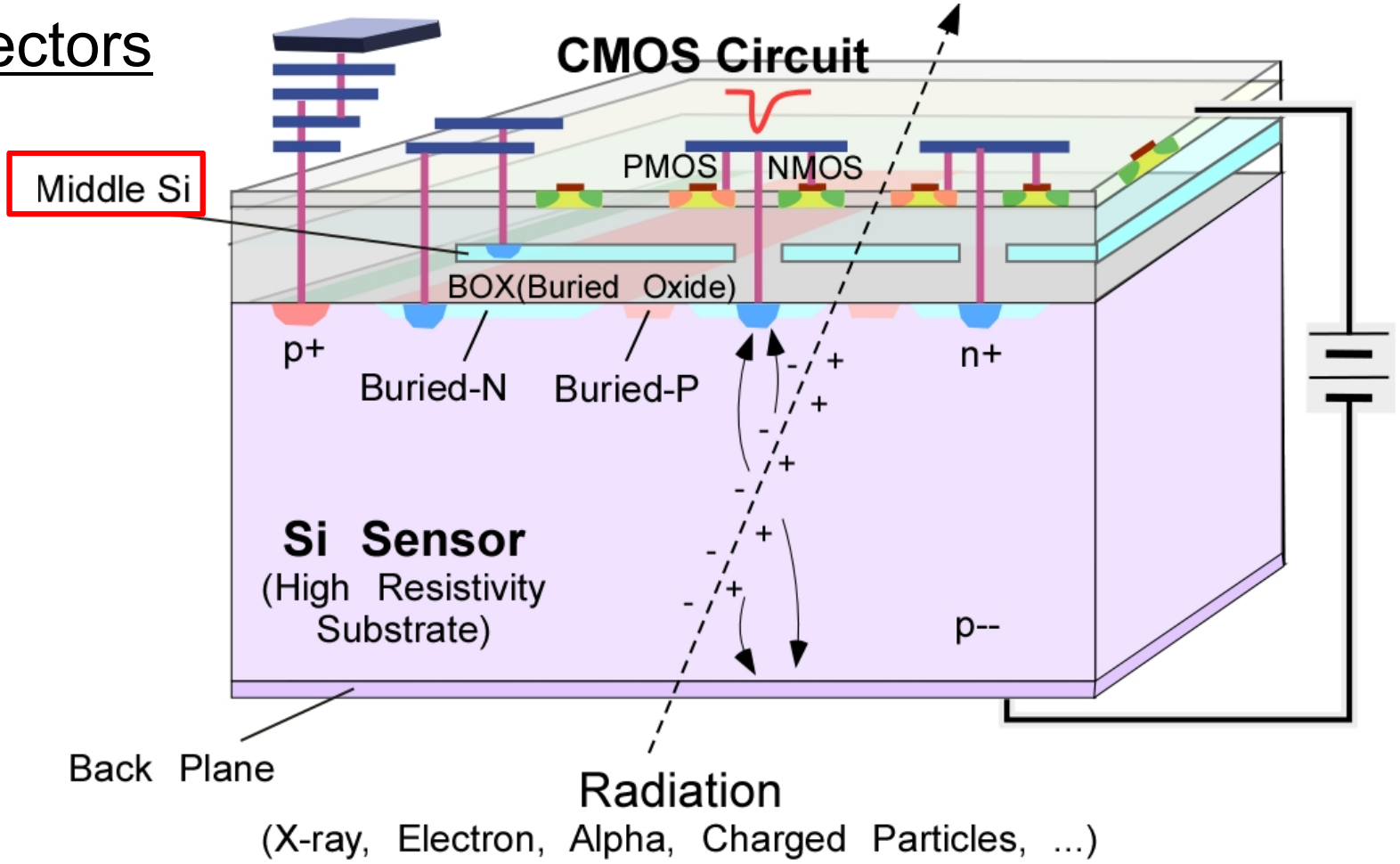
Sensor and Electronics are located very near. This cause ..



The BPW layer solved the back gate issue, but other issues are not yet solved.

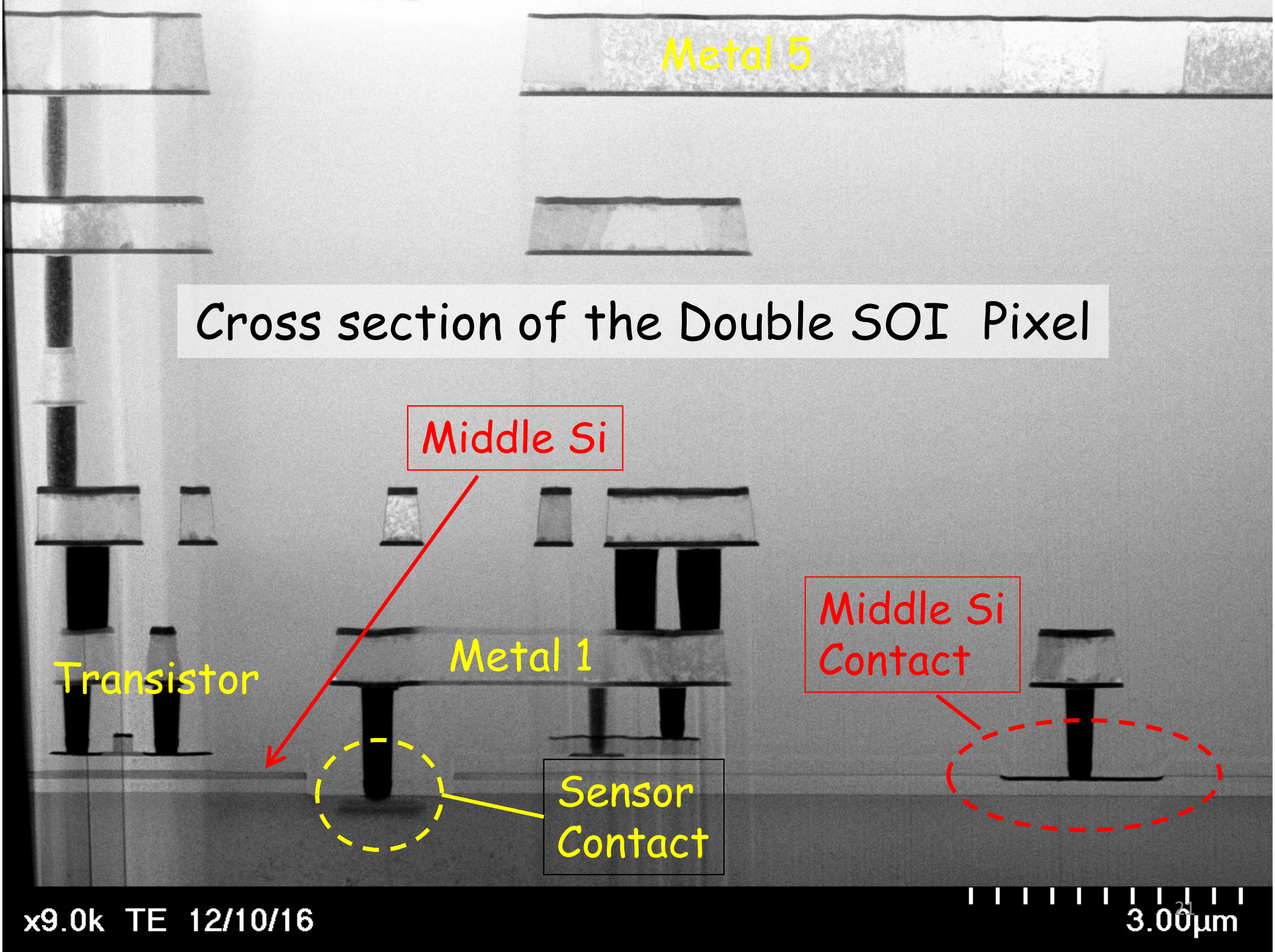
Then we introduced additional conductive layer under the transistors (→ Double SOI).

SOIPIX Detectors (Double)



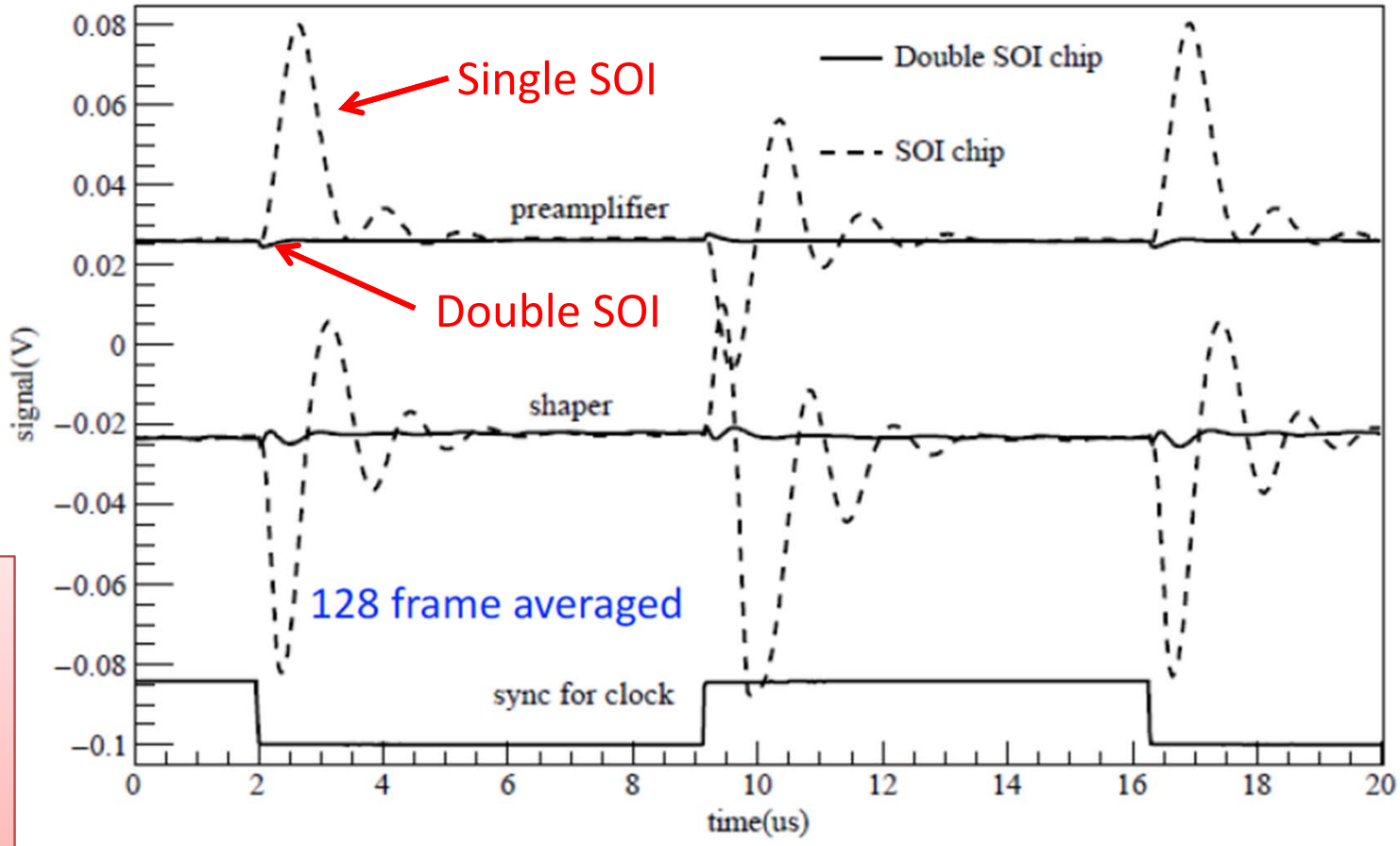
Double SOI Detector

- Middle Si layer shields coupling between sensor and circuit.
- It also compensate E-field generated by radiation trapped hole.
- Good for Complex function and Counting-type sensor.
- Can be used in High radiation environment.


Metal 5
Cross section of the Double SOI Pixel
Middle Si
Transistor
Metal 1
Middle Si
Contact
Sensor
Contact
x9.0k TE 12/10/16
3.00µm

Effect of Double SOI

Cross Talk from Clock line



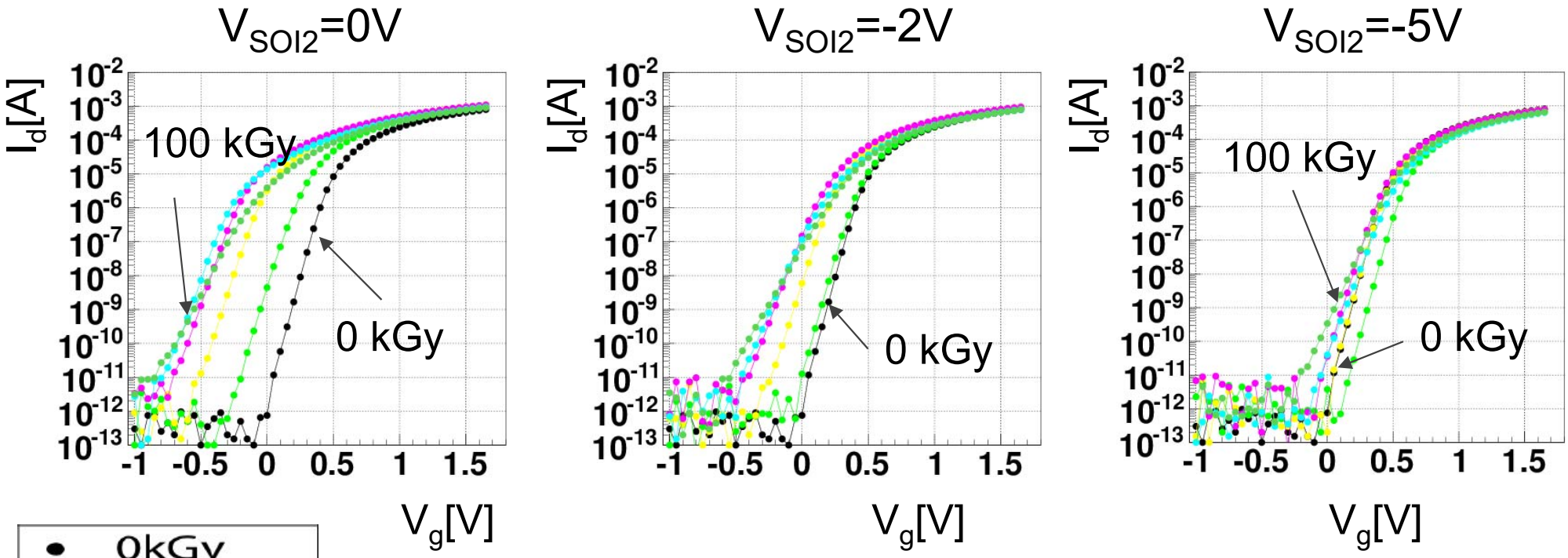
(by Lu Yunpeng (IHEP))

Shield:
Cross Talk between Circuit and Sensor is reduced to 1/20.

Gamma-ray Irradiation Test
(Id-Vg Characteristics v.s. SOI2 Potential)

I/O normal Vth
Source-Tie Tr.
L/W =0.35um/5um

NMOS



By setting Middle Si potential (Vsoi2) to -5V, Id-Vg curve returned nearly to pre-irradiation value at 100 kGy(Si) (10 Mrad).

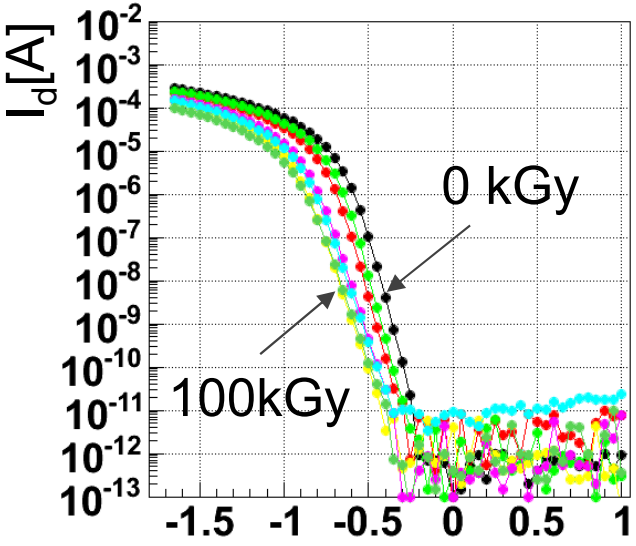
(by U. of Tsukuba)

Variation of Id-Vg Characteristics and Effect of SOI2 Potential

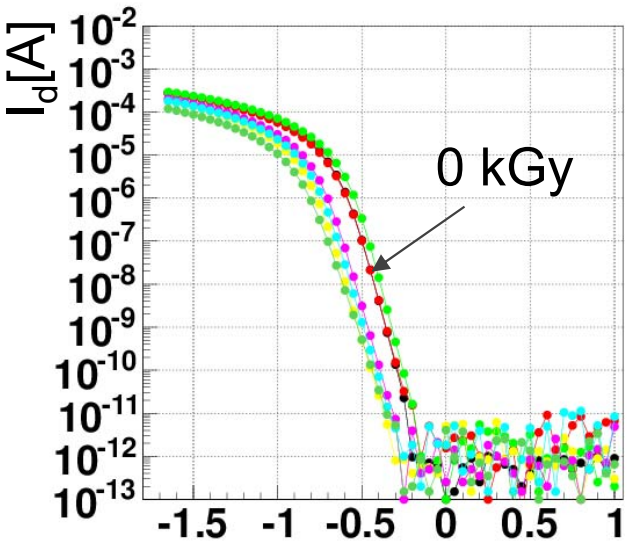
PMOS

I/O Normal Vt
Source-Tie
L/W =0.35um/5um

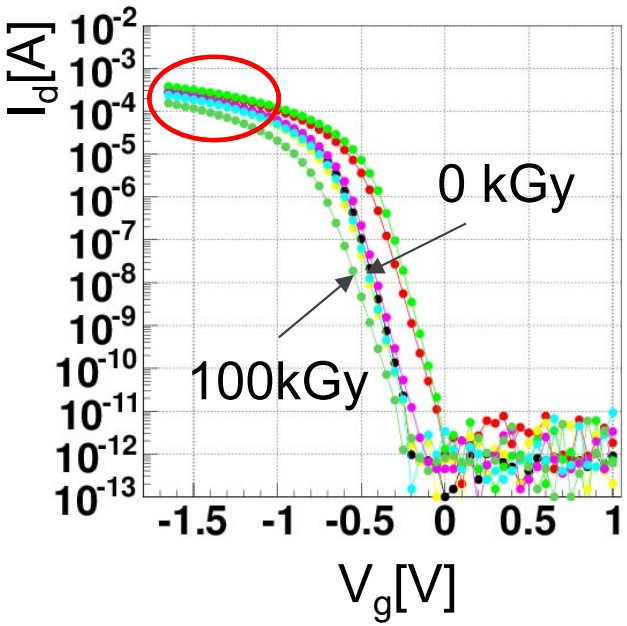
V_{SOI2}=0V

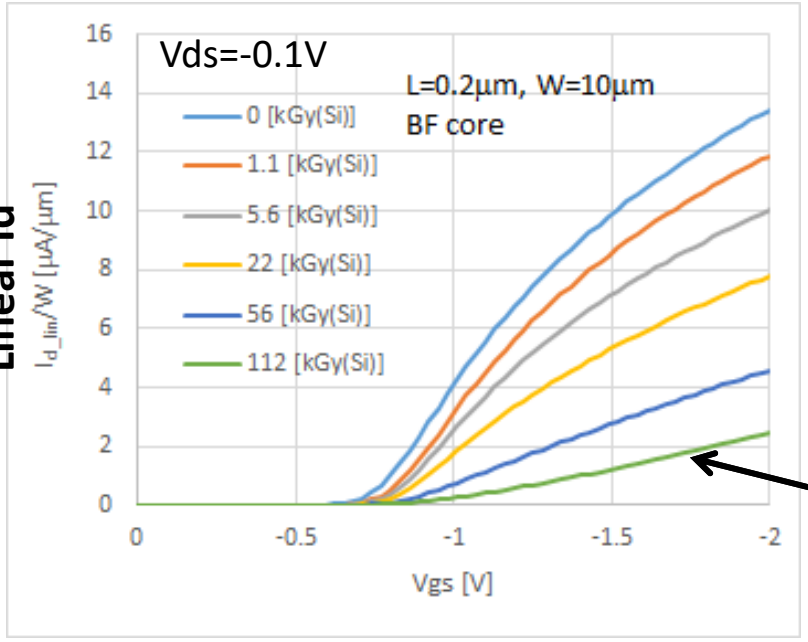


V_{SOI2}=-2V



V_{SOI2}=-5V





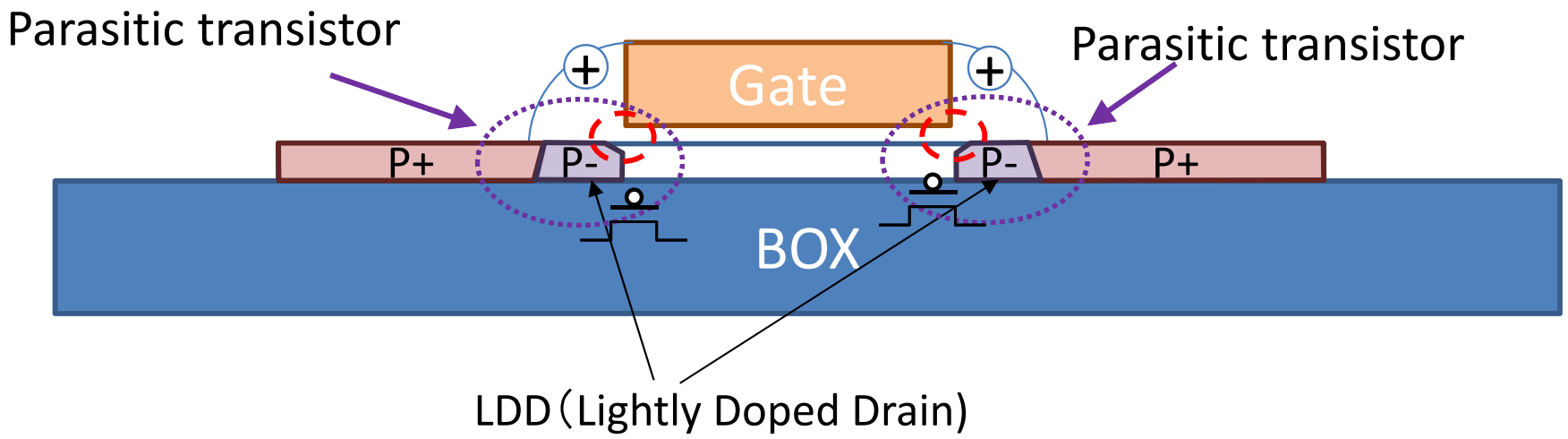
-80%

112kGy

Threshold voltage shift is not so large in PMOS, but Drain Current decreases much .

Dose Increase in Lightly Doped Drain (LDD) Region

- Major cause of the drain current degradation by radiation is Vth increase at gate edge due to positive charge generation in spacer.
- Charge in spacer control the Vth of the parasitic transistor.
- To reduce this effect, lightly doped drain (LDD) dose should be increased.
- Present process has rather low dose in LDD region to aiming lower power.

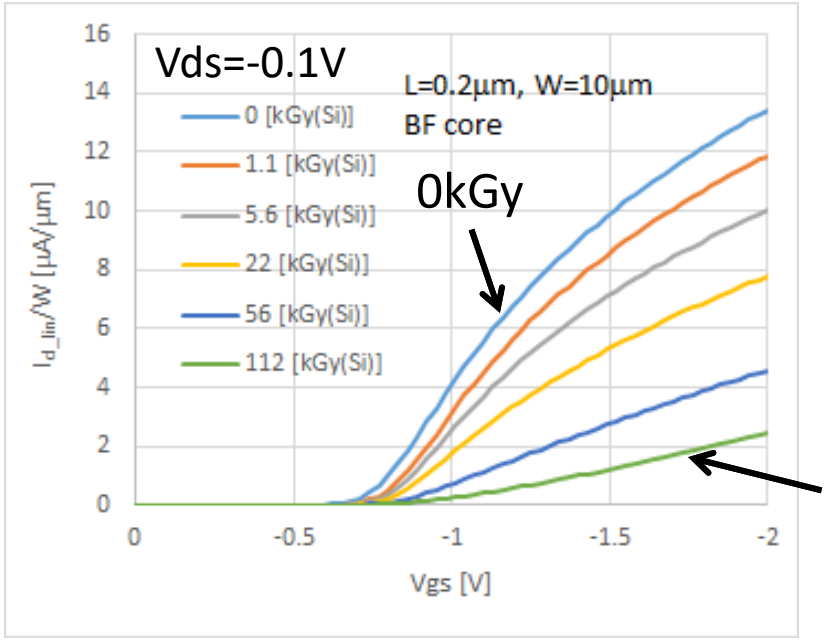


(by I. Kurachi)

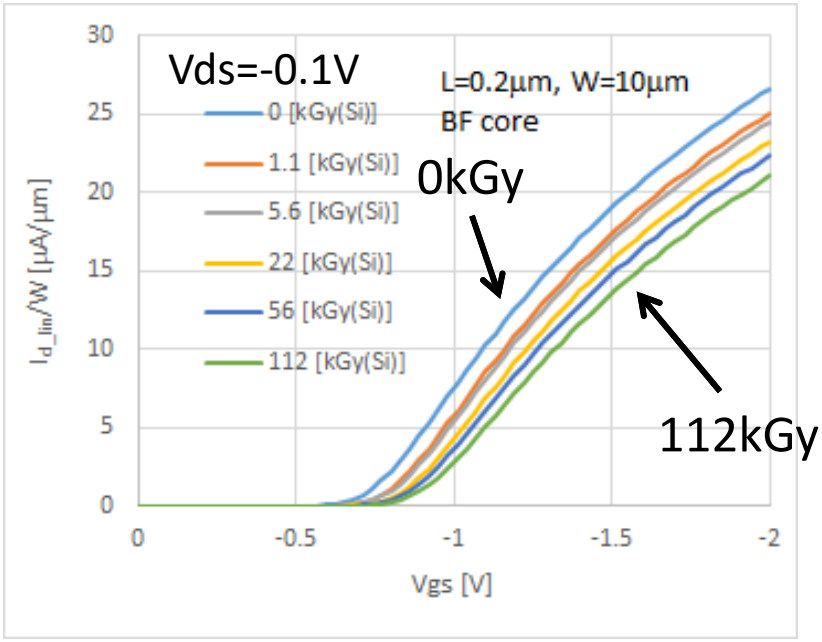
Id-Vg Characteristics in Triode Region

Linear Id

Previous Process



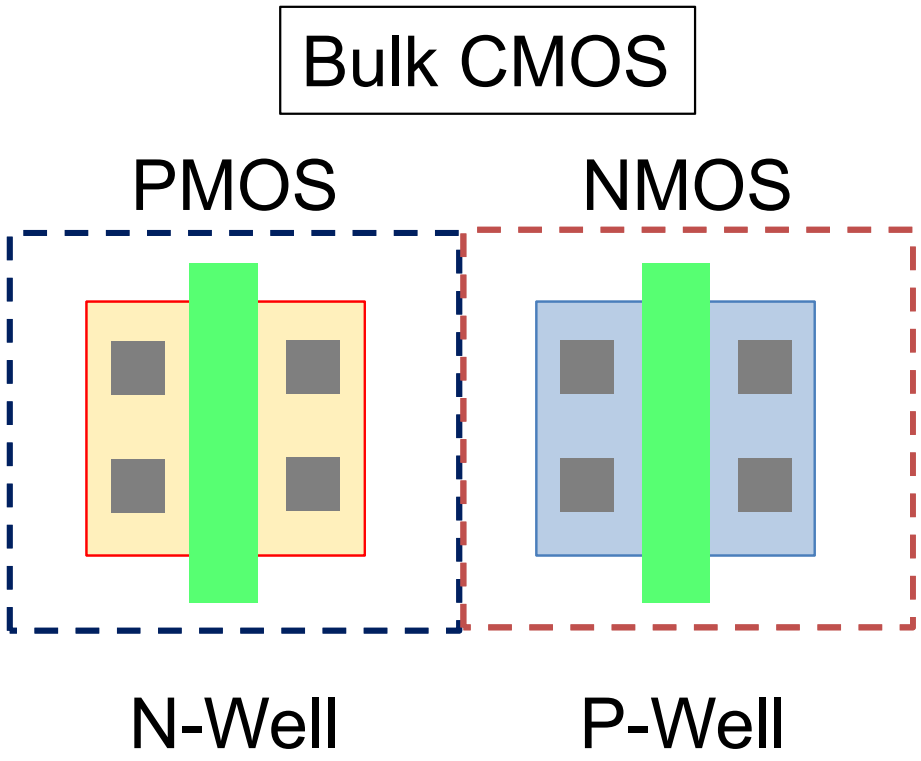
LDD Dose x 6

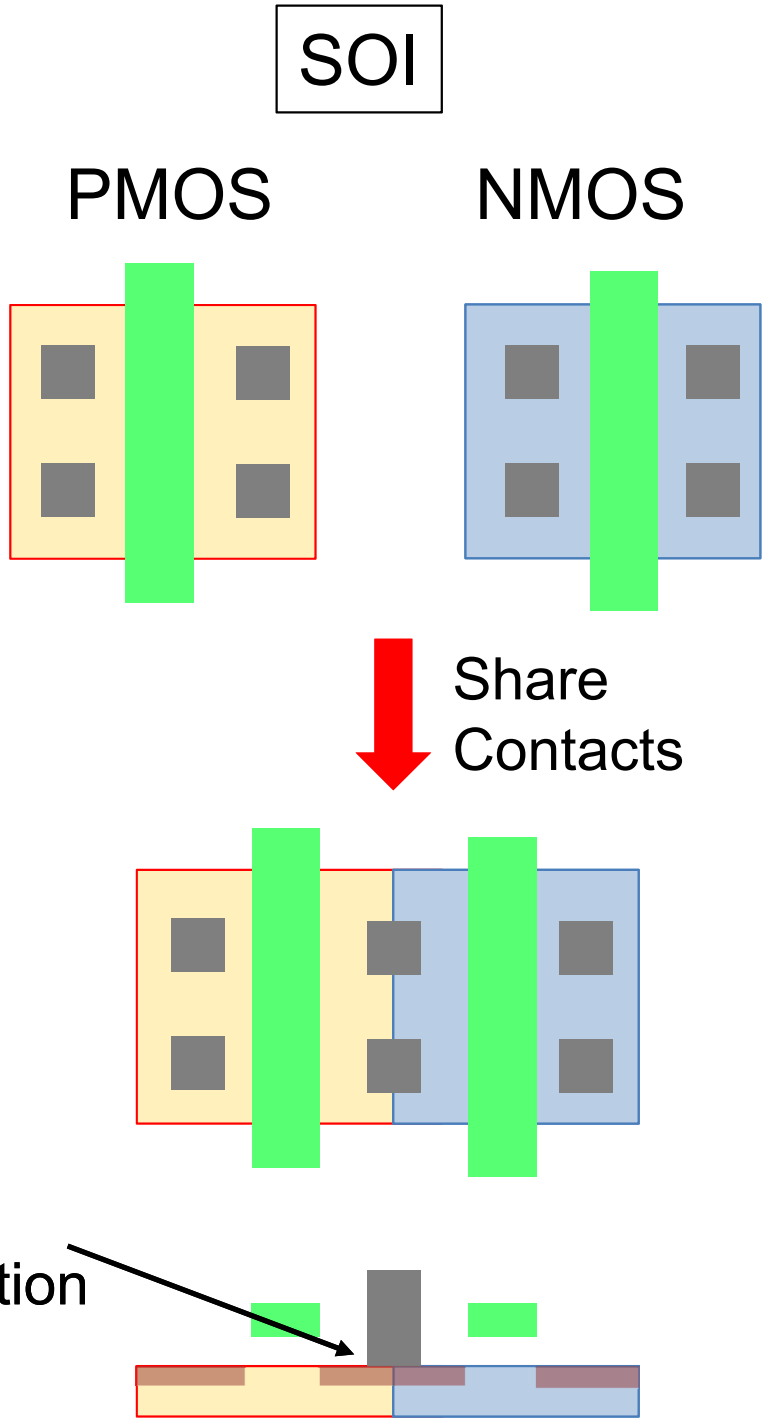


With increasing Implantation dose of PLDD region 6 times higher than present value, the degradation is reduced from 80% to 20% at 112 kGy(Si).

Ref.) I. Kurachi, et al. "Analysis of Effective Gate Length Modulation by X-Ray Irradiation for Fully Depleted SOI p-MOSFETs, IEEE Trans. on Elec. Dev. Vol. 62, Aug. 2015, pp. 2371-2376.

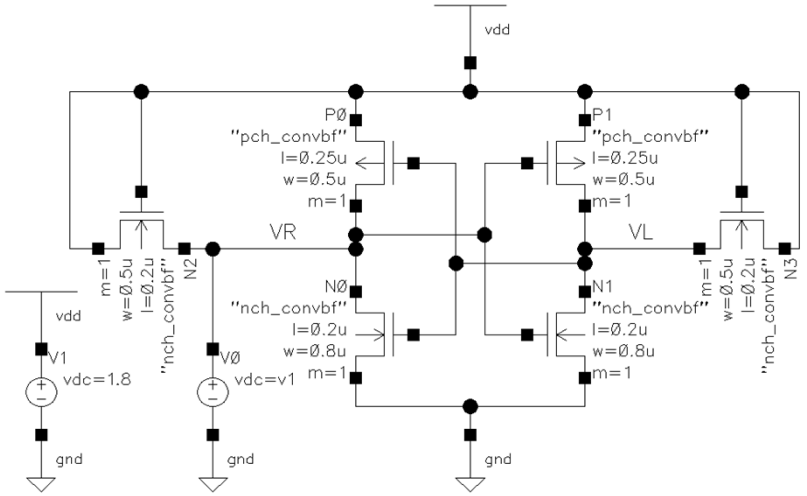
Layout Shrink（Active Merge)

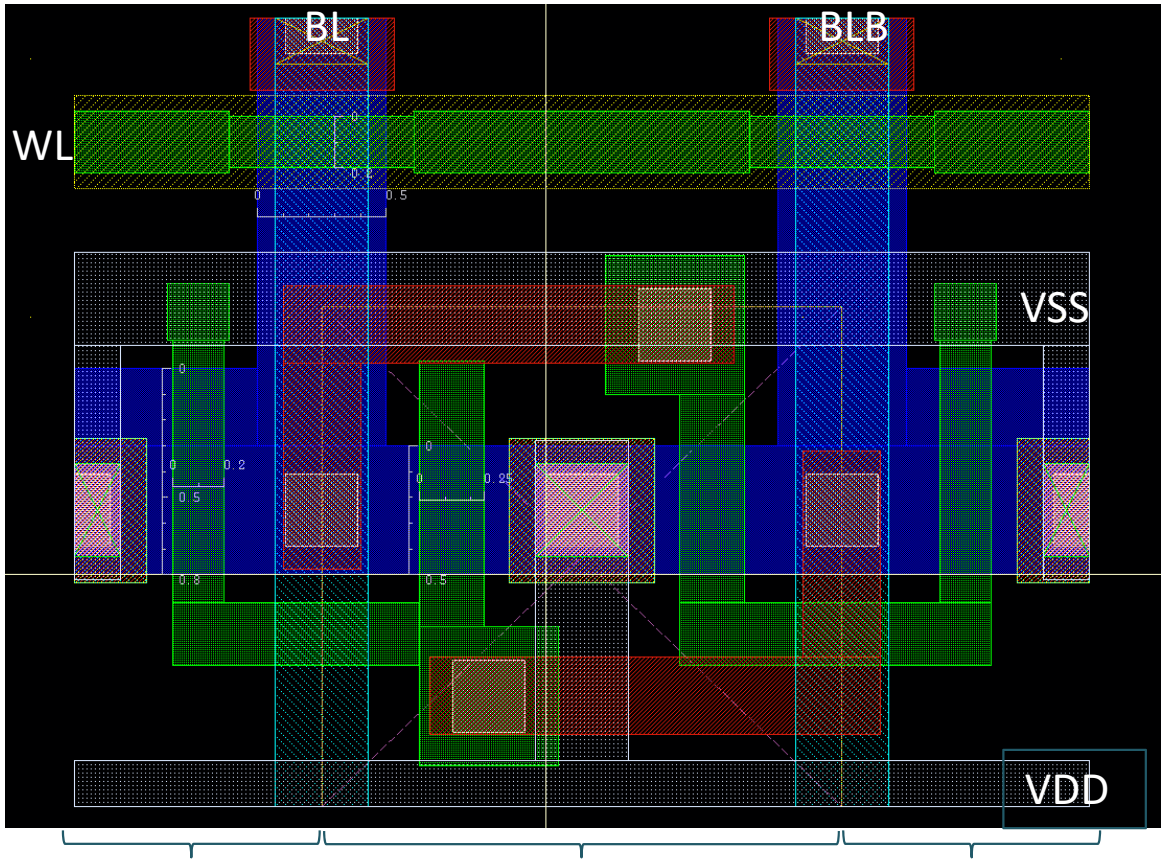




In the SOI process, it is possible to merge NMOS & PMOS Active region and share contacts.

Single Port SRAM Bit Cell





Only 1 Active region

Nch Pch Nch

Cell Size : 3.94µm X 3.06µm = 12.06µm²

III. Detector Examples

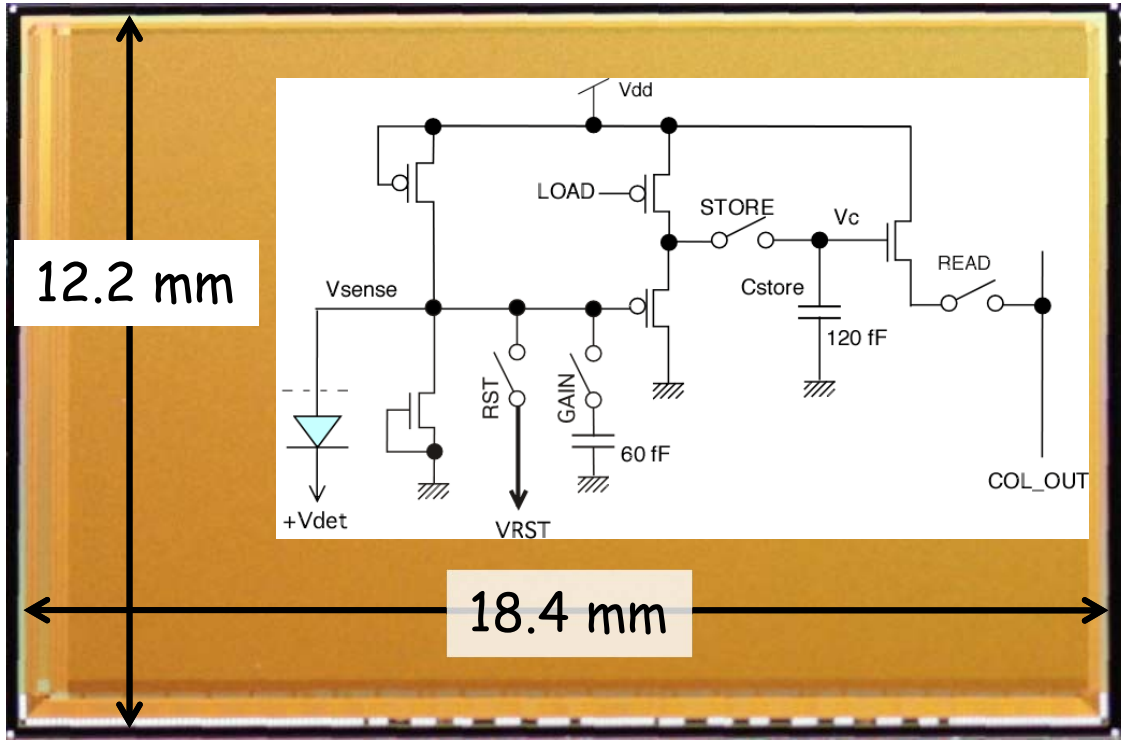
On-Going SOI Projects

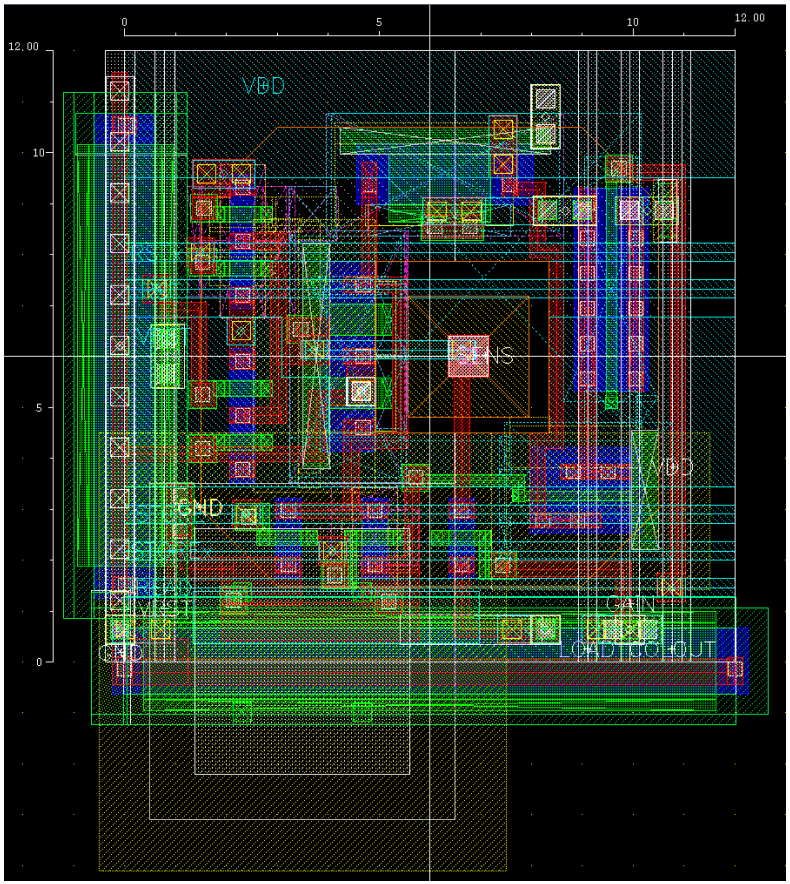
- INTPIX : Genera Purpose Integration Type
  → KEK、Tsukuba.
- SOPHIAS : Large Dynamic Range Large Area for XFEL, SR → Riken
- XRPIX : X-ray Astronomy in Satellite
  → Kyoto, Miyazaki, Shizuoka,,,,
- SOFIST : Linear Collider Vertex Detector
  → KEK, Tsukuba, Osaka, Tohoku,,, (China, Poland)
- CNPIX : General Purpose Counting Type → KEK, China
- STJPIX : Superconducting Tunnel Junction on SOI
  → Tsukuba, AIST.
- MALPIX : TOF Imaging Mass Spectrometer
  → KEK, Osaka.
- 30...

and Many Other Project are being planned

Integration Type Pixel (INTPIX)

Pixel Size : 12x12 μm²
896x1408 (~1.3 M) pixels、
11 Analog out port、Column CDS.

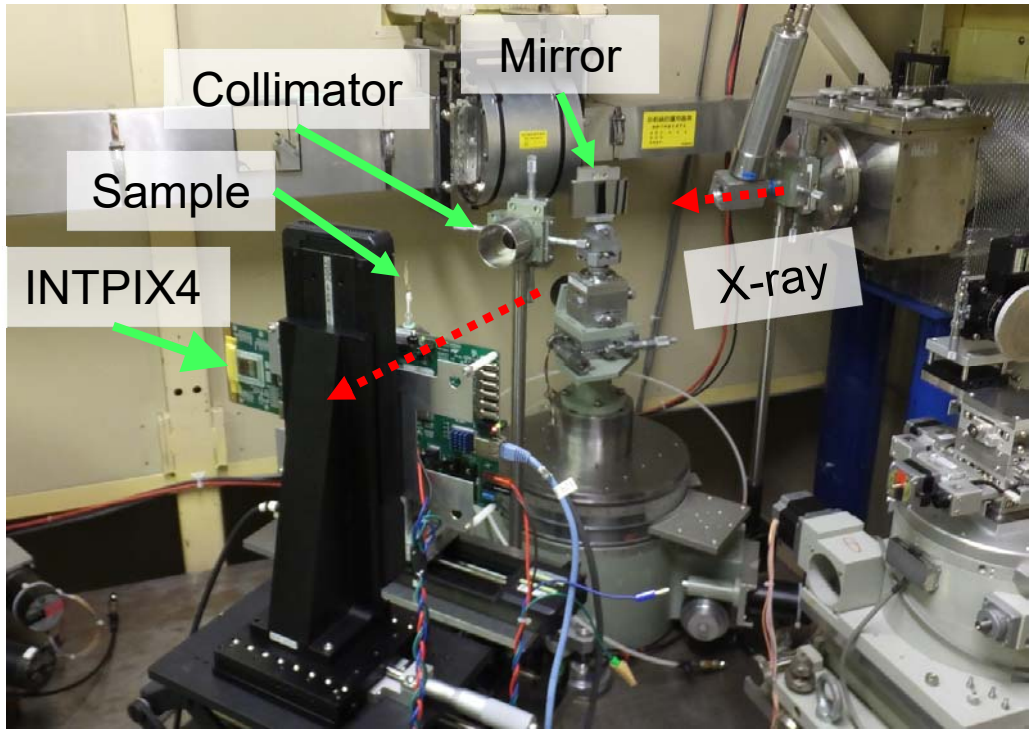


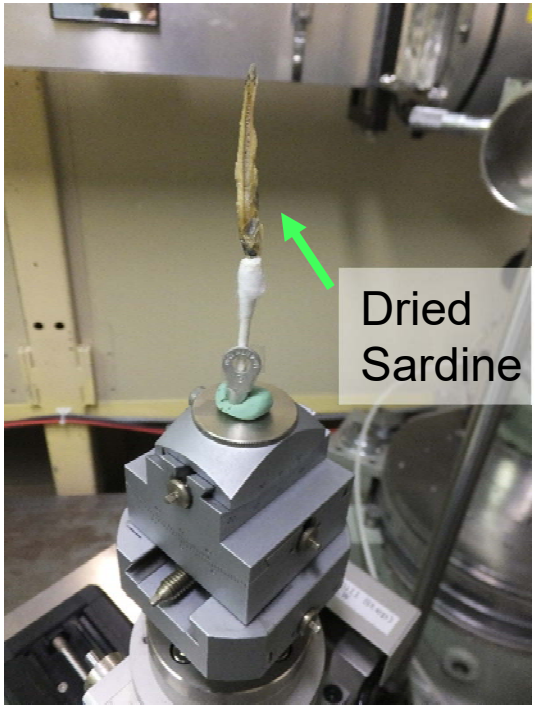


INTPIX5

3D CT Imaging at KEK PF

INTPIX





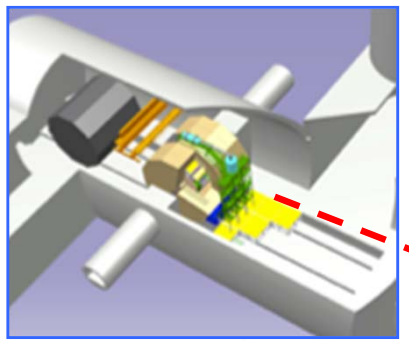
- Sensor : INTPIX4 FZn, Backside Illumination
- HV : 200V、Integration Time : 1ms、ScanTime : 320ns/pix, 1000frame/event
- KEK PF, X-ray Energy : 9.5keV
- Took images for 0~180° at every 1 degree.

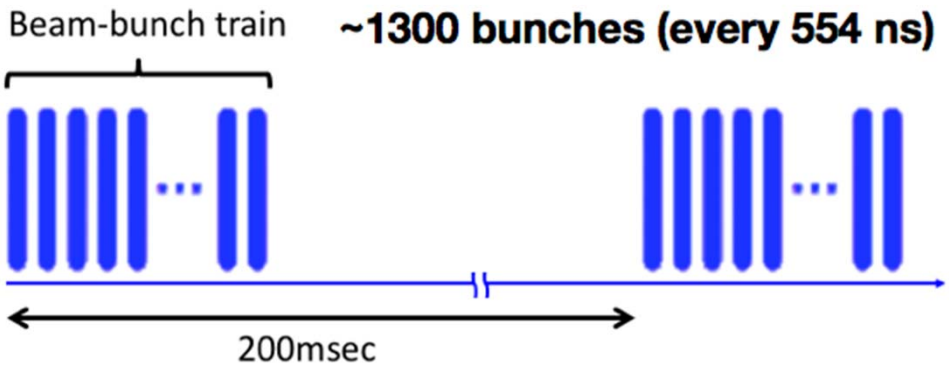
(by R. Nishimura, K. Hirano (KEK)

INTPIX4: Computed Tomography with Syncrotron X-ray

(by R. Nishimura, K. Hirano (KEK)

ILC Acc. Design Overview (in TDR)

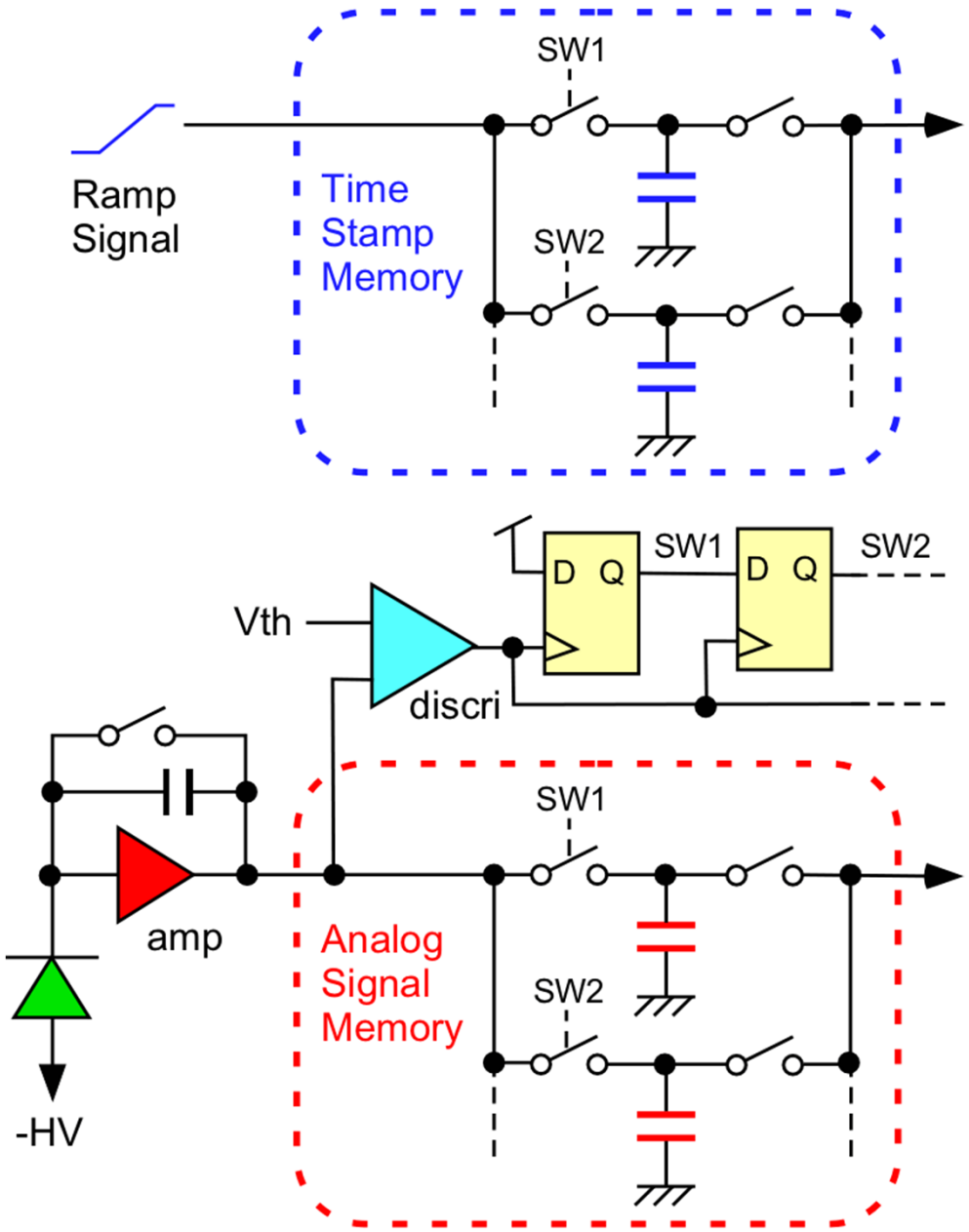




Item	Parameters
C.M. Energy	500 GeV
Length	31 km
Luminosity	1.8 x10^{34} $cm^{-2}s^{-1}$
Repetition	5 Hz
Beam Pulse Period	0.73 ms
Beam Current	5.8 mA (in pulse)
Beam size (y) at FF	**5.9** nm
SRF Cavity G. Q_0	**31.5** MV/m Q_0 = 1x10^{10}

ILC Vertex Detector R&D : SOFIST

(SOI sensor for Fine measurement of Space & Time)

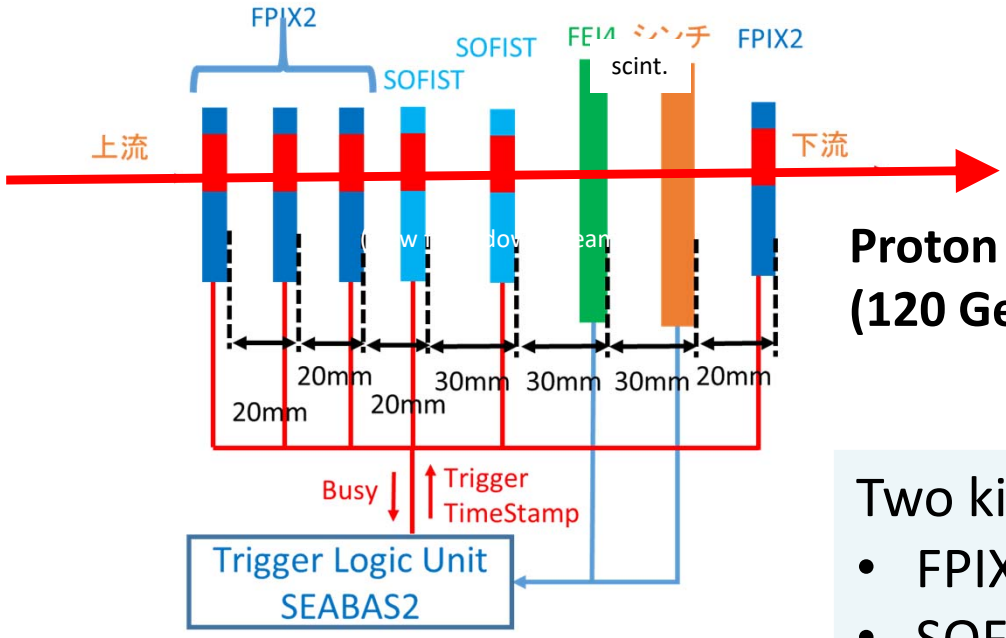


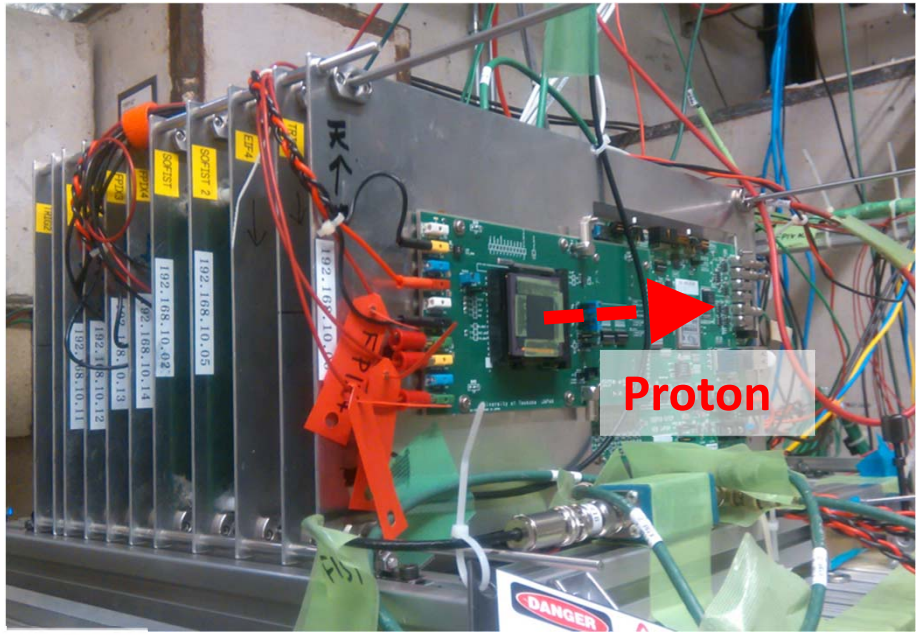
Test Chip Spec.

- Chip size: 2.9 × 2.9 mm2
- Substrate (FZ n-type, 2 kΩ•cm)
- Pixel size: 20~25 μm
- No. of Pixel: 50 × 50 pixels
- Gain: 32 mV/ke- (@Cf=5fF)
- Analog signal memories: 2 for signal or 2 for time
- Column-ADC: 8 bit
- Zero Suppression Logic

R&D for 3D integration is also progressing.

Tracking Resolution:
High-Energy Beam test @Fermi National Accelerator Lab.



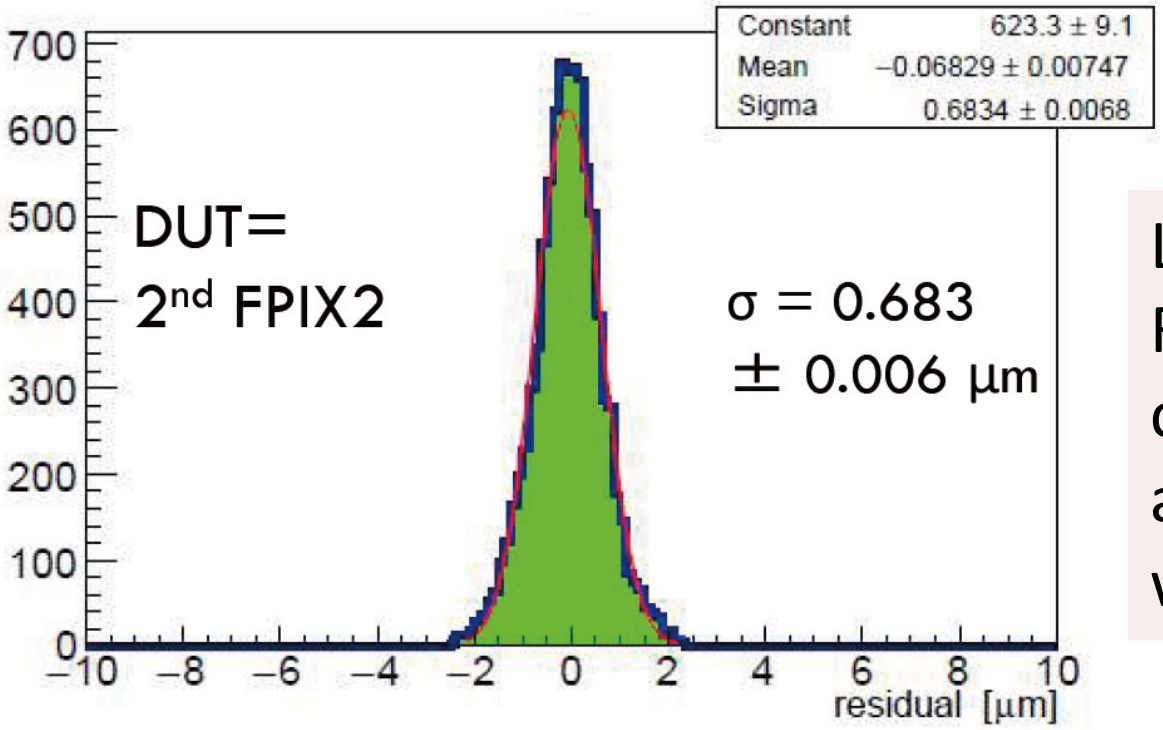


Proton Beam
(120 GeV/c)

Two kinds of SOIPIX-DSOI detectors are used:

- FPIX2 x 4: 8 μm square pixel detector
- SOFIST1 x 2: 20 μm square pixel detector

Tracking Resolution (cont.)

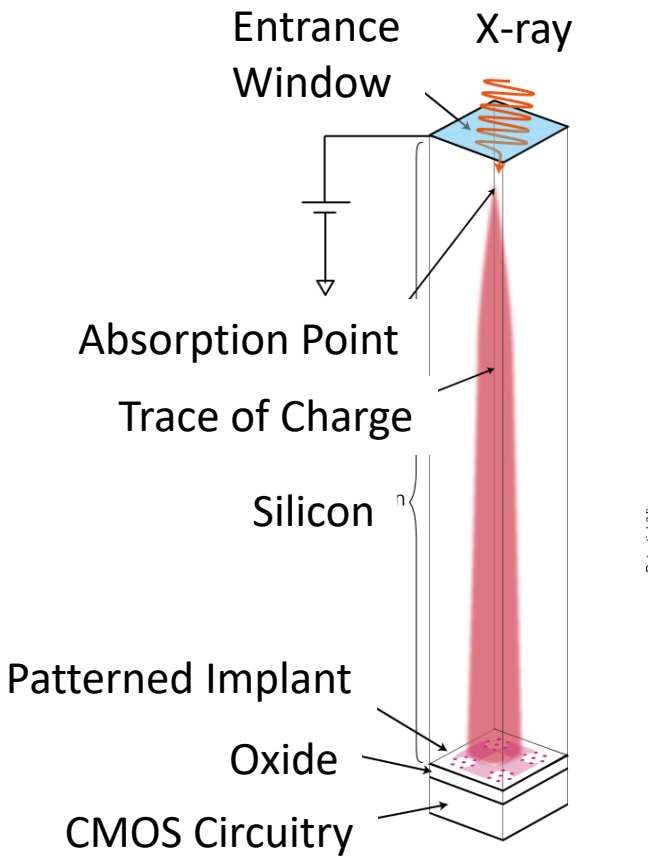


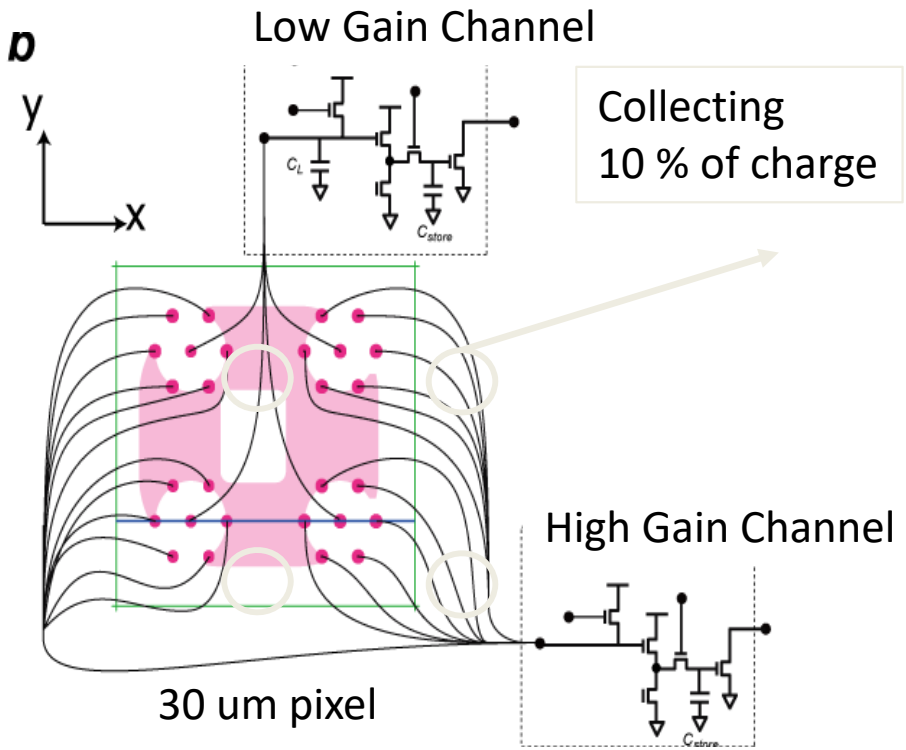
Less than 1 μm Position Resolution for high-energy charged particle is achieved first in the world !

(K. Hara et al., Development of Silicon-on-Insulator Pixel Detectors, Proceedings of Science, to be published)

SOI Photon-Imaging Array Sensor (*SOPHIAS*) *for* X-ray Free Electron Laser (XFEL) SACLA

SOPHIAS

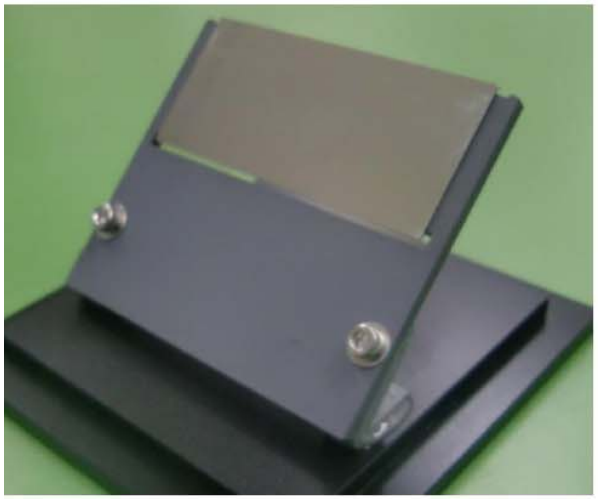




0.25 μW/pixel without power pulsing

SOPHIAS (2007-2018)

T. Kudo, N. Teranishi, K. Ozaki, collab. with KEK, Lapis Semiconductor, Kyocera etc.



Imaging Area:
64.77 x 26.73 mm^2
Largest in class

SOPHIAS

Major Specifications

Pixel Number: 1.9 M
Pixel: 30 μm□
Rad. Hardness: 1 GGy @ 7 keV
Frame Rate: 60 Hz
Noise: 180 e-rms (0.1 phs.@6 keV)
Peak Signal: 18.7 Me- (11400 phs.@ 6 keV)

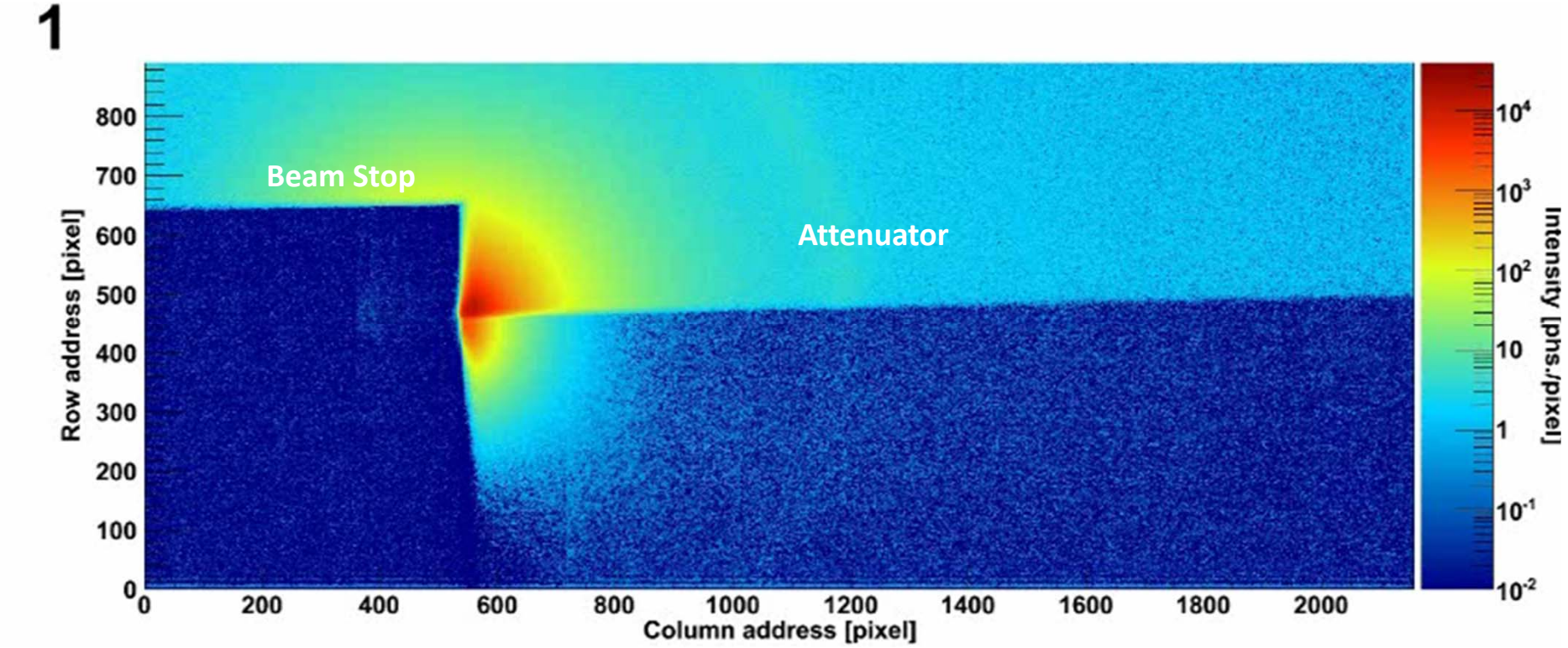
Peak Signal Density: 12.7 phs./1 μm□@ 6 keV
Highest among XFEL detectors
cf) 3.7 phs/1 μm□ (Jungfrau, PSI)

Status

Development completed.
Yield improvement ongoing.
Sensor Production to be Completed in FY2018.

Wide Dynamic Range: SOPHIAS

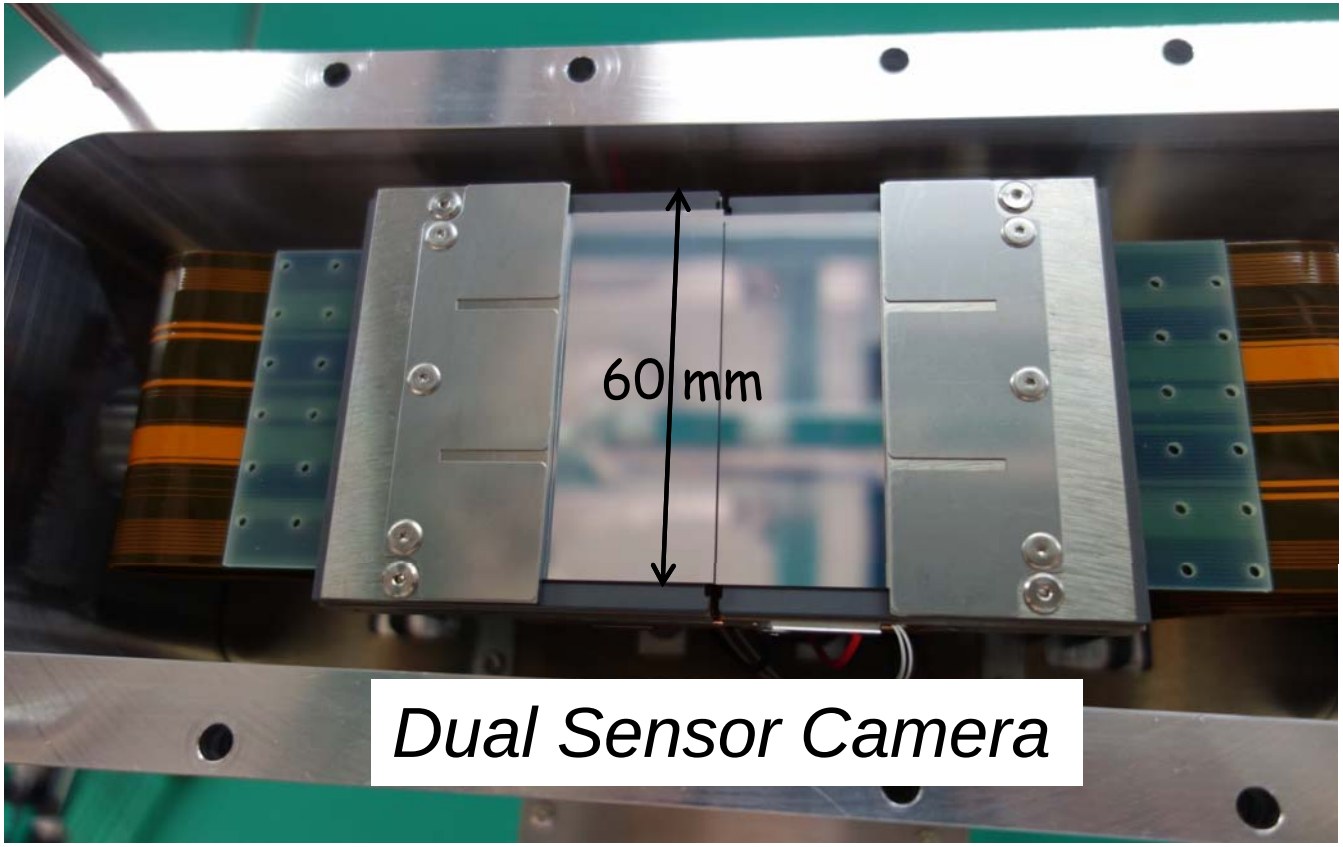
SACLA BL3 6keV (1.5×10^{11}phtons/pls)
CoO: dia. 22 nm; t=1mm
Sensor is operated at the 60 Hz frame/second mode
Dynamic Range: 1 ~ 10,000 6keV photon/pix (~ 18.7M e-/pix)



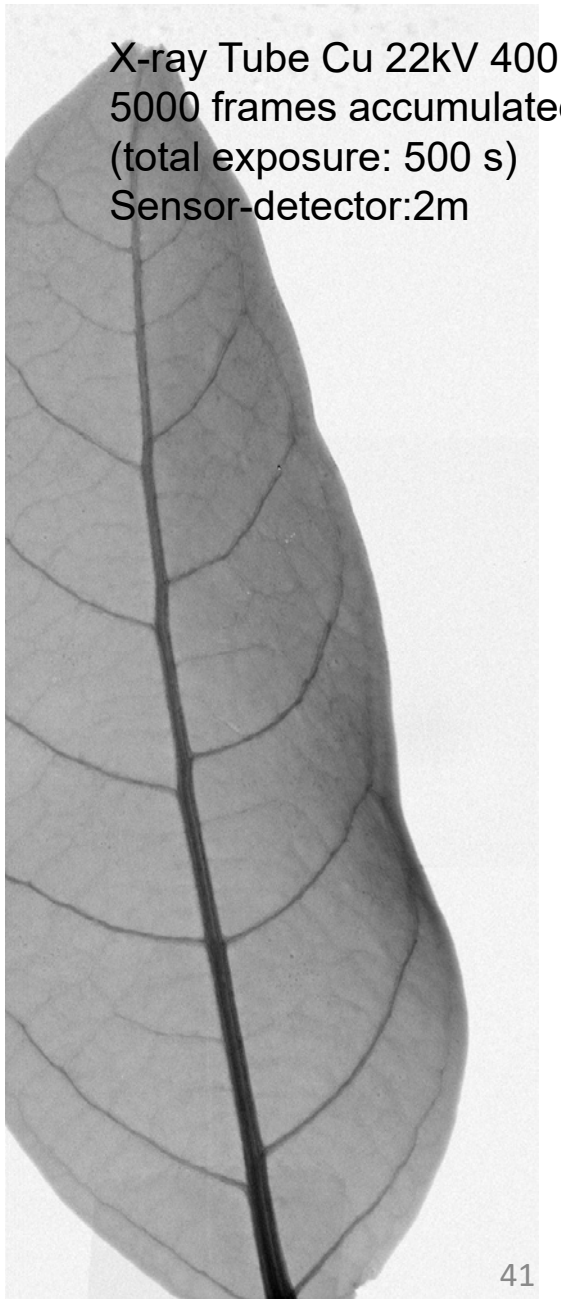
SOI Photon-Imaging Array Sensor (*SOPHIAS*) *for* X-ray Free Electron Laser (XFEL) SACLA

Utilization of SOPHIAS has been started for various experiments in SACLA@RIKEN.

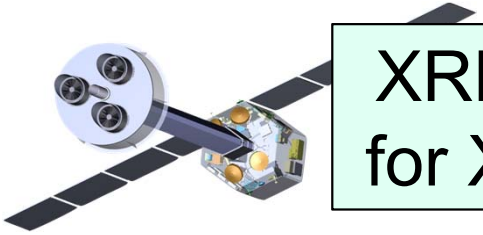
- Dynamics of Atomic Structure
- Direct Observation of Chemical Reactions
- etc.



Dual Sensor Camera

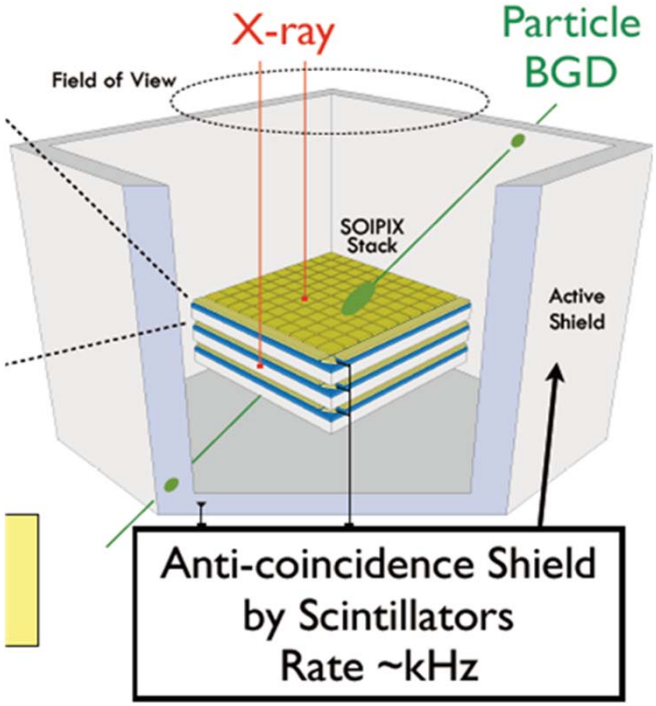


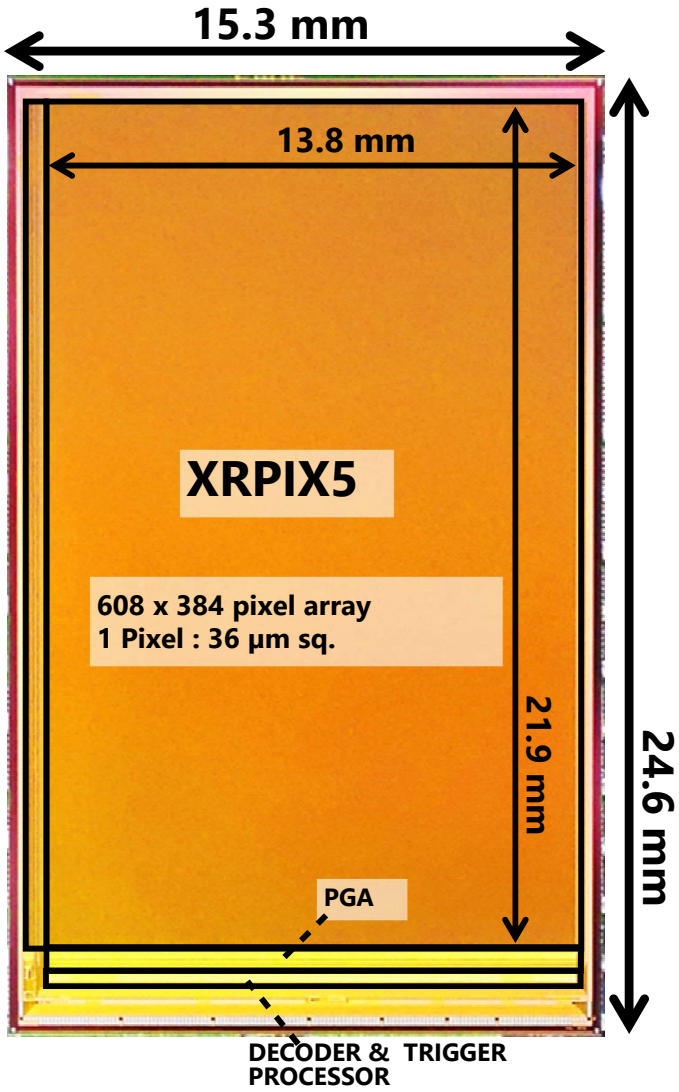
X-ray Tube Cu 22kV 400uA
5000 frames accumulated
(total exposure: 500 s)
Sensor-detector:2m



XRPIX: Event-Driven Detector for X-ray Astronomical Satellite

Timing resolution of CCD is too poor to make anti-coincidence.

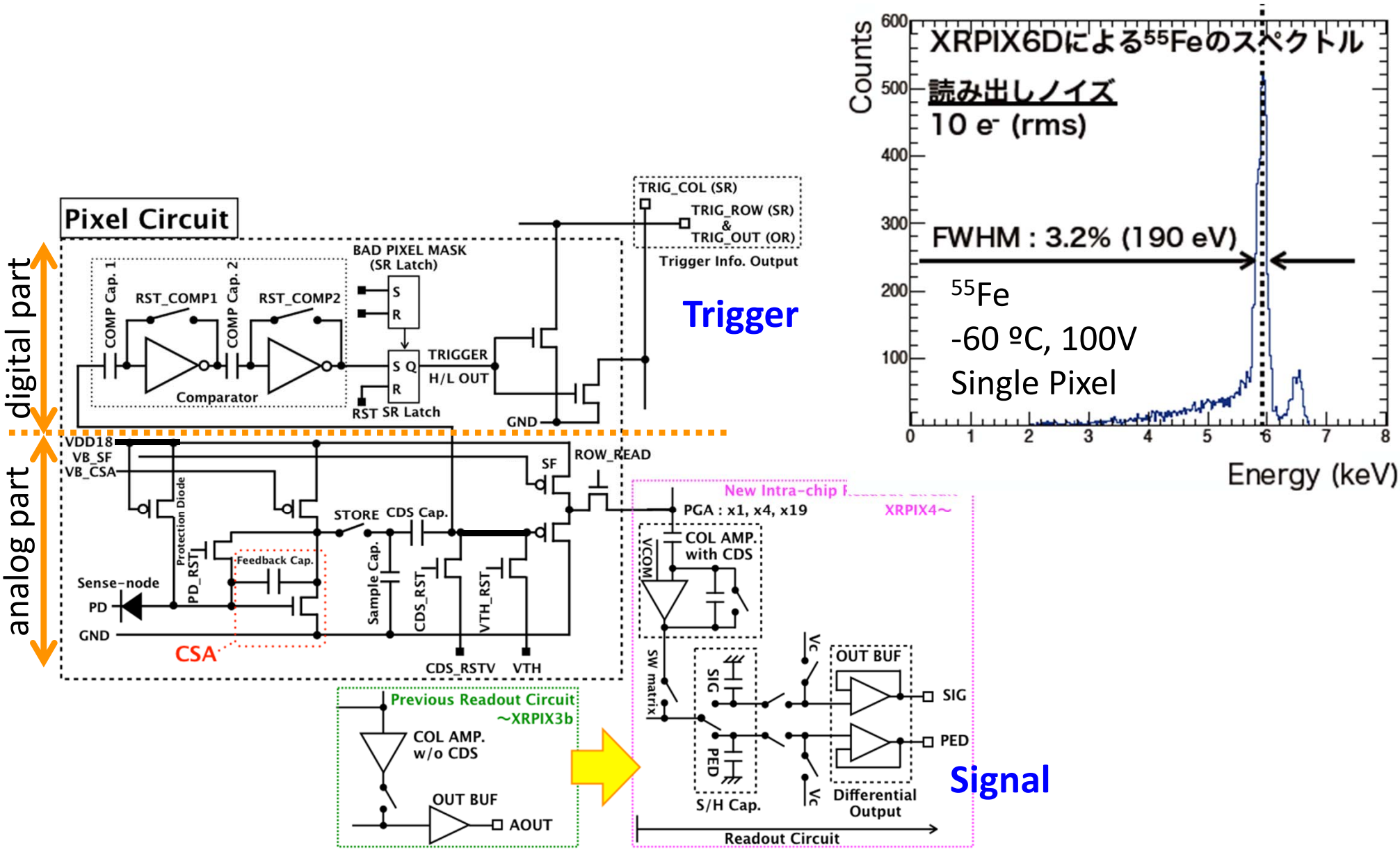




Aiming to install in the next satellite FORCE (Forcusing On Relativistic universe and Cosmic Evolution)

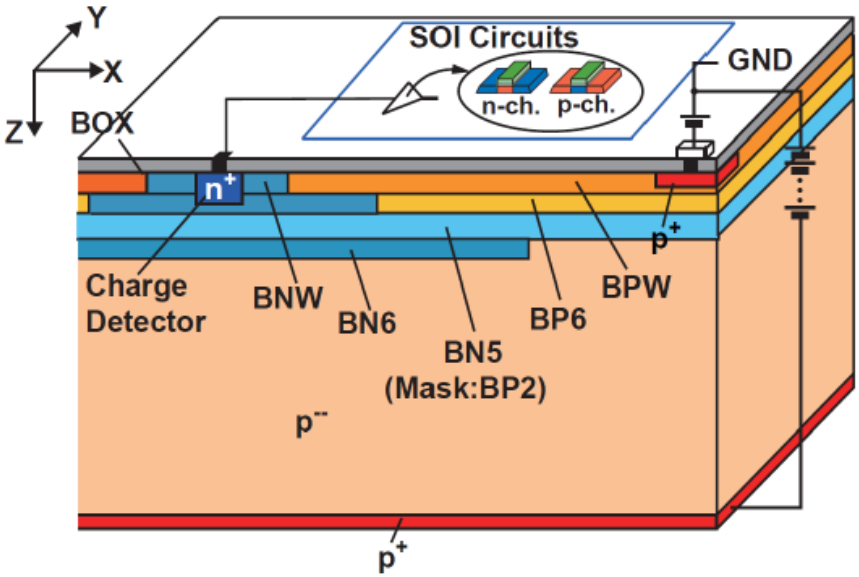
(Kyoto U. etc.)

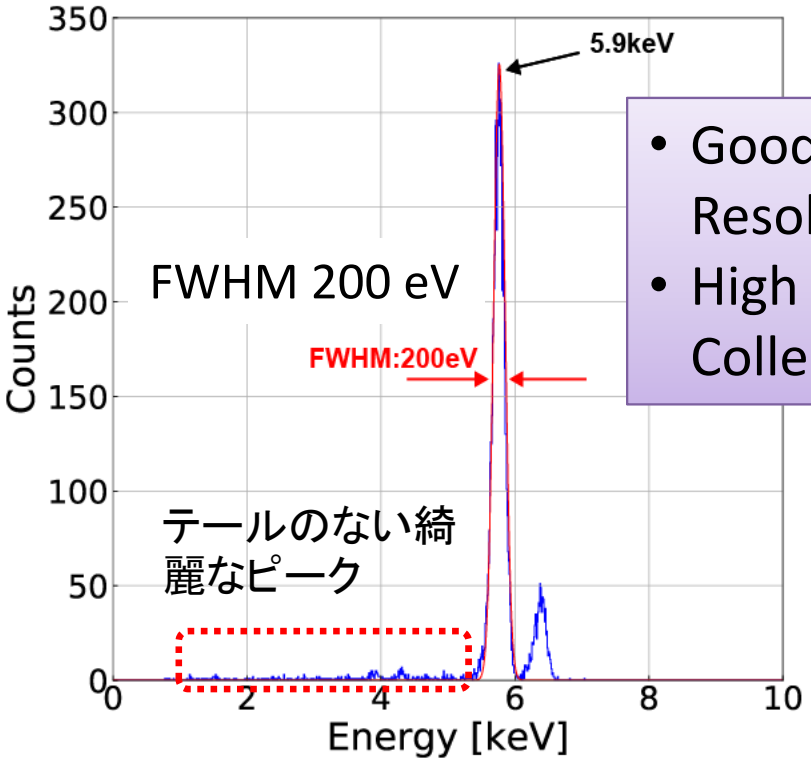
XRPIX5: Event Driven X-ray Astronomy Detector



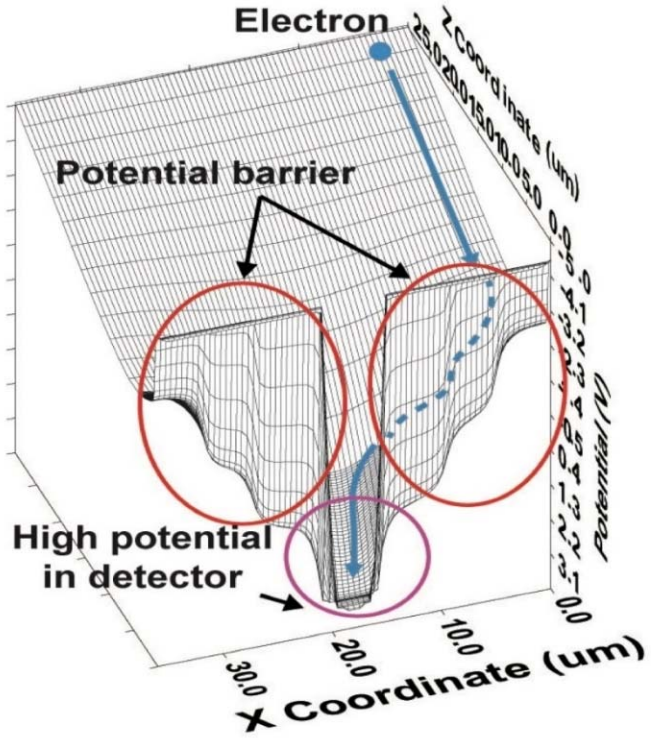
New Sensor Structure: Pinned Depleted Diode (SOIPIX-PDD)

Gain = 70 μV/e-
Noise = 11.0 e-
Dark Current = 57 pA/cm2 @-35˚C





- Good Energy Resolution
- High Charge Collection Efficiency

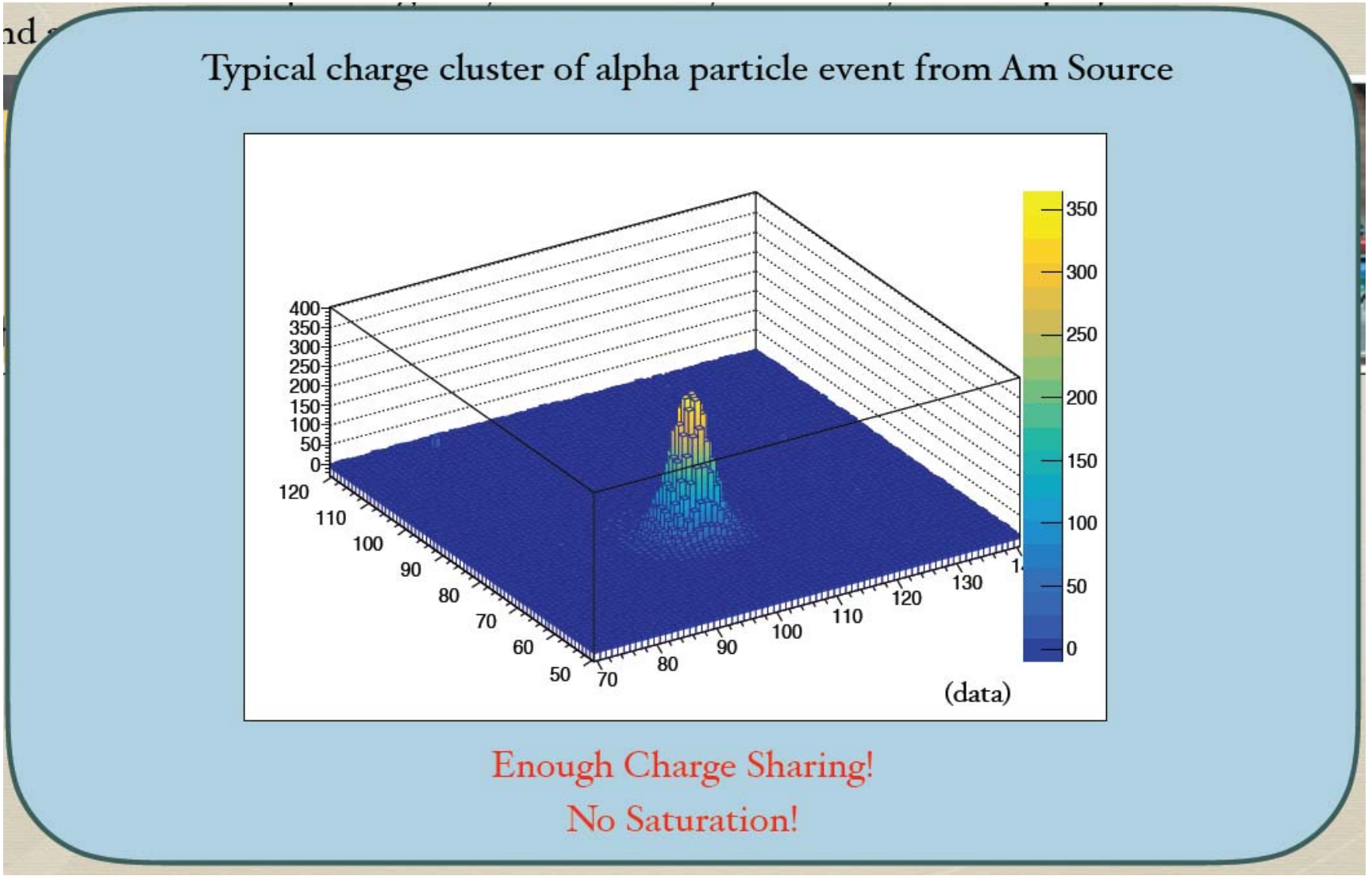


(静岡大　川人研)

Neutron Detection (Boron Converter)

Micron resolution!

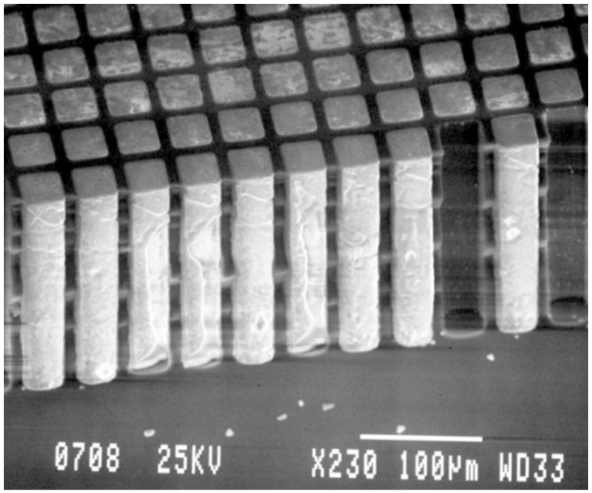
$^{10}B + n \rightarrow {}^{7}Li + {}^{4}He + 2.31\ MeV + \gamma(0.48\ MeV)$

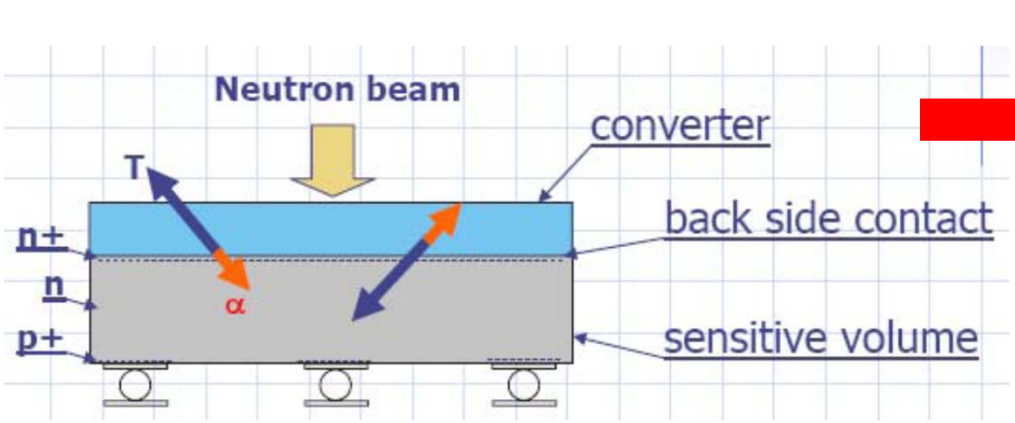


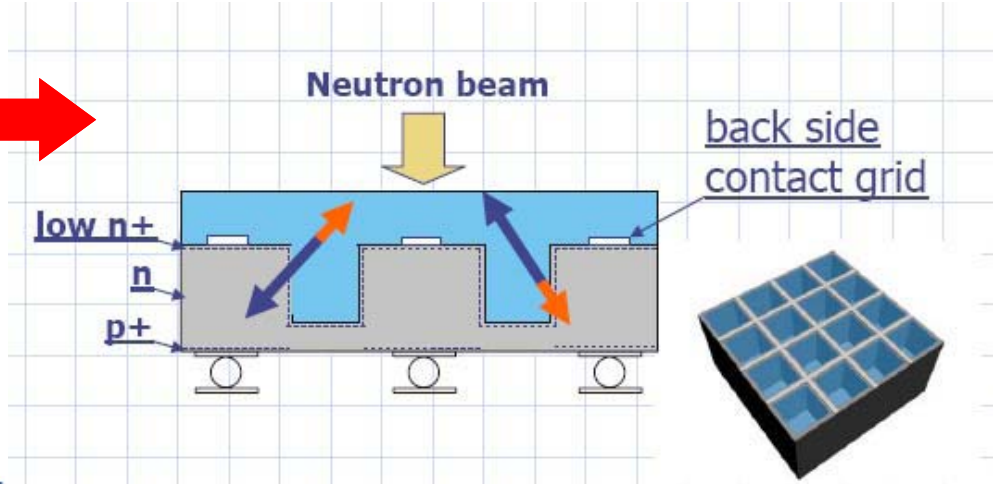
櫻井(物質材料機構)、神谷 (東大理)、

Toward Higher Detection Efficiency

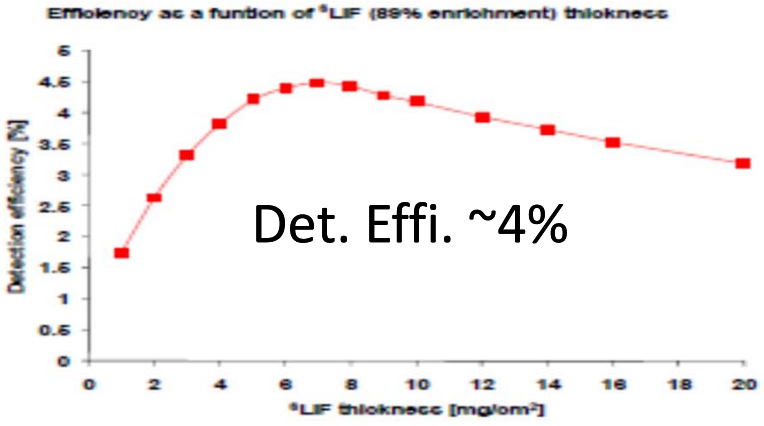
$^{6}Li + n \rightarrow {}^{4}He + {}^{3}H + 4.79\ MeV$





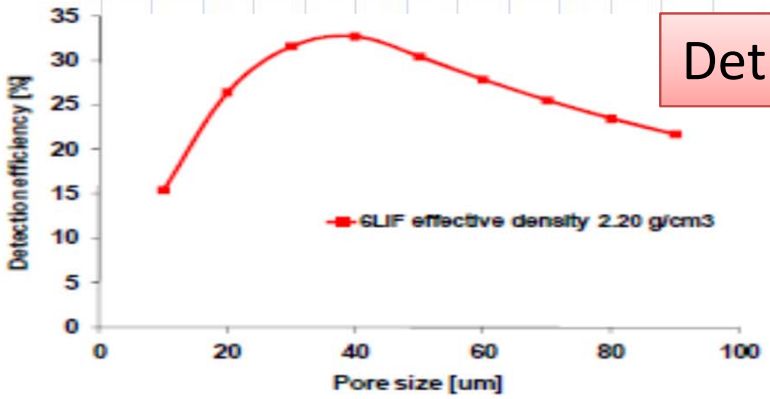


Det. Effi. >30%



Det. Effi. ~4%

a)



b)

Christer Fröjdh, Vertex2016,
https://indico.cern.ch/event/452781/contributions/2297517/attachments/1344468/2026375/VERTEX2016.pptx

IV. Summary

- SOI pixel technology becomes mature. Back-gate and sensor-circuit coupling issues are solved by introducing double SOI wafer.
- Radiation tolerance is improved to more than 100 kGy(Si) by biasing middle Si of the Double SOI.
- NMOS-PMOS active merge reduces layout size very much. This is almost equivalent to go to finer process while keeping analog voltage of 0.2um process (1.8V/3.3V).
- Many kinds of SOI X-ray detectors are developed (or under development) so far.
- Our SOI Pixel process run is open to academic people. Please join the run.

Thank You!