SAMURAI DAQ

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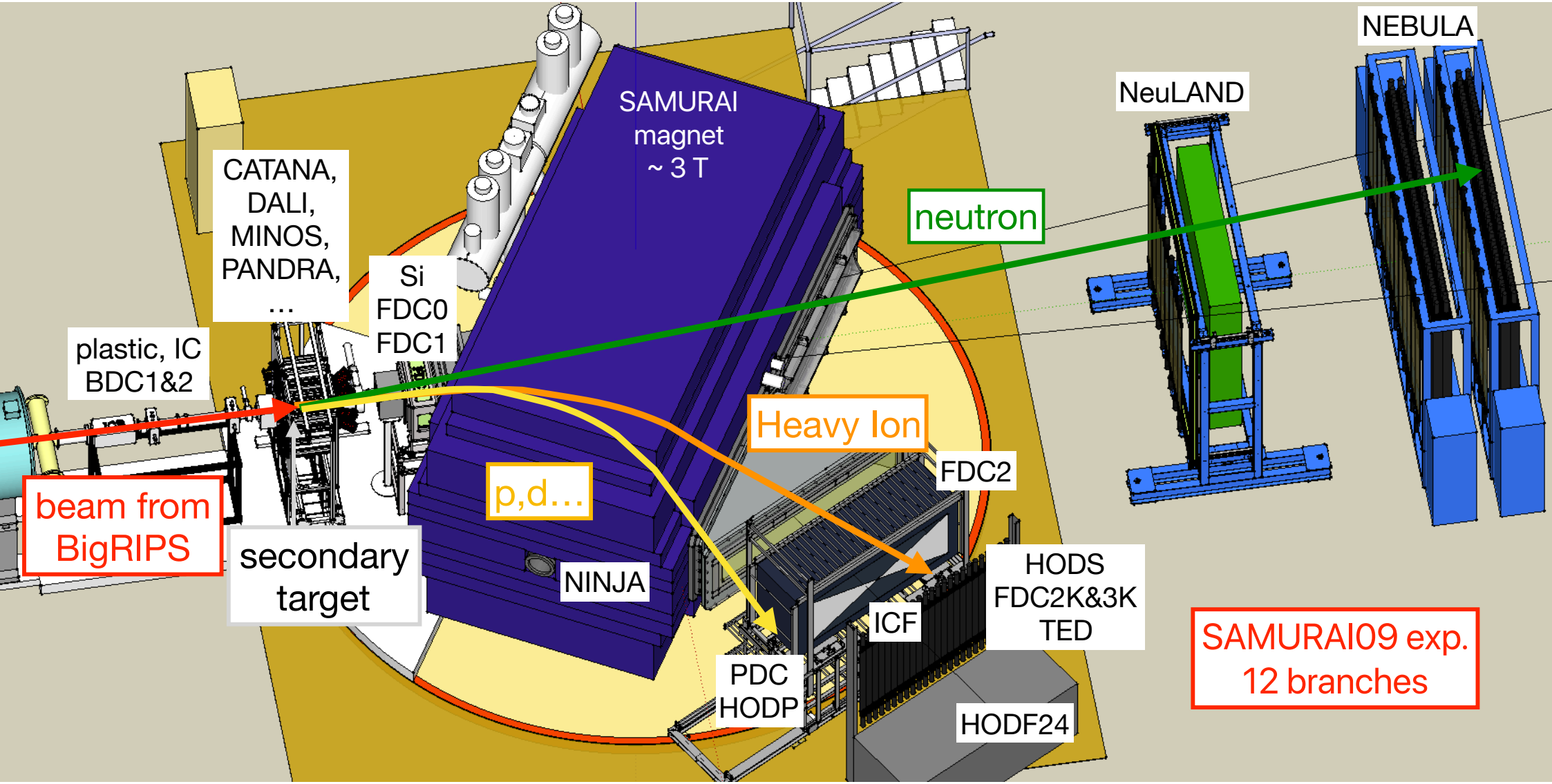
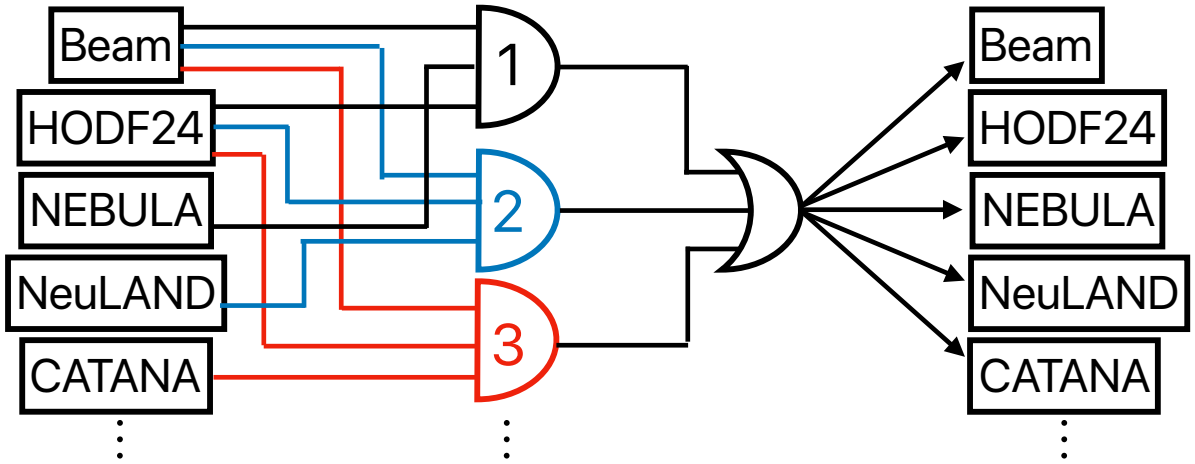
SAMURAI: versatile spectrometer



Common trigger and common dead time

Branch with longest dead-time determine live time.



April 2017

Branch	Dead time[μs]
B3F	230
BDC	150
FDC1	140
FDC2-1	170
FDC2-2	170
HODF24	90
NEBULA-Q	140
NEBULA-T	120
CATANA	50
NeuLAND	80

The B3F branch (scaler, beam-line plastics,...): ~50 μs with DMA transfer now.

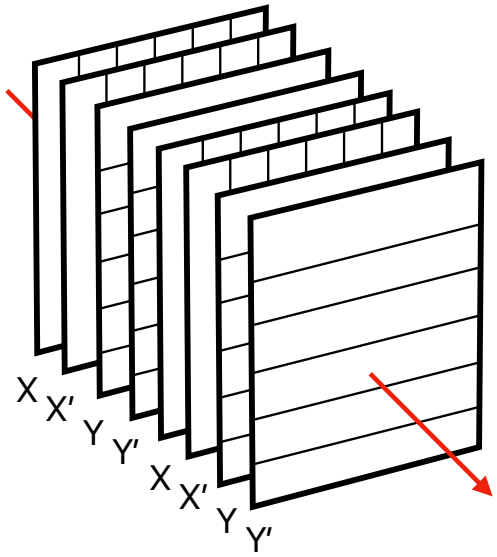
→ Drift chambers!

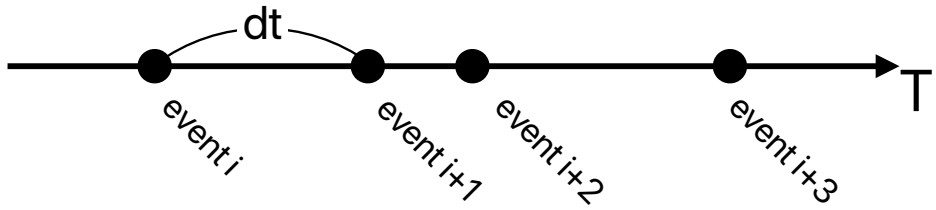
Longer dead-time of drift chambers

Multiple layers: large number of hits from single DC

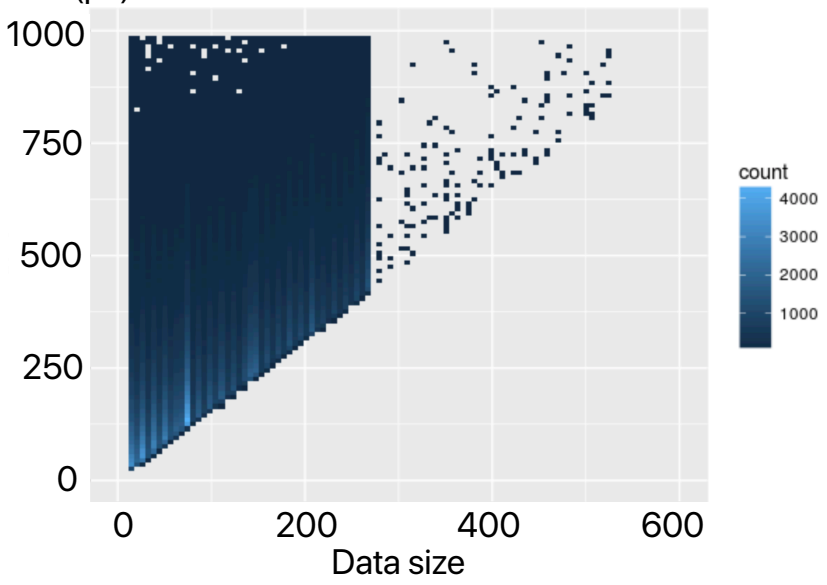
→ modules with shorter dead-time/channel are favorable.

DC (8 or 14 layers)

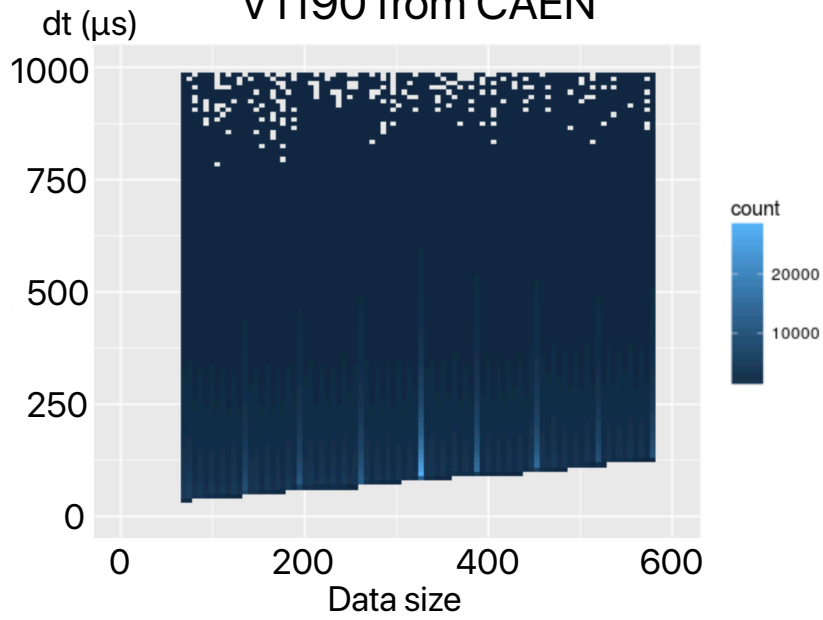




AMT-TDC from AMSC



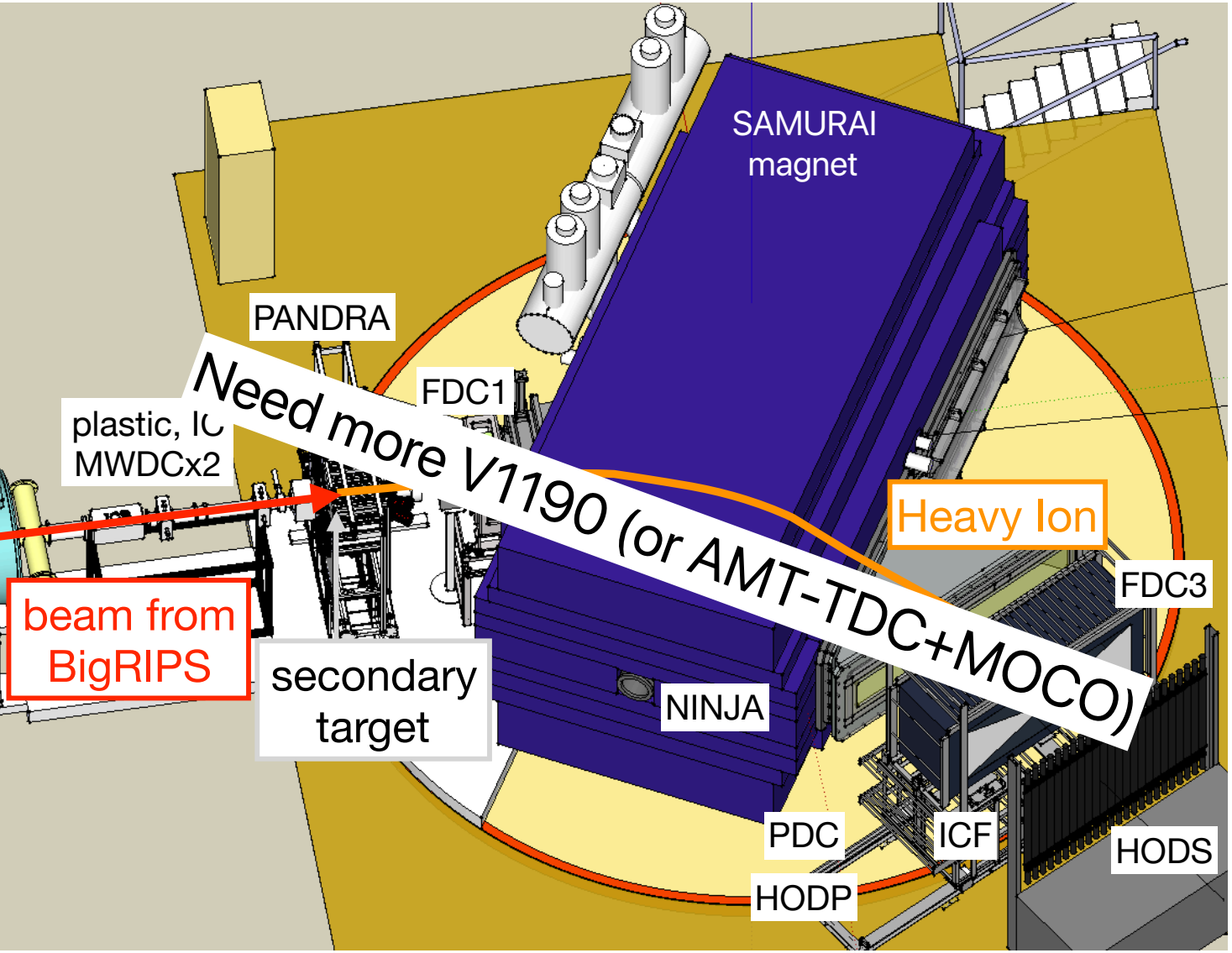
V1190 from CAEN



V1190 has better dead-time/channel

Courtesy of Gao & Sasano

Dead time is much shorter in SAMURAI11



BDC, FDC1, FDC2K&3K
AMT-TDC → V1190

FDC2: 98 ASD cards
→FDC2K & 3K: 16 ASD cards

SAMURAI09 (2017 April)
~230 μs dead time
70% livetime with 1.4kHz request

SAMURAI11 (2019 April)
~50 μs dead time
60% livetime with 10kHz request

network infrastructure, power of event-build PC,
more V1190 with FDC2

Triggers for SAMURAI

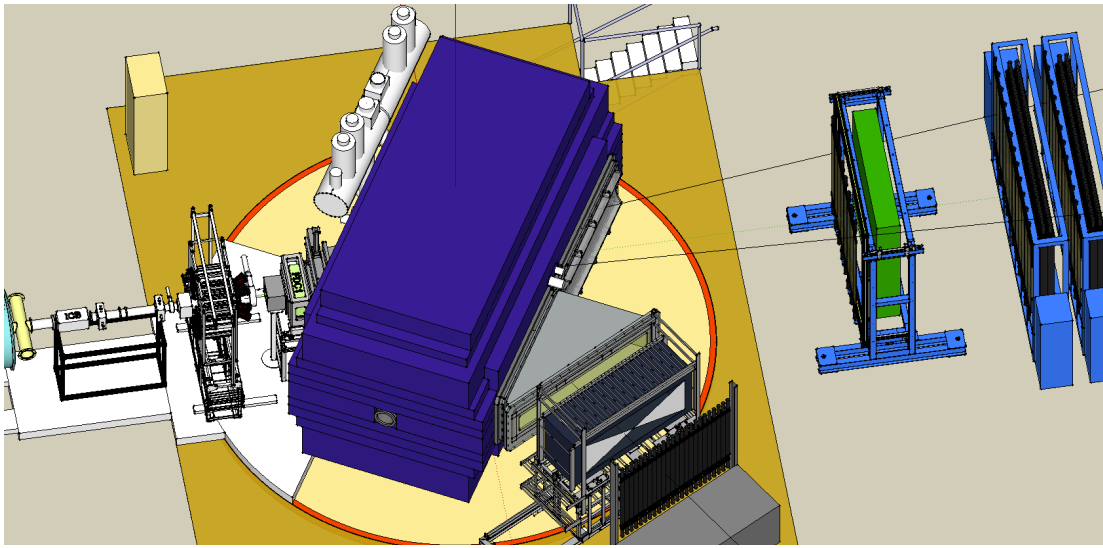
Beam ⊗ HODF ⊗ (NEBULA + NeuLAND)

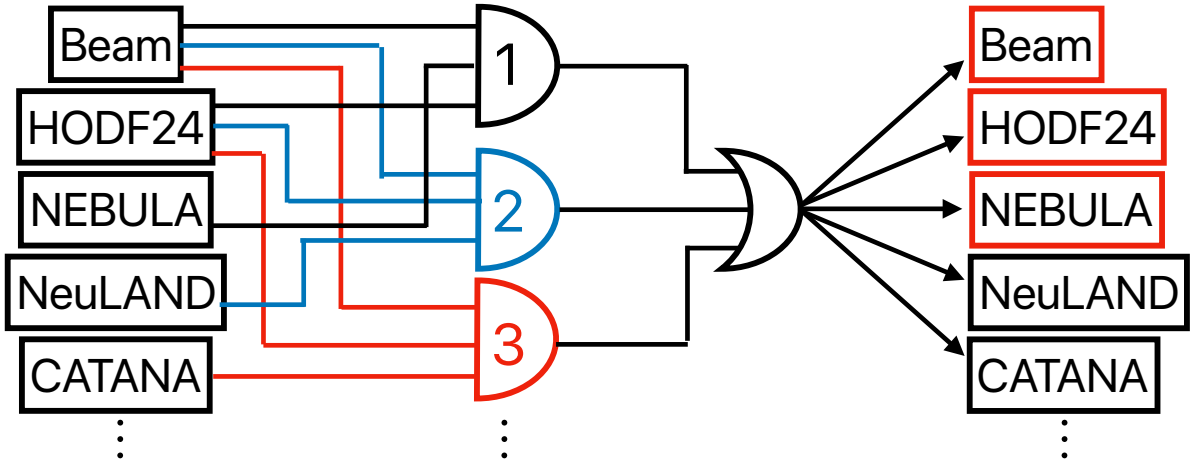
Downscaled beam

Beam ⊗ HODF ⊗ CATANA

Beam ⊗ HODF-left ⊗ HODF-right

⋮

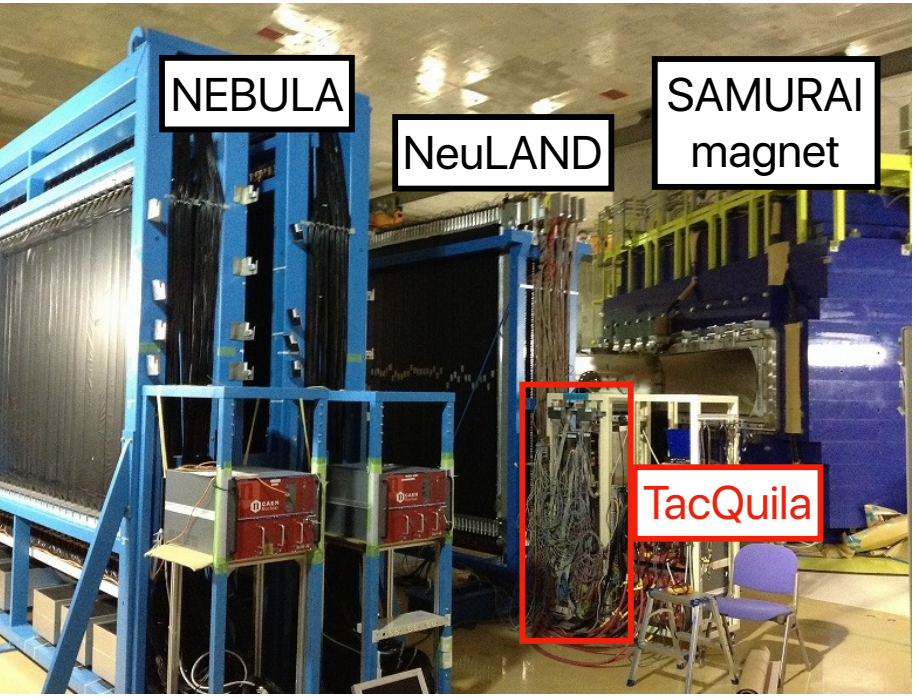




Since several branches use classical QDC/TDC, triggers must arrive earlier than signals at QDC/TDC inputs.

Fast trigger generation: mandatory

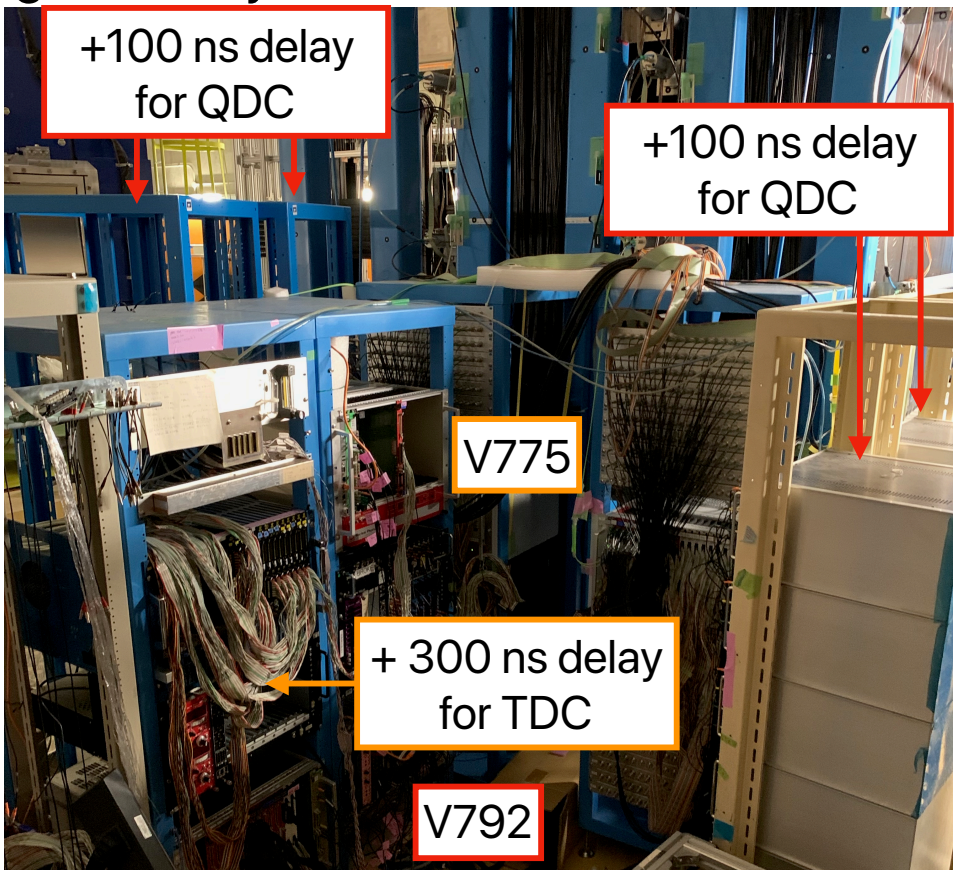
NeuLAND+TacQuila from GSI in 2015



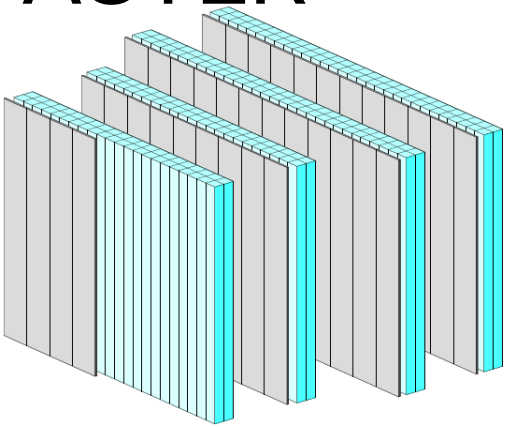
TacQuila: QDC+single-hit TDC based on ASIC
Trigger generation: 205 ns
~100 ns slower than NEBULA!

Add delays to NEBULA/HODF

NEBULA
144 plastic scintillator bars with PMTs at both ends.
→ 288 analog/logic signals for QDC/TDC
Original delays: 500 ns



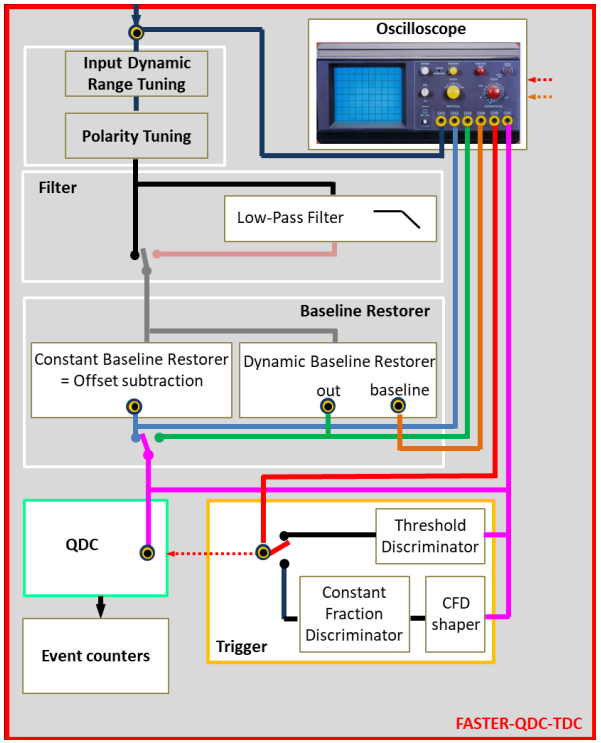
Near future: NEBULA-PLUS with FASTER



NEBULA-PLUS: Upgrading NEBULA with 90 NEBULA-type scintillator bars
→ 180 PMTs - Hamamatsu H11284

FASTER digital electronics: developed at LPC-CAEN (http://faster.in2p3.fr)
QDC & TDC module:
µTCA crate: 4 channels/module
12 bit, 500 MHz, 2 V max input, time stamping
→ Intrinsic time resolution: ~8 ps
→ Max charge: 1.5 µC
Trigger less system
modified to provide trigger = and of 2 PMTs
→ 450 ns delay to generate

35 FASTER modules are ordered
Funding requested for remaining 10 modules



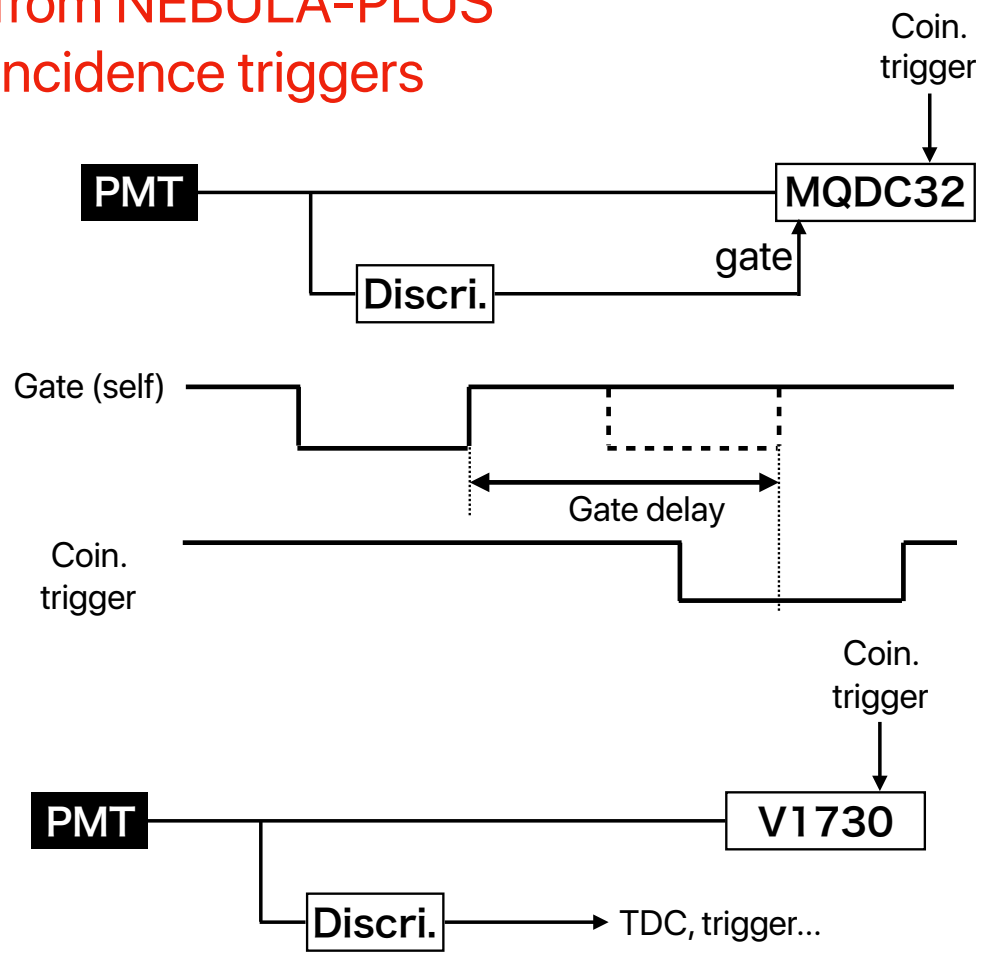
Courtesy of Orr

Free from cable delays in future!

To cope with late trigger from NEBULA-PLUS
Higher flexibility of coincidence triggers

Possibility for existing NEBULA.
- Delayed gating with MQDC32 from Mesytec
  - Conversion time = 250 ns
  - <3% loss of event with 500 kHz beam

Possibility for for HODF24.
- V1730 (Flash ADC + FPGA)
  - Charge integration at FPGA: less data size
- FASTER from LPC-CAEN



Summary and outlook

- SAMURAI DAQ
  - Many DAQ branches (>10).
  - Common trigger and common dead time.

- SAMURAI DAQ is getting faster.
  - Dead time: 230 us (April 2017) → 50 us (April 2019).
    - 50 us is realized with smaller DC and without neutron detectors.
      - More V1190s are necessary for full SAMURAI setup.
    - High power event-build PC, and better network infrastructure.

- SAMURAI DAQ will be free from cable delays in future.
  - Late trigger generation from NEBULA-PLUS.
  - High flexibility of the experimental triggers.