FEM-IB debugging

NWU, NCU, INTT group
M1 Mika Shibata
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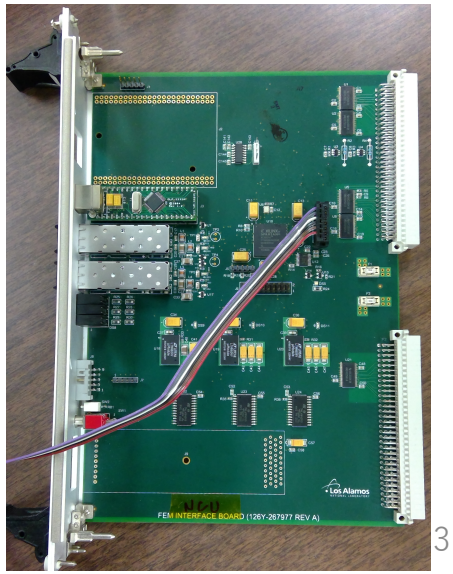
Back ground

- One FEM-IB couldn’t work.

Goal

- Search the cause of this problem and fix it.



What we know about FEM-IB status

Operation status

FEM-IB test

Here is the FEM-IB cheking affair

- We couldn't get data.
  - All modules without FEM-IB can work. (cables, INTT, FEM, ROC,…)
  - FPGA code of bad FEM-IB is same as that of NWU's.

Usable code for test bench

FEM-IB code

File name: 30-Aug-13

Download page: Location of the code

FEM IB 1, FEM IB 1 code

ROC FPGA and port : **C-1**
ROC chip power cable port : J1A
LV power setting : 3.6V
FPGA current : 0.62A->0.62A

	FEM	FEM code	FEM IB	FEM IB code	computer	ROC	bco/start board	JTAG	all cables	result
3	NWU	NWU	NCU 1	NCU 1 (same as NWU)	NWU	NWU	NWU		NWU	bad

- No data

ROC FPGA and port : **C-3**
ROC chip power cable port : J2A
LV power setting : 3.61V
FPGA current : 0.66A->0.66A

	FEM	FEM code	FEM IB	FEM IB code	computer	ROC	bco/start board	JTAG	all cables	result
3	NWU	NWU	NCU 1	NCU 1 (same as NWU)	NWU	NWU	NWU		NWU	bad

- No data

What we know about FEM-IB status

1. Differences of attached modules
2. Slow Control can work.
   - FEM-IB's LED can change when we sent command via GUI.
3. **FPHX chip's current doesn't change.**

Numbers which are written on FEM board panel are **different** from numbers of FPGA codes!

What we know about FEM-IB status

Differences of attached modules

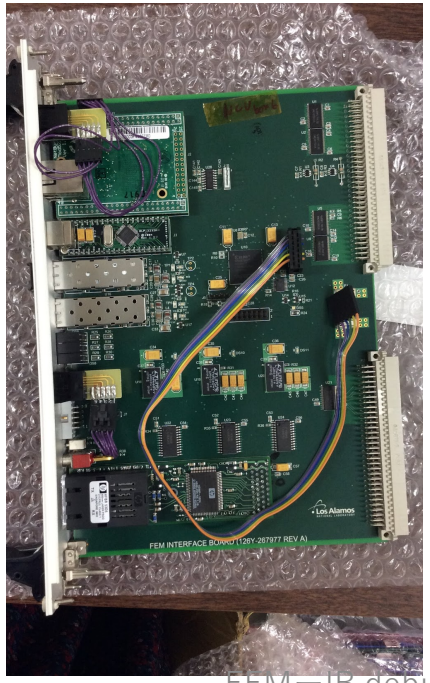
These modules are not used for Test Bench.

good FEM IB (box6)

Things not attached

(In the test at NWU, we used NWU's receiver to connect optical cable.)

- Start receiver

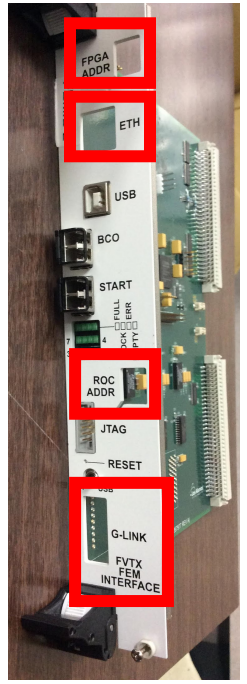


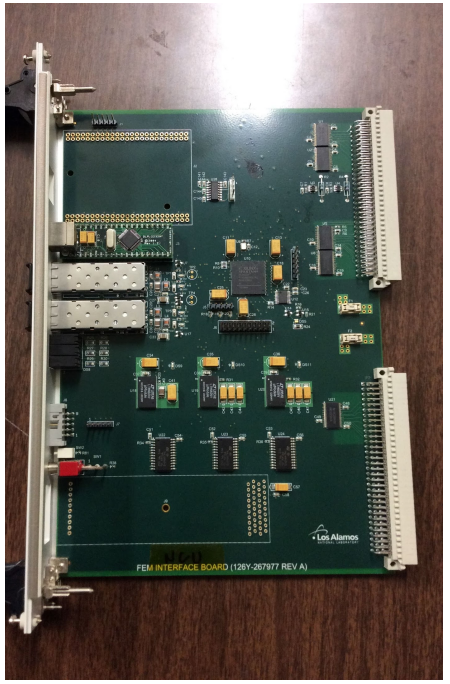
bad FEM IB 1

Things not attached

(In the test at NWU, we didn't use any NWU's things for below places.)

- FPGA ADDR
- ETH
- ROC ADDR
- G-LINK

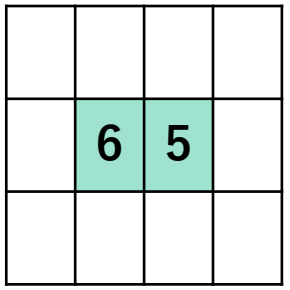




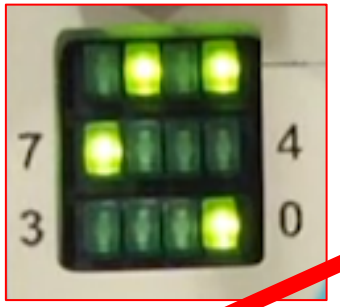
What we know about FEM-IB status

LED

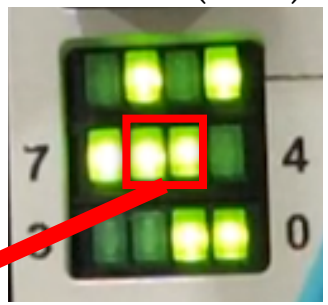
- No.5, 6 are lighting while the FEM-IB power is on.
  →The problem may come from the lack of modules.
  (No.5, 6 LED show “CRATE_ID”)



FEM-IB(NWU)



FEM-IB(NCU)



- FPGA ADDR
- ETH
- ROC ADDR
- G-LINK


```
LOCKED <= LOCKED_int;
LED_OUT(7) <= not GTM_LINK;
--LED_OUT(6) <= GLINK_RST_int;
LED_OUT(6 downto 5) <= CRATE_ID;
--LED_OUT(4) will go on if a start_calib command received from GTM
LED_OUT(3 downto 0) <= COMMAND_VME_int(3 downto 0);
```

FEM_IB_top.vhd

The FEM-IB’s LED can move same as good FEM-IB’s.

Detail: LED's color

- LED_TEST[] (1 downto 0)
  - LED_OUT(0)=0 : RED
  - LED_OUT(0)=1 : Green
  - LED_OUT(0)=Z : none

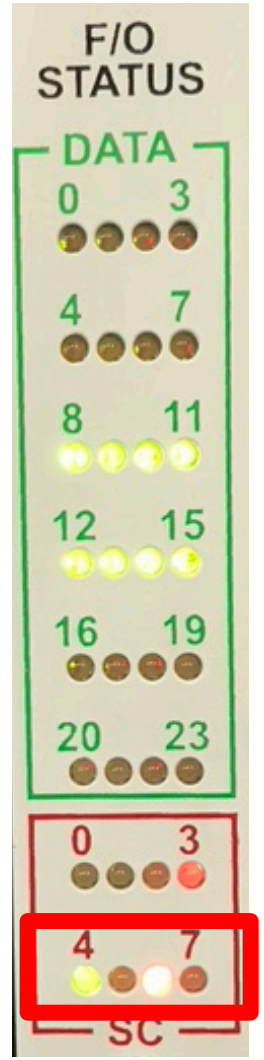
LED_OUT()<= '0' and '1' mean that the LED's color is red and green respectively. LED_OUT()<= 'Z' means that the LED isn't turn on.

- LED_TEST(0)=0(both NCU and NWU)
- LED_TEST(1)=0(both NCU and NWU)

```
LED_OUT(3) <= LED_TEST(0) when LED_TEST(1) = '1' else
                                    'Z' when (LED_TEST(1) = '0' and LED_TEST(0) = '1') else
                                    '1' when EMPTY = '1' else
                                    'Z';
LED_OUT(2) <= LED_TEST(0) when LED_TEST(1) = '1' else
                                    'Z' when (LED_TEST(1) = '0' and LED_TEST(0) = '1') else
                                    '0' when BUSY = '1' else
                                    'Z';
LED_OUT(1) <= LED_TEST(0) when LED_TEST(1) = '1' else
                                    'Z' when (LED_TEST(1) = '0' and LED_TEST(0) = '1') else
                                    '0' when MODE = '1' else
                                    'Z';
LED_OUT(0) <= LED_TEST(0) when LED_TEST(1) = '1' else
                                    'Z' when (LED_TEST(1) = '0' and LED_TEST(0) = '1') else
                                    'Z'; --'0' when MODE_2 = '1' else 'Z'; --LOCKED_int = '1' else 'Z';
```

DATA
LED_OUT()

3	2	1	0



Detail: FEM LED position and the meaning

Numbers which are written on FEM board panel are **different** from numbers of FPGA codes.

LED_OUT(7)~LED_OUT(0) of FPGA code (SlowControl_FEM.vhd)
II
No.0~7 of DATA on FEM board panel

LED_OUT(23)~LED_OUT(0) of FPGA code (FEM_top.vhd)
II
No.8~23 of DATA and No.0~7 of SC on FEM board panel

SlowControl_FEM.vhd
LED_OUT( )

7	6	5	4
3	2	1	0

FEM_top.vhd
LED_OUT( )

23	22	21	20
19	18	17	16
15	14	13	12
11	10	9	8
7	6	5	4
3	2	1	0

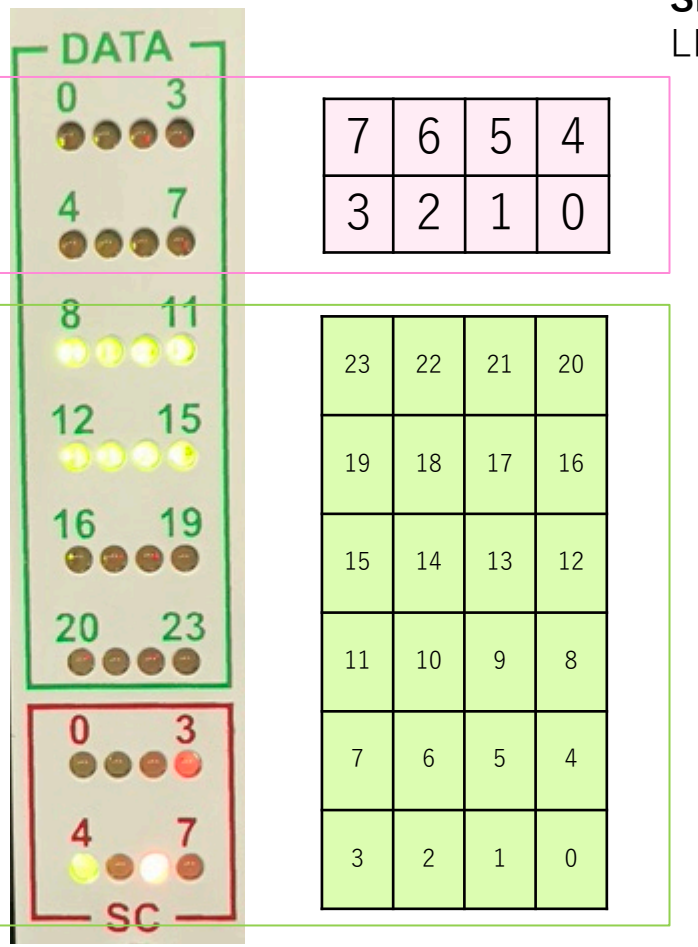
SYNC_OK	COMMAND_VME(2) = '1' and ((FEM_ADDR_VME = FEM_ADDR_REF) or FEM_ADDR_VME = x"F")	COMMAND_VME(1) = '1' and ((FEM_ADDR_VME = FEM_ADDR_REF) or FEM_ADDR_VME = x"F")	COMMAND_VME(0) = '1' and ((FEM_ADDR_VME = FEM_ADDR_REF) or FEM_ADDR_VME = x"F")
FEM_LVL1_DELAY(3 downto 1)	FEM_LVL1_DELAY(3 downto 1)	FEM_LVL1_DELAY(3 downto 1)	FEM_COMB_MODE

SYNC_OK_3_3	SYNC_OK_3_2	SYNC_OK_3_1	SYNC_OK_3_0
SYNC_OK_2_3	SYNC_OK_2_2	SYNC_OK_2_1	SYNC_OK_2_0
SYNC_OK_1_3	SYNC_OK_1_2	SYNC_OK_1_1	SYNC_OK_1_0
SYNC_OK_0_3	SYNC_OK_0_2	SYNC_OK_0_1	SYNC_OK_0_0
DATA_IN_0_BUF(0)	DATA_IN_1_BUF(0)	DATA_IN_2_BUF(0)	DATA_IN_3_BUF(0)
ENPTY	BUSY	MODE	Z

ENPTY and BUSY flash when calibration test is running

Detail: FEM LED position and the meaning

Numbers which are written on FEM board panel are **different** from numbers of FPGA codes.



SlowControl_FEM.vhd
LED_OUT( )

7	6	5	4
3	2	1	0

LED_OUT(7)~LED_OUT(0) of FPGA code (SlowControl_FEM.vhd)
II
No.0~7 of DATA on FEM board panel

23	22	21	20
19	18	17	16
15	14	13	12
11	10	9	8
7	6	5	4
3	2	1	0

LED_OUT(23)~LED_OUT(0) of FPGA code (FEM_top.vhd)
II
No.8~23 of DATA and No.0~7 of SC on FEM board panel

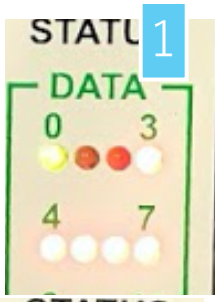
FEM_top.vhd
LED_OUT( )

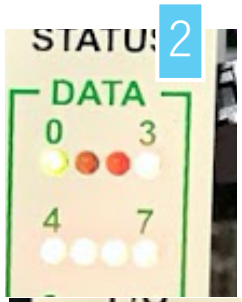
Detail: SC LEDs of FEM

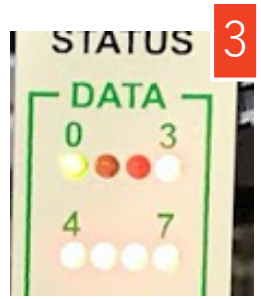
SC LEDs can change according to input signal (FPGA_ADDR_VME (2 downto 0)) from FPGA ADDR on FEM-IB board.

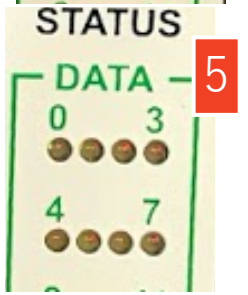
- Bad FEM-IB doesn't have FPGA ADDR module so the signal shows "000".
- Good FEM-IB have FPGA ADDR module so the signal can change.
  - These LED's are correctly working. (we checked FPGA code (FEM_IB_top.vhd))

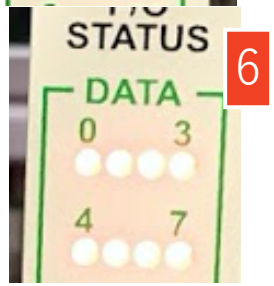
FPGA ADDR	FPGA_ADDR_VME (2 downto 0)	Calibration test result
0	000	OK
1	001	failed
2	010	failed
3	011	OK
4	100	failed
5	101	OK
6	110	OK
7	111	OK

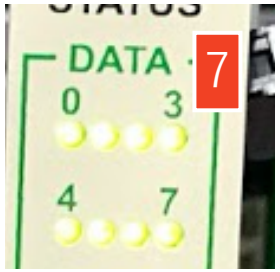




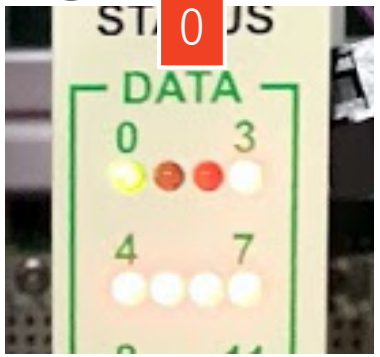


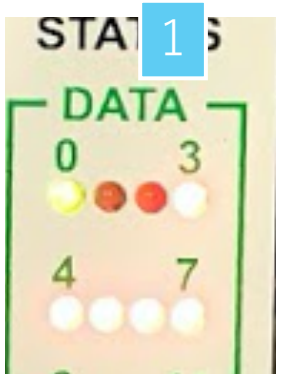


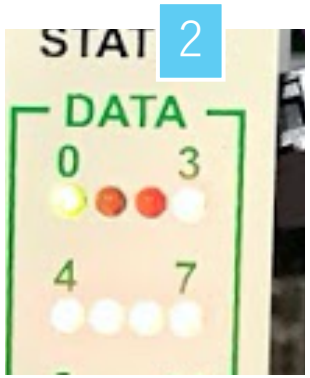


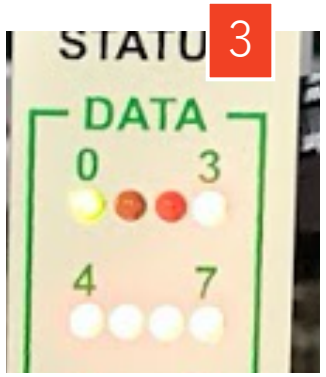


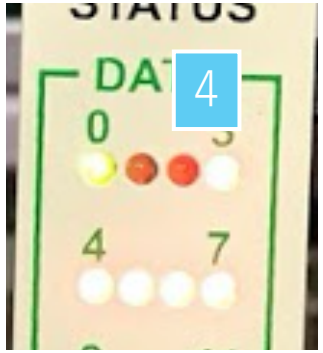
Detail: FEM LED meaning check











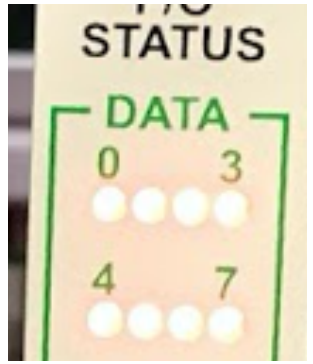

```
LED_OUT(7) <= '1' when SYNC_OK = '1'
LED_OUT(6) <= '0' when COMMAND_VME(2) = '1' and ((FEM_ADDR_VME = FEM_ADDR_REF) or FEM_ADDR_VME = x"F") else
'Z';
LED_OUT(5) <= '0' when COMMAND_VME(1) = '1' and ((FEM_ADDR_VME = FEM_ADDR_REF) or FEM_ADDR_VME = x"F") else
'Z';
LED_OUT(4) <= '0' when COMMAND_VME(0) = '1' and ((FEM_ADDR_VME = FEM_ADDR_REF) or FEM_ADDR_VME = x"F") else
'Z';
LED_OUT(3 downto 1) <= FEM_LVL1_DELAY(3 downto 1);
LED_OUT(0) <= '0' when FEM_COMB_MODE = '1'
```

- SYNC_OK = ‘1’ **GREEN**
- COMMAND_VME(0) = ‘1’ **none”Z”**
- COMMAND_VME(1) = ‘1’ **none”Z”**
- COMMAND_VME(2) = ‘0’ **RED**
- FEM_LVL1_DELAY(3 downto 1) = “000” **RED RED RED**
- FEM_COMB_MODE = ‘1’ **RED**

Detail: FEM LED meaning check

```
LED_OUT(0) <= FPGA_ADDR_VME(0) when FPGA_ADDR_VME(2 downto 1) = "11"
LED_OUT(3 downto 1) <= "111" when FPGA_ADDR_VME = "111" else
                       "000" when FPGA_ADDR_VME = "110"
LED_OUT(4) <= FPGA_ADDR_VME(0) when FPGA_ADDR_VME(2 downto 1) = "11"
LED_OUT(5) <= FPGA_ADDR_VME(0) when FPGA_ADDR_VME(2 downto 1) = "11"
LED_OUT(6) <= FPGA_ADDR_VME(0) when FPGA_ADDR_VME(2 downto 1) = "11"
LED_OUT(7) <= FPGA_ADDR_VME(0) when FPGA_ADDR_VME(2 downto 1) = "11"
```

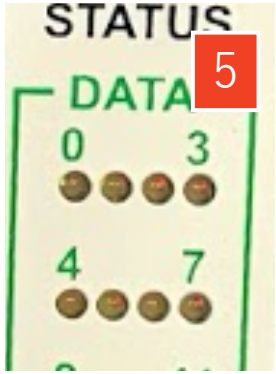
6



7

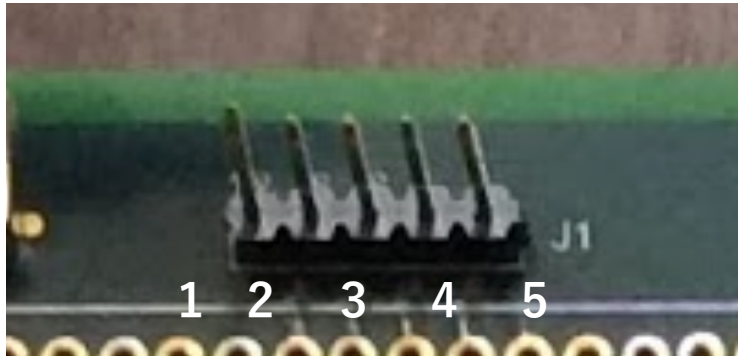
6. FPGA_ADDR_VME(2 downto 0) = “110” → FPGA_ADDR_VME(0) = 0->Red
7. FPGA_ADDR_VME(2 downto 0) = “111” → FPGA_ADDR_VME(0) = 1->Green

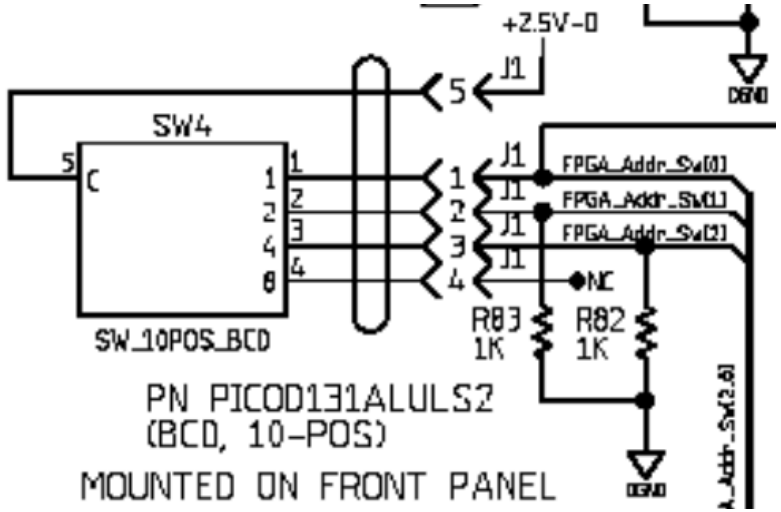
```
LED_OUT(0) <= 'Z' when FPGA_ADDR_VME = "101”
LED_OUT(3 downto 1) <= "ZZZ" when FPGA_ADDR_VME = "101"
LED_OUT(4) <= 'Z' when FPGA_ADDR_VME = "101"
LED_OUT(5) <= 'Z' when FPGA_ADDR_VME = "101"
LED_OUT(6) <= 'Z' when FPGA_ADDR_VME = "101”
LED_OUT(7) <= 'Z' when FPGA_ADDR_VME = "101"
```

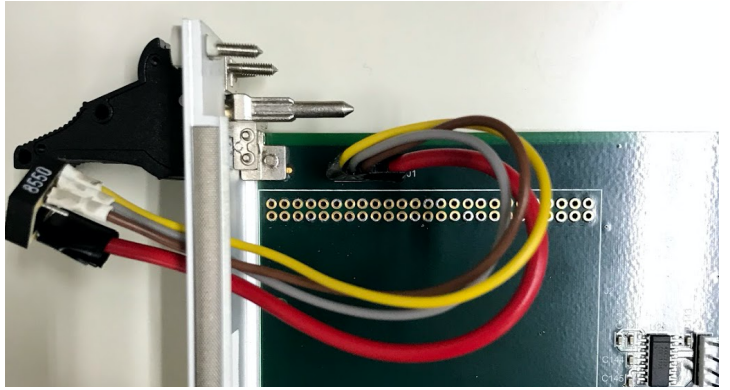


5. FPGA_ADDR_VME(2 downto 0) = “101” → FPGA_ADDR_VME(0) = 0 -> Z

We made FPGA ADDR switch







- Bad FEM-IB didn't have this switch so we made it.
- This switch can work expectedly. (This can change FEM's LEDs.)
- But this switch isn't the cause of FEM-IB problem.

FPHX chip’s current doesn’t change.

1. **FPHX chip’s current doesn’t change.**
   - The current should decline when “INIT” command is sent. (ex. 0.62A->0.52A)
   - On GUI, we checked whether ”INIT” command was sent or not and know the command was sent. (Other commands also look workable)
   - “FFR” command reaches at ROC board. (The signal can checked on ROC board using oscilloscope)
   - FEM-IB USB port can get data correctly.
     - We compared these signals of good fem-ib and bad fem-ib.
     - These signals are same.

Order for global start / Calibration test

1. FO Sync
2. FPGA RST
3. FFR
4. Init
5. Enable RO
6. Latch FPGA
7. Set L1 Delay
8. BCO Start
9. Calib
10. Start DAQ

“INIT”
：Download parameters to FPHX chips. This needs to be issued after FFR. If INIT has worked properly, you should see the digital current draw for the wedges drop from the value that you have after a FFR.

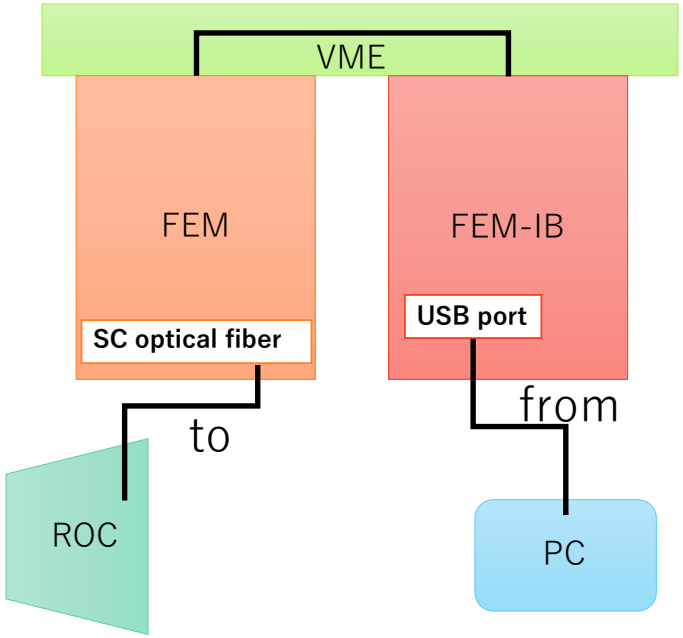
Data from PC to ROC

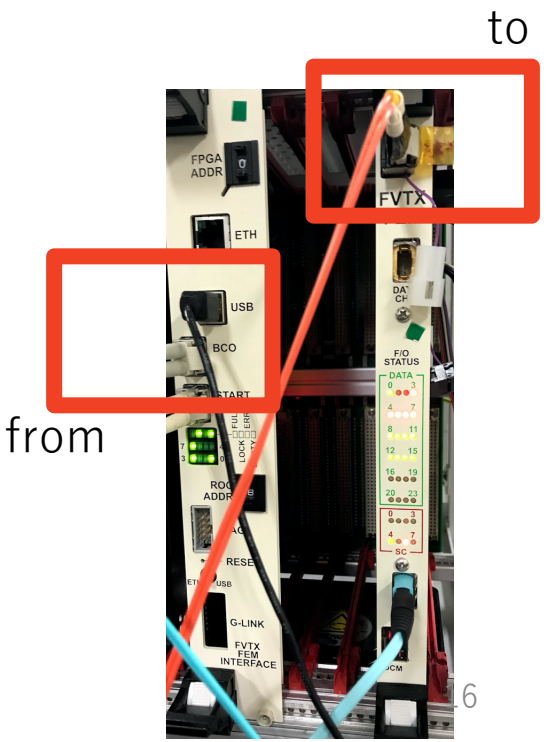
- **We checked commands' signals from USB port on FEM-IB to SC port on FEM.**

1. **FEM-IB USB port** can get data correctly.
   - We compared **these signals** of good fem-ib and bad fem-ib.
   - These signals are same.

2. **FEM SC port** cannot get data correctly.
   - We compared **these signals.**
   - These signals are slightly different.

FEM board is same, so signals may break between FEM-IB and VME.

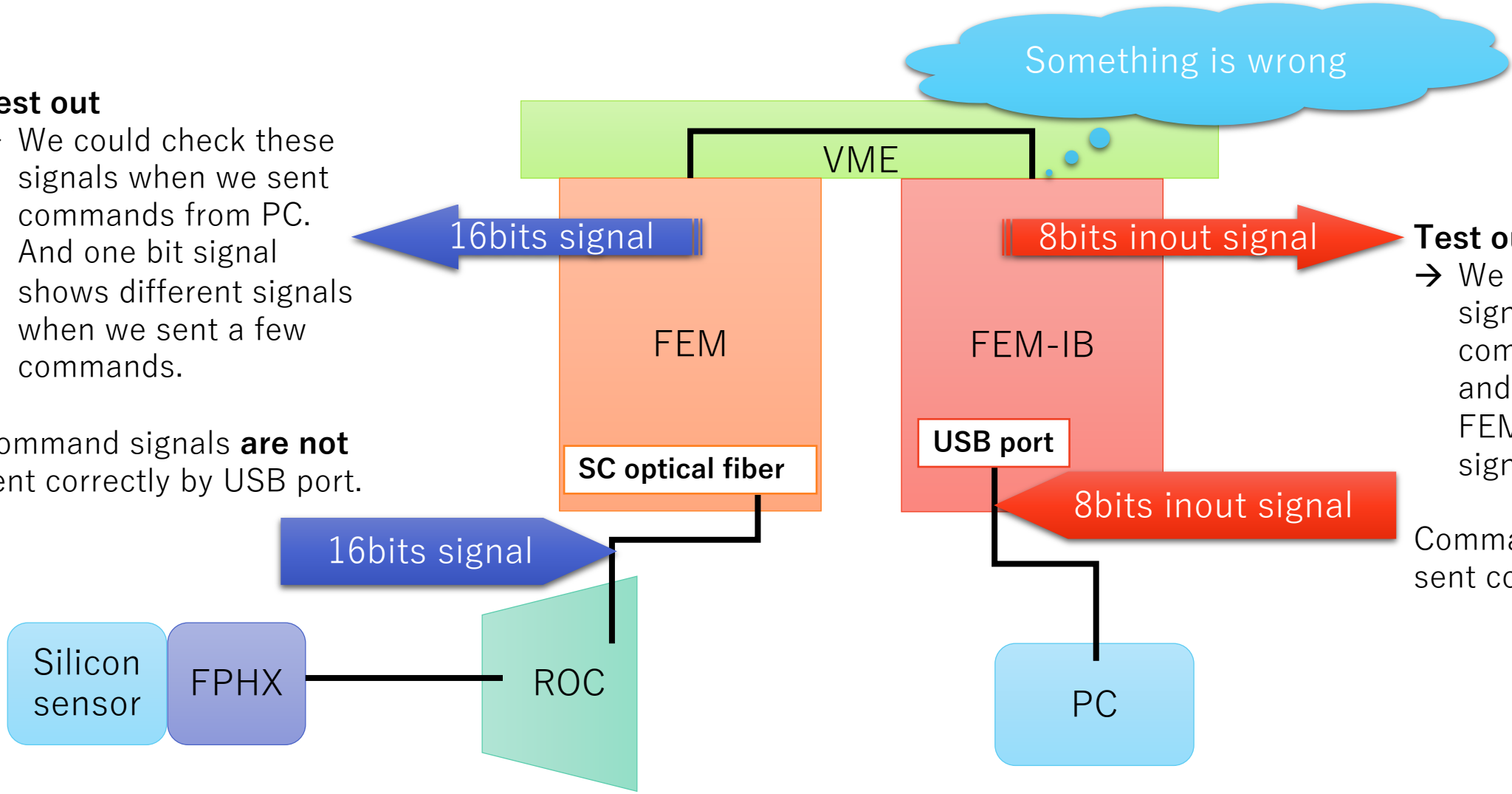




Detail: Data from PC to ROC

Test out
→ We could check these signals when we sent commands from PC. And one bit signal shows different signals when we sent a few commands.

Command signals **are not** sent correctly by USB port.

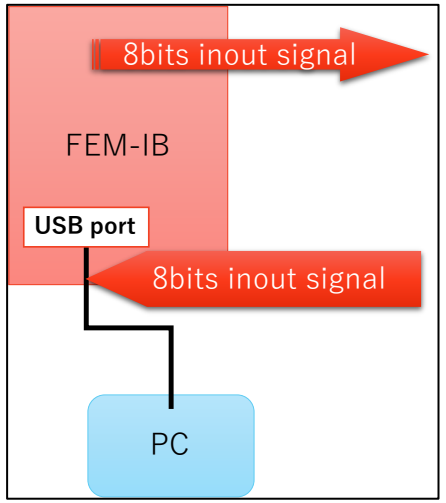


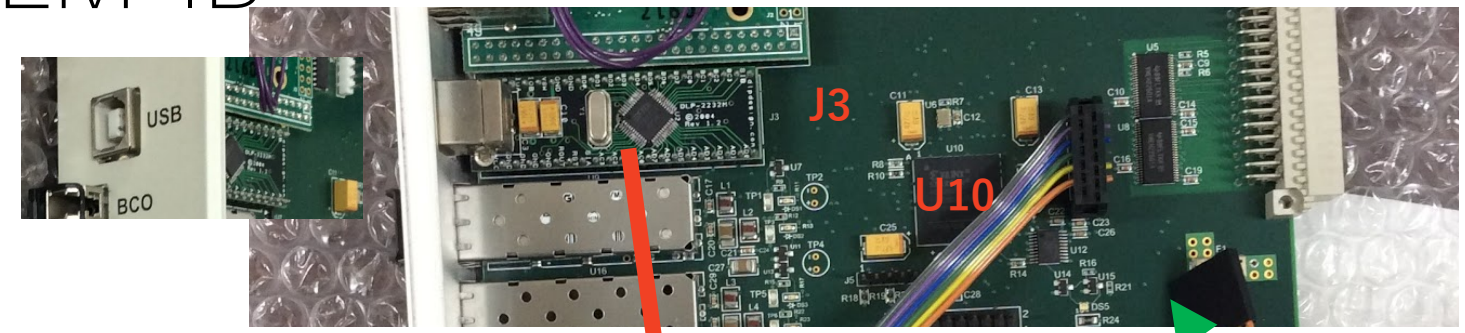
Test out
→ We could check these signals when we sent commands from PC and good and bad FEM-IB have same signals.

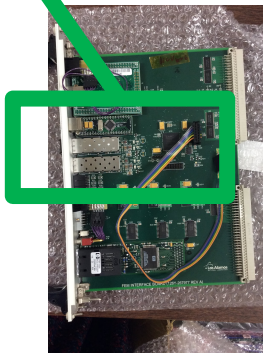
Command signals **are** sent correctly by USB port.

FEM board is same, so signals may break between FEM-IB and VME.

Detail: Data from PC to FEM-IB





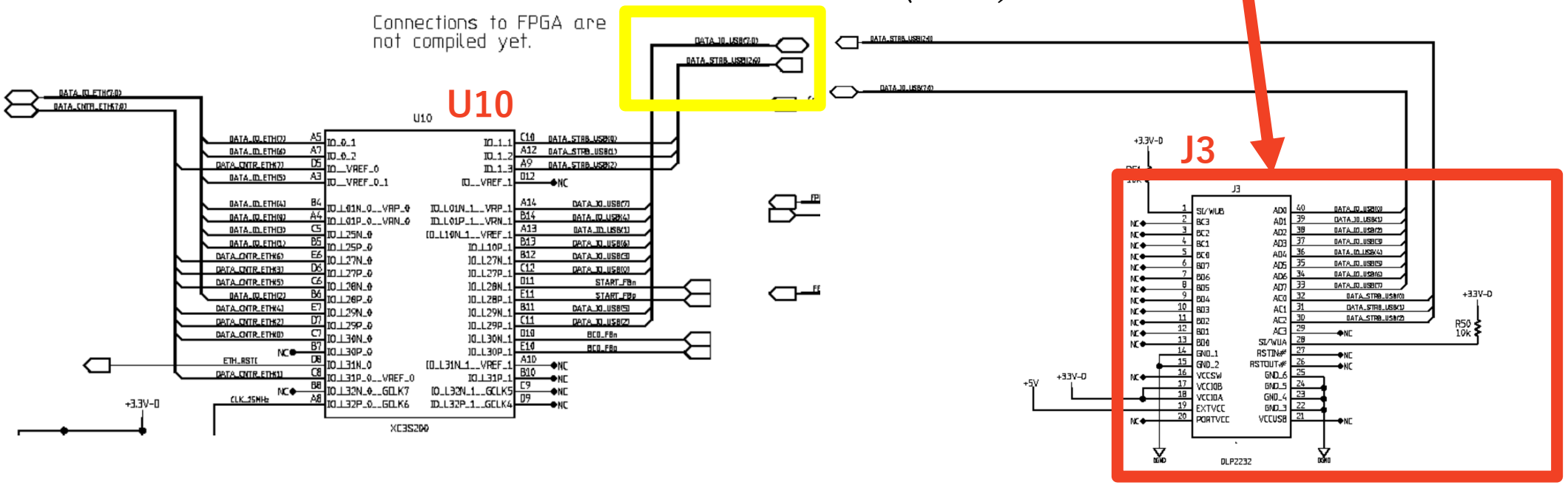


FEM-IB

```
DATA_IO_USB                    : inout std_logic_vector(7 downto 0);
```

Test out data (8bits)

Connections to FPGA are not compiled yet.

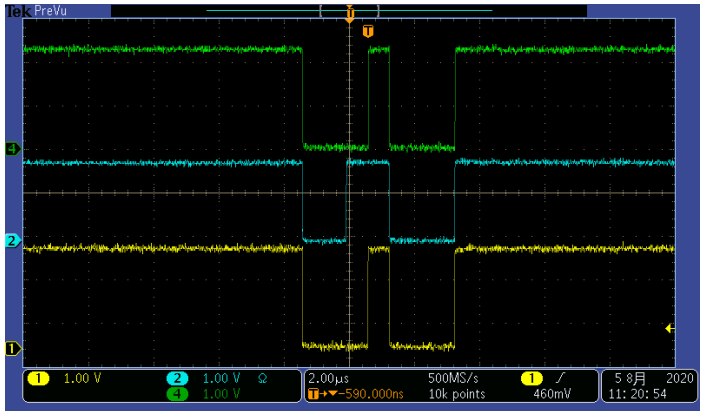


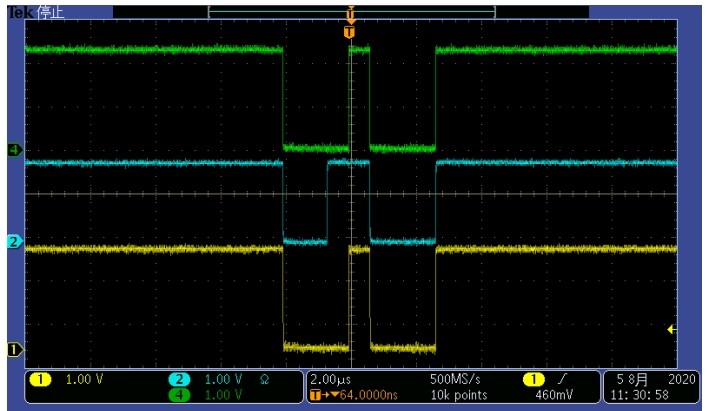
Detail: Data from PC to FEM-IB
Fo sync

good

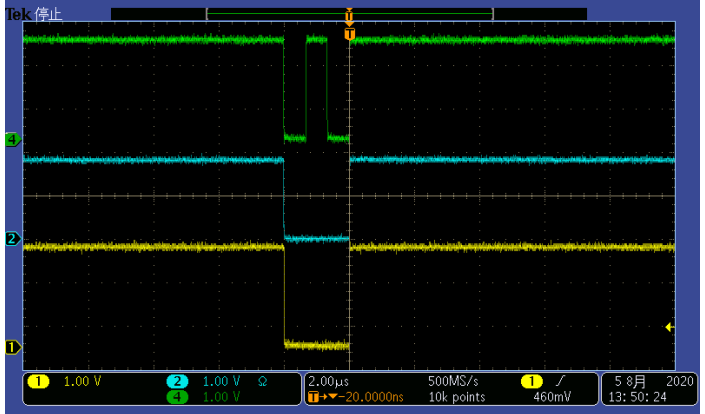
bad

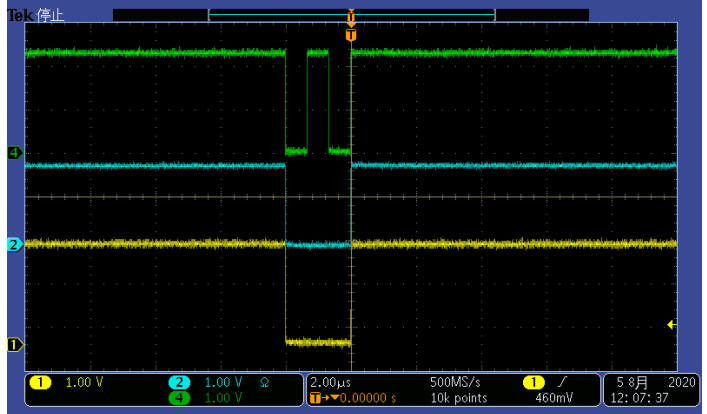
4 5 6



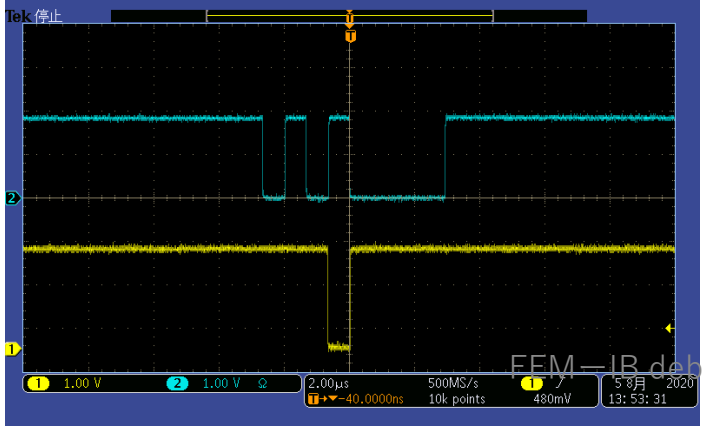


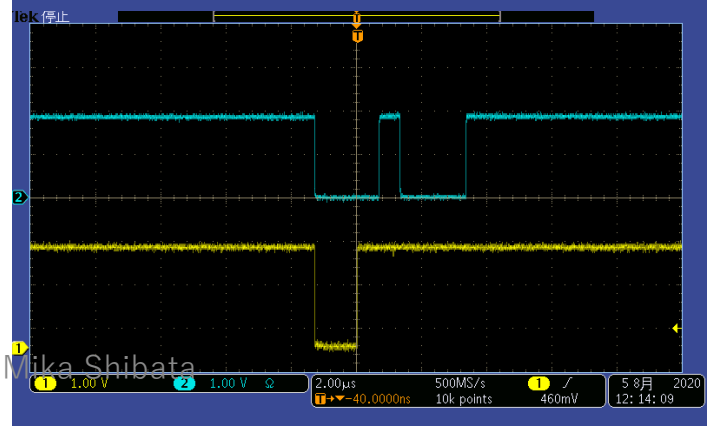
123





07

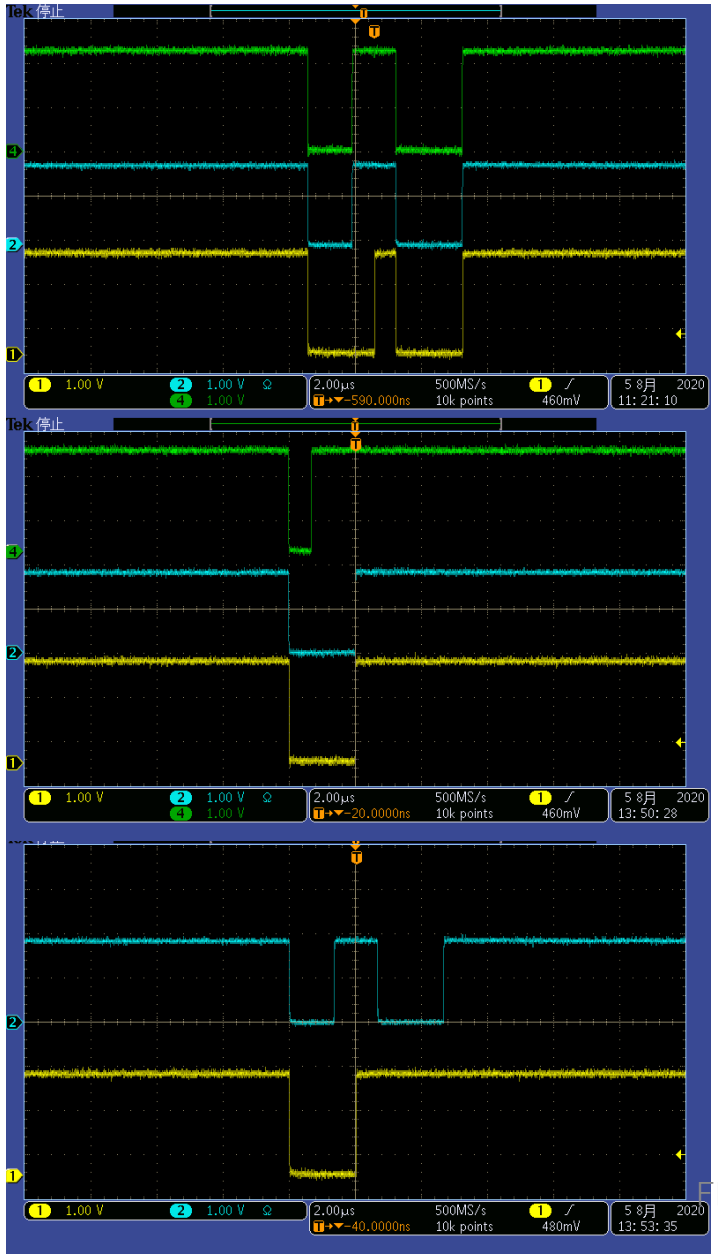




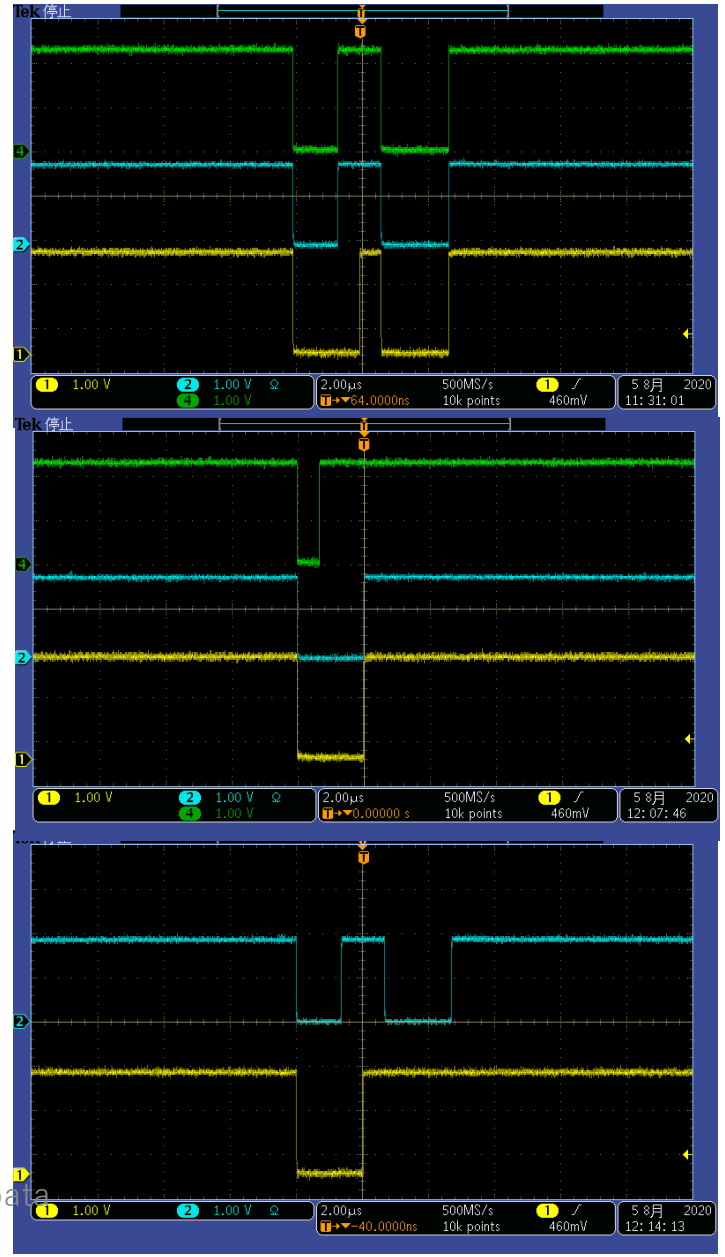
Detail: Data from PC to FEM-IB

Fpga reset

good

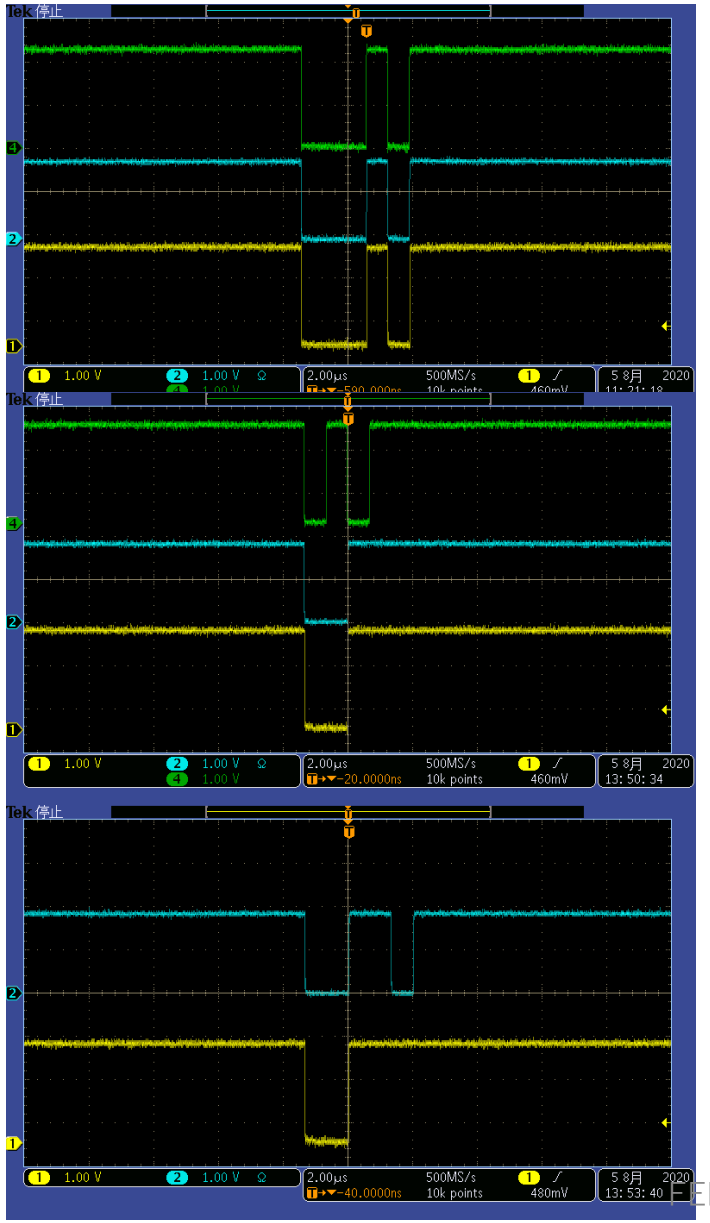


bad



Detail: Data from PC to FEM-IB ffr

good



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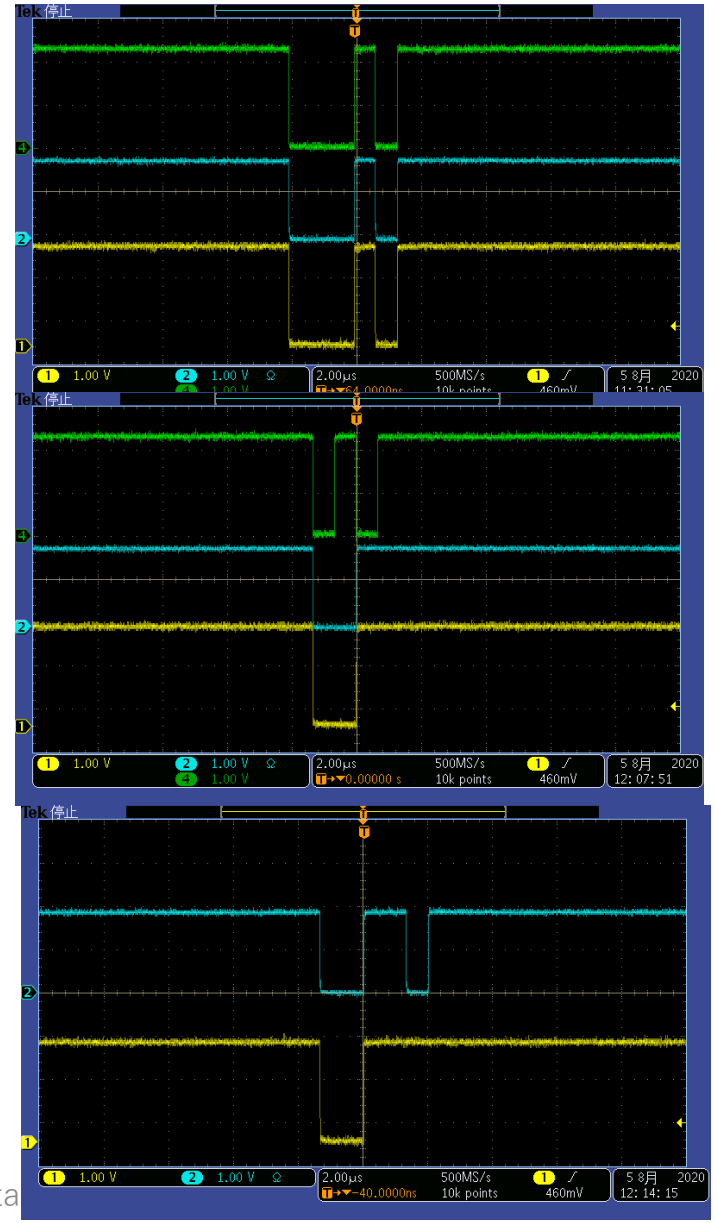
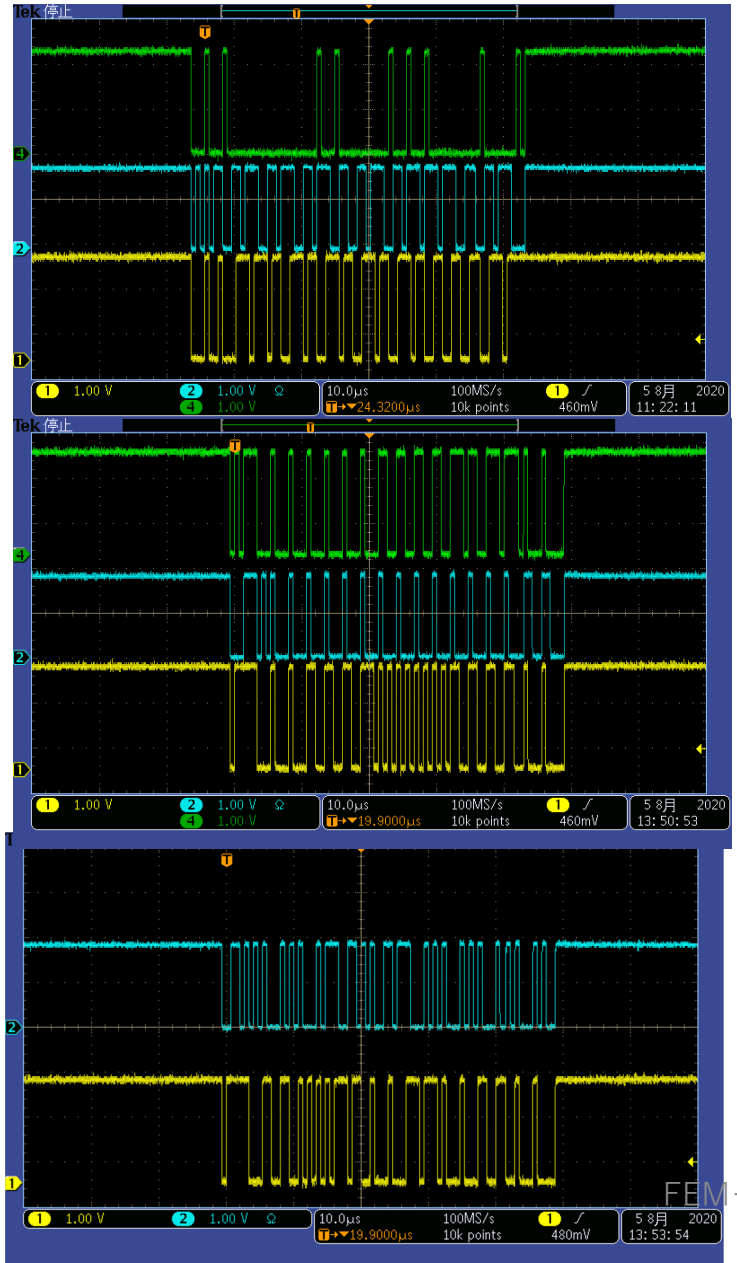
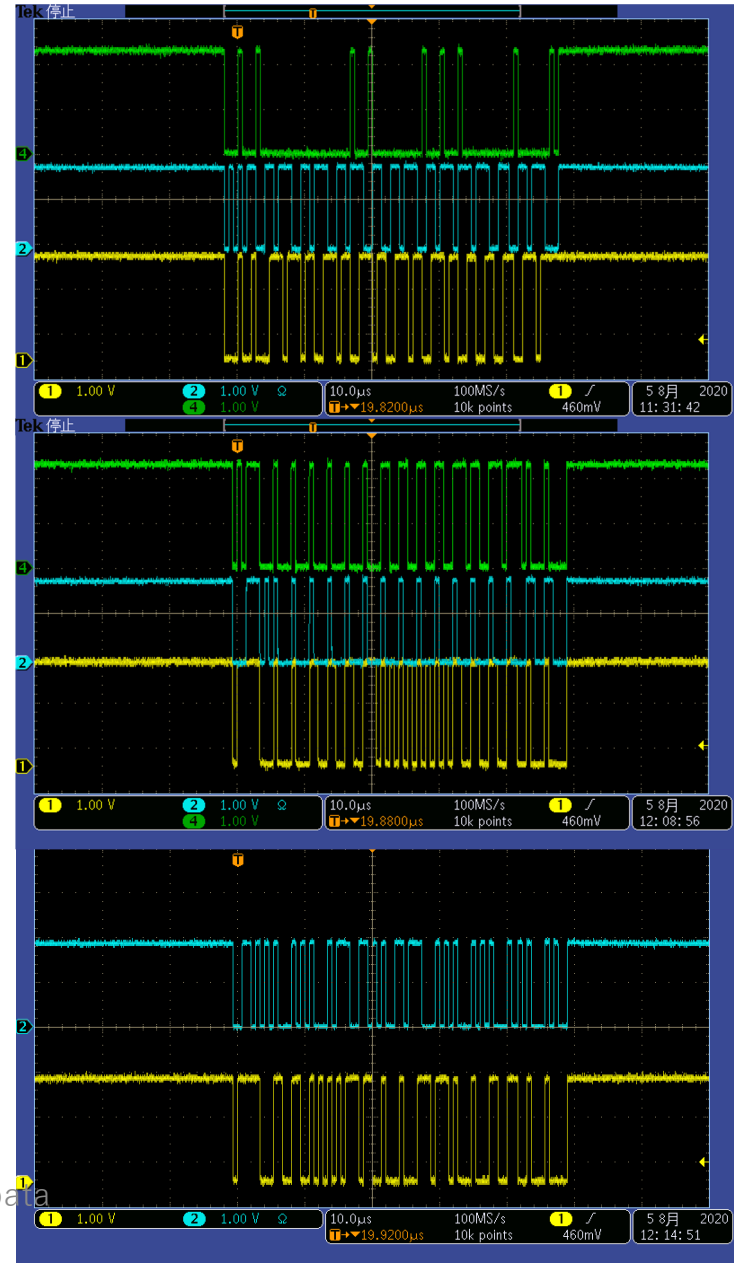


Detail: Data from PC to FEM-IB init

good



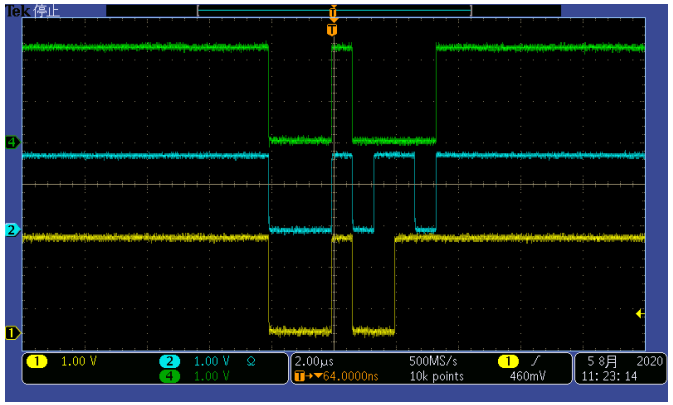
bad

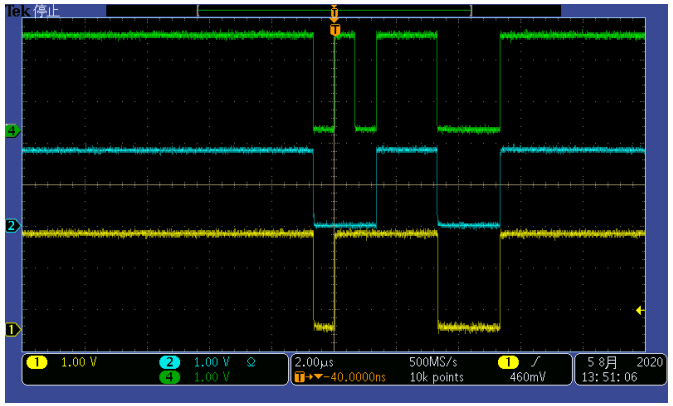


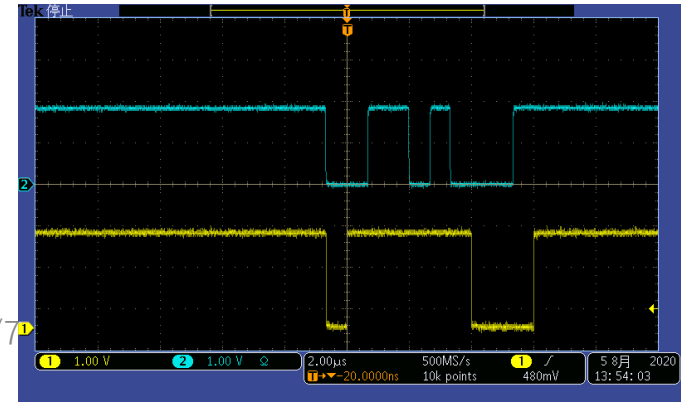
Detail: Data from PC to FEM-IB

Enable ro

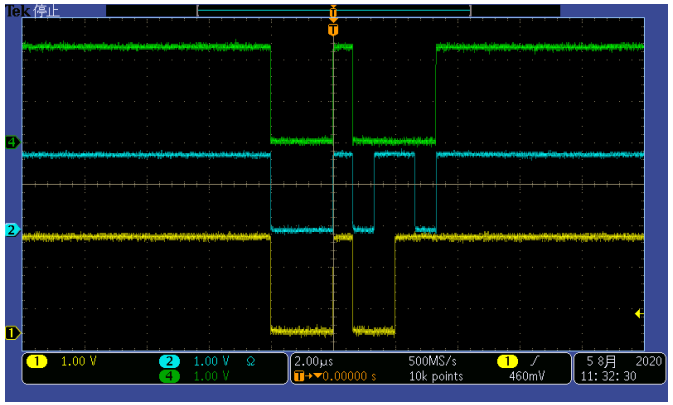
good

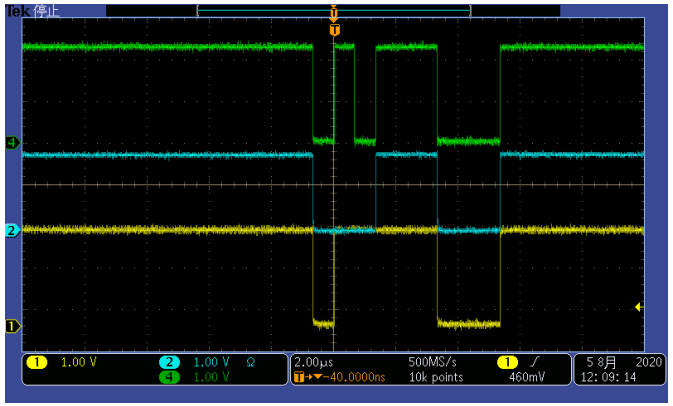


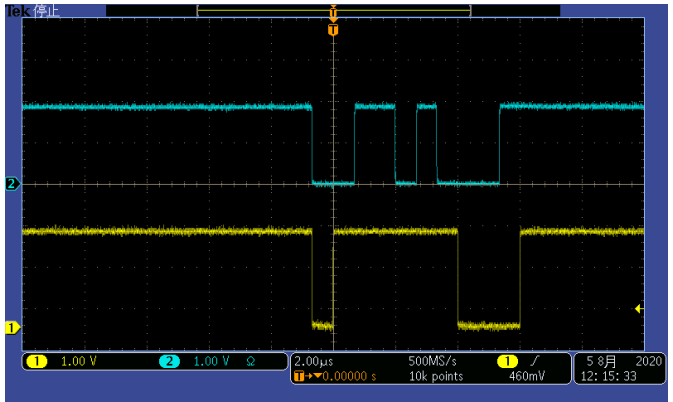




bad

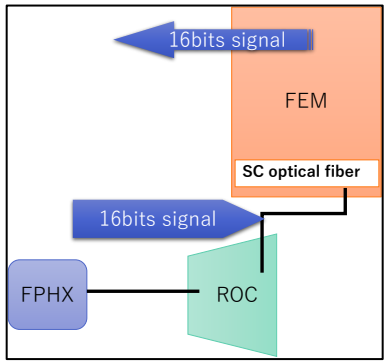




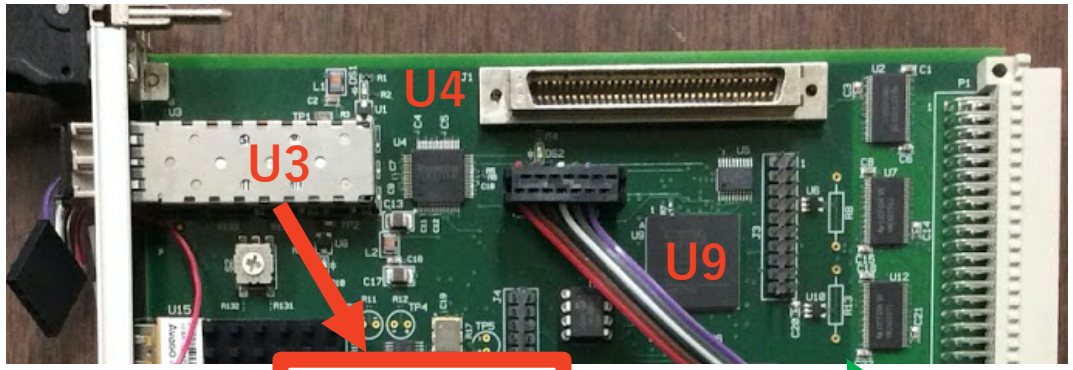


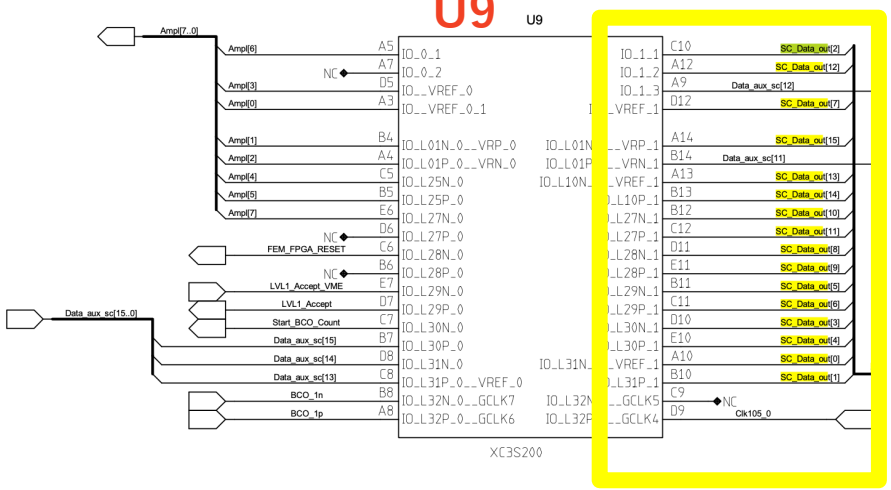
Detail: Data from FEM to ROC

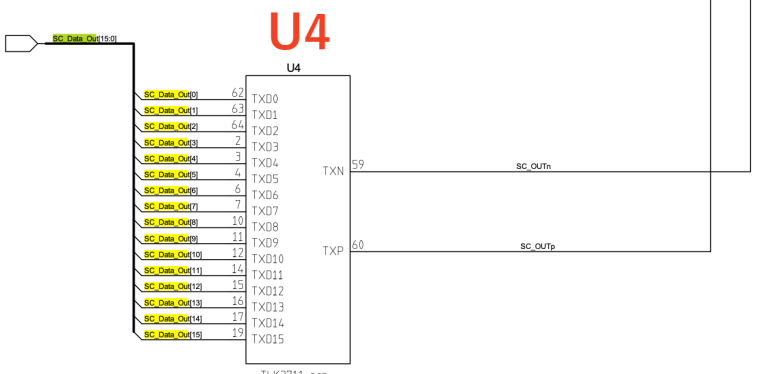
```
DATA_TX_OUT(0)                      <= WEDGE_ADDR_OUT;          --ADDR
DATA_TX_OUT(1)                      <= COMMAND_OUT;                     --COMMAND
DATA_TX_OUT(2)                      <= READ_EN_BUF and READ_EN;         --CS_ADDR
DATA_TX_OUT(3)                      <= DATA_FIFO_OUT(0);                --DO_SC
DATA_TX_OUT(4)                      <= STROBE;                                  --Data STROBE
DATA_TX_OUT(6 downto 5)     <= (others => '0');
DATA_TX_OUT(7)                      <= DATA_FIFO_OUT(1);                --CS_SC_VME
DATA_TX_OUT(8)                      <= BUSY;                                    --BUSY from FEM Data FPGA
DATA_TX_OUT(12 downto 9)    <= TCK_VME & TDI_VME & TMS_VME & TRST_VME;
DATA_TX_OUT(15 downto 13)   <= FPGA_ADDR_VME;
```

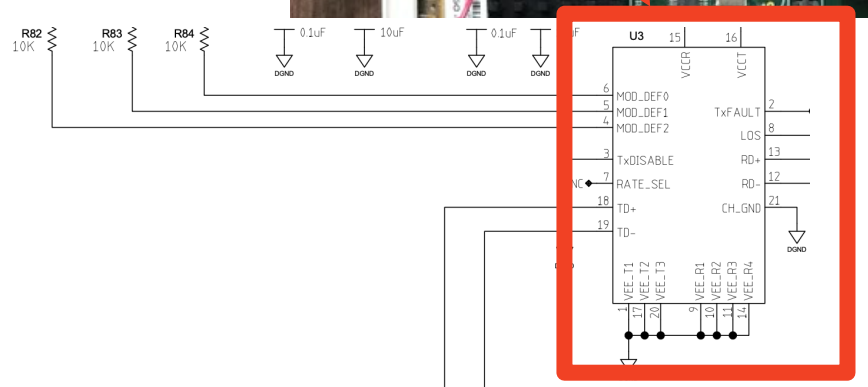


Test out data (16 bits)

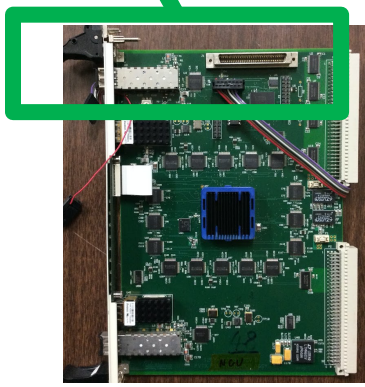








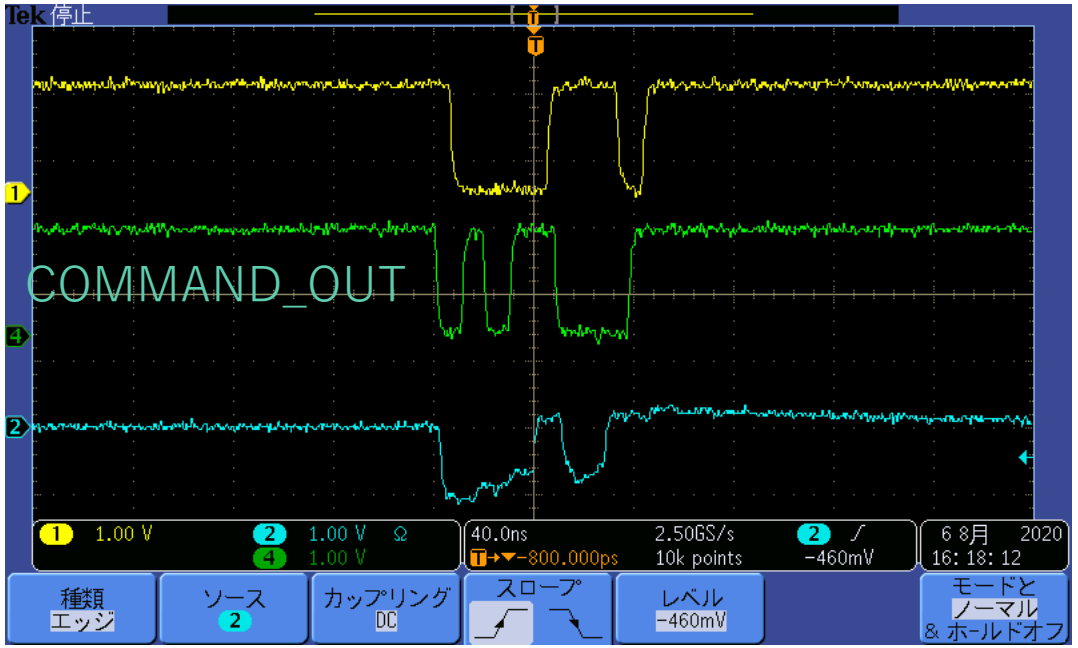
U3



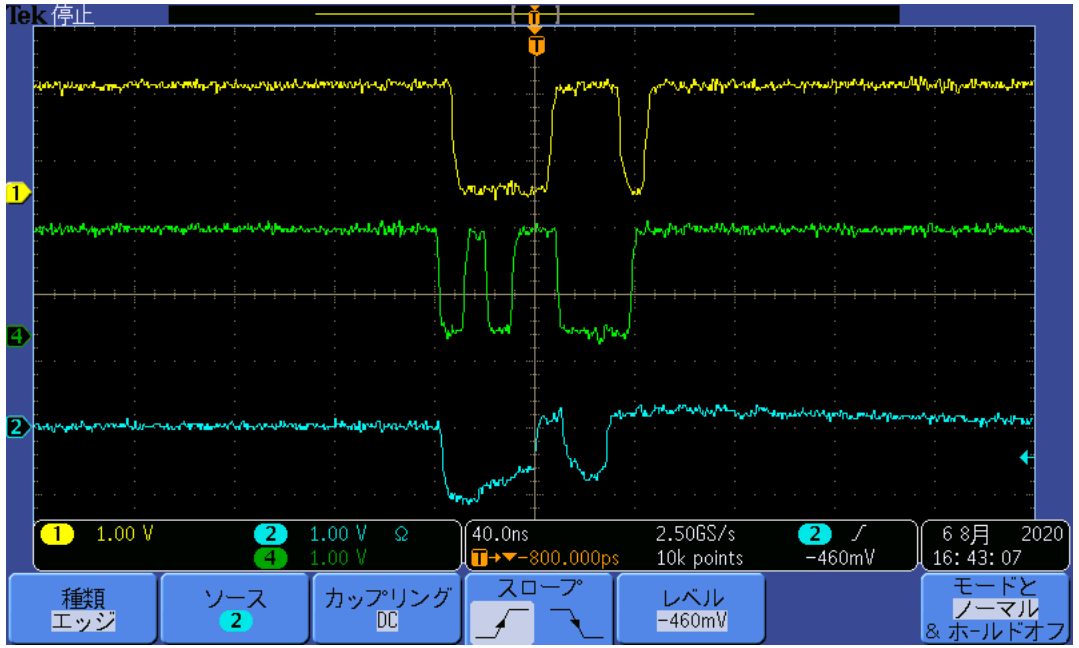
FEM

Detail: Data from FEM to ROC
FO SYNC

good

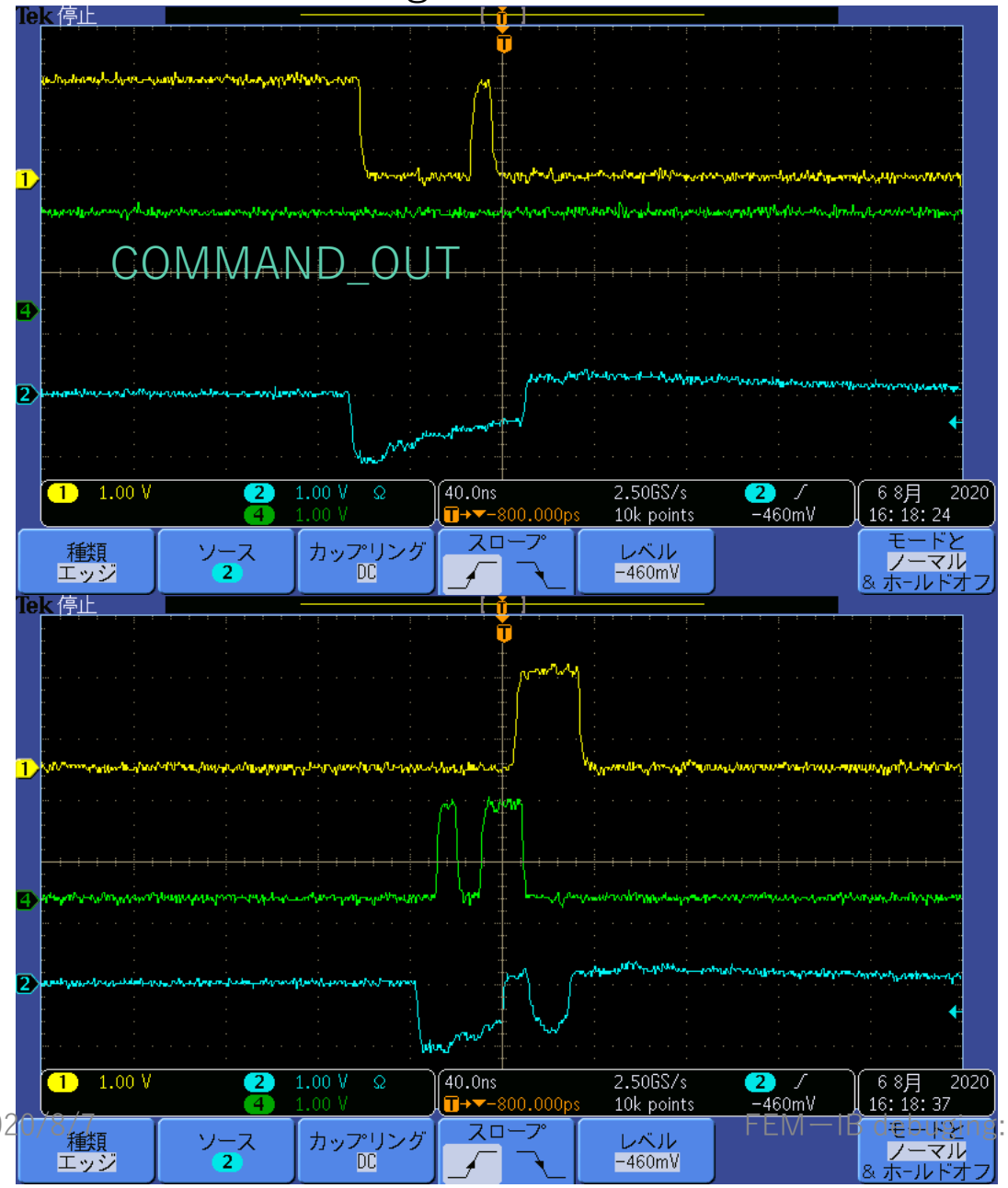


bad

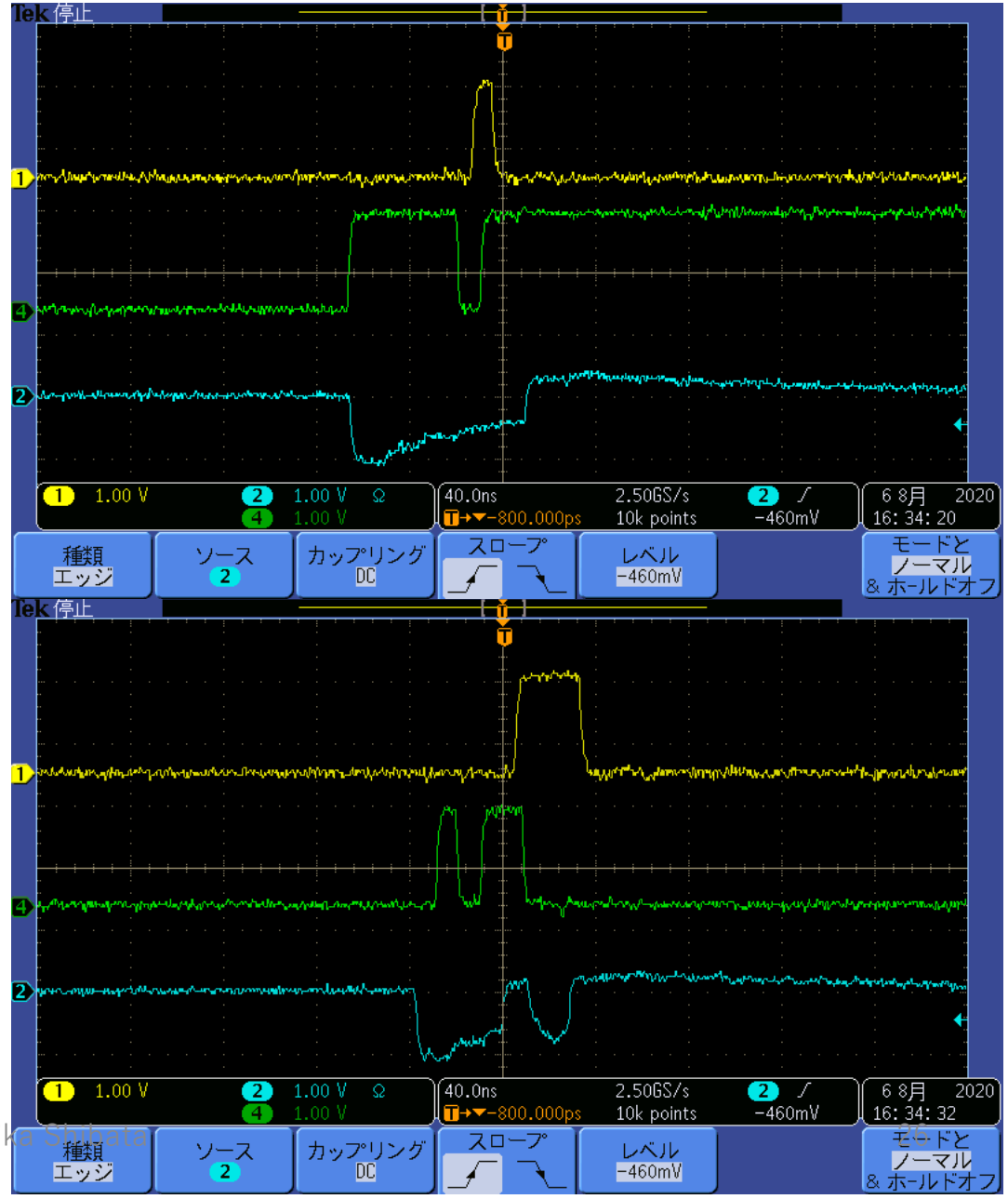


Detail: Data from FEM to ROC
Fpga reset

good

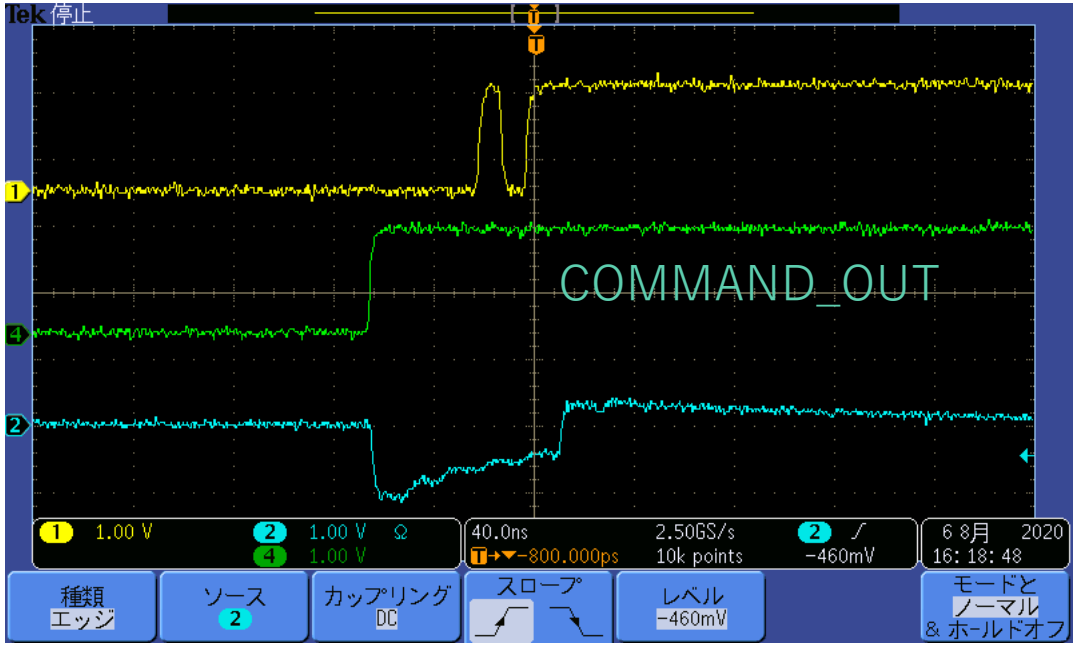


bad

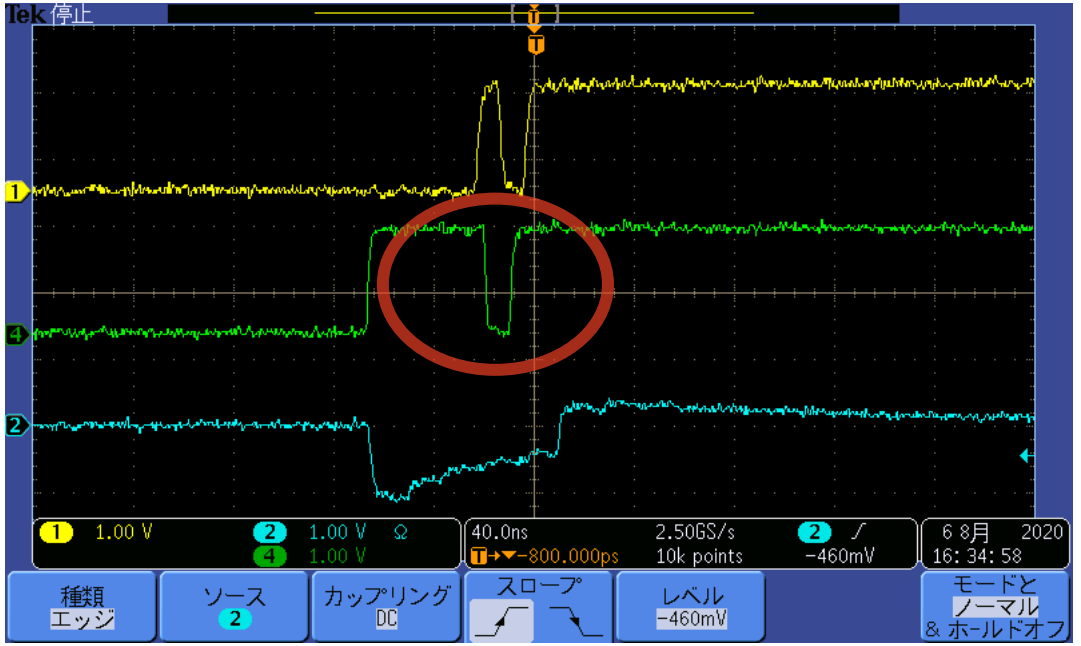


Detail: Data from FEM to ROC
ffr

good

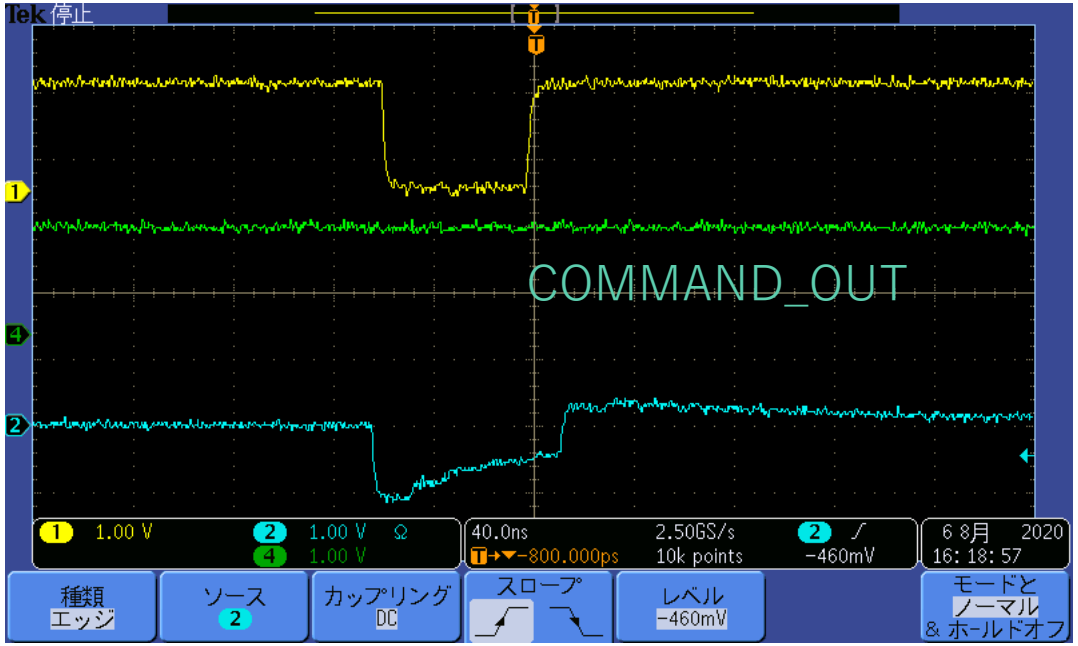


bad

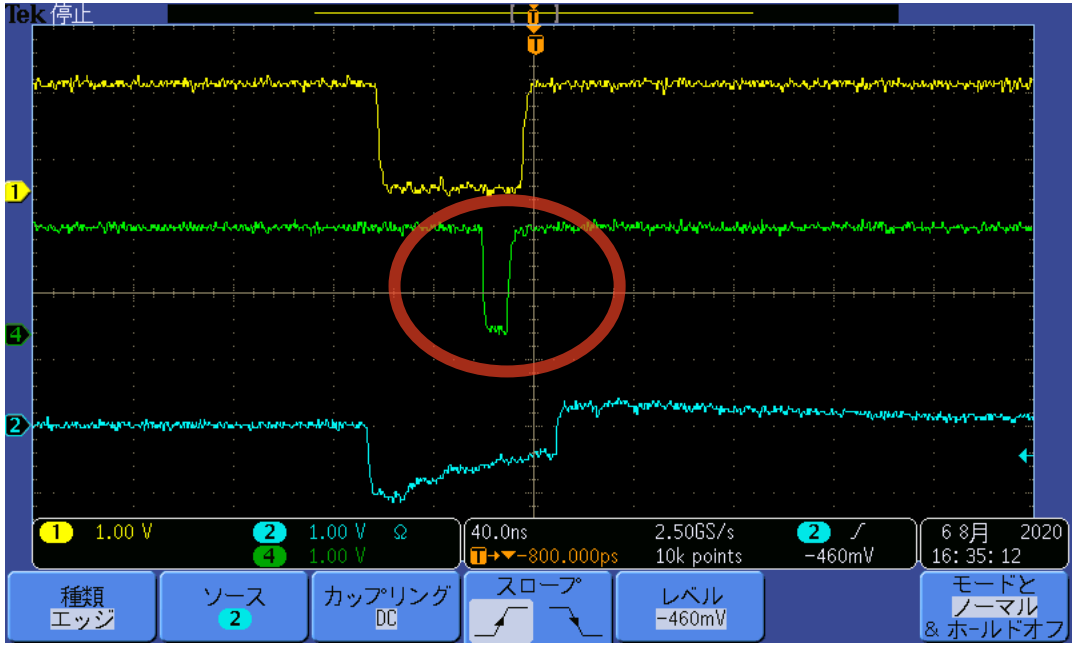


Detail: Data from FEM to ROC init

good

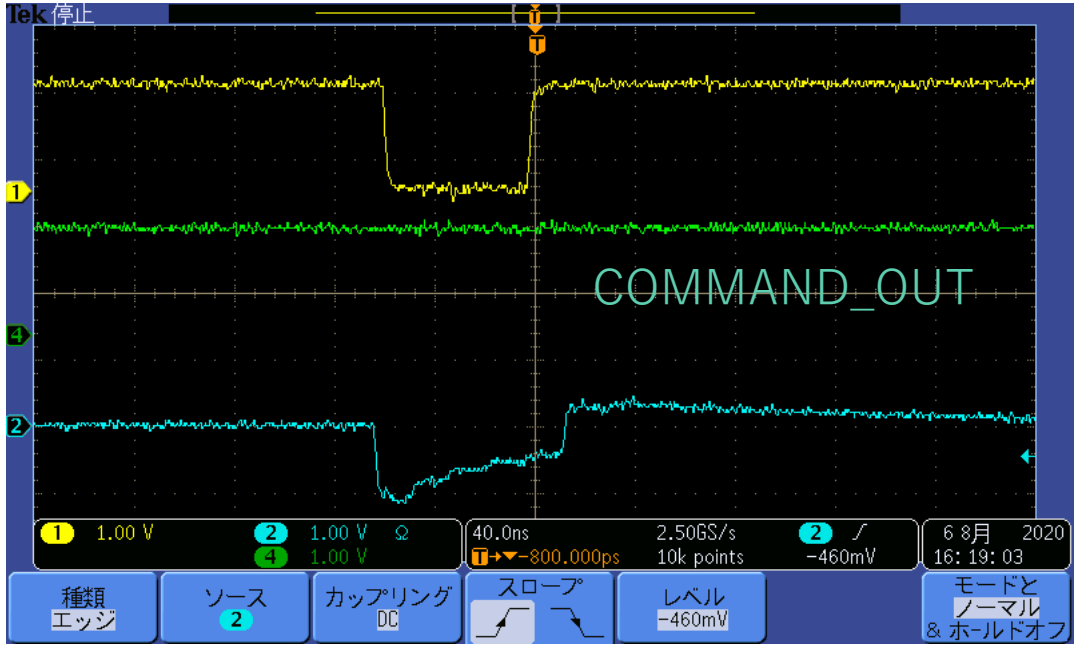


bad

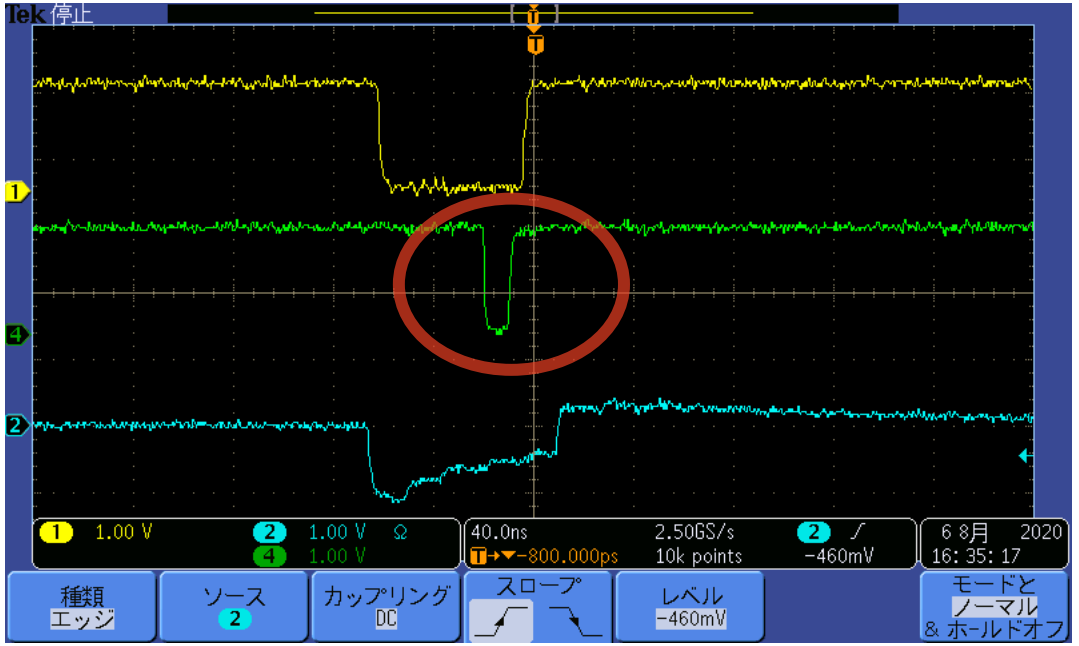


Detail: Data from FEM to ROC
Enable ro

good

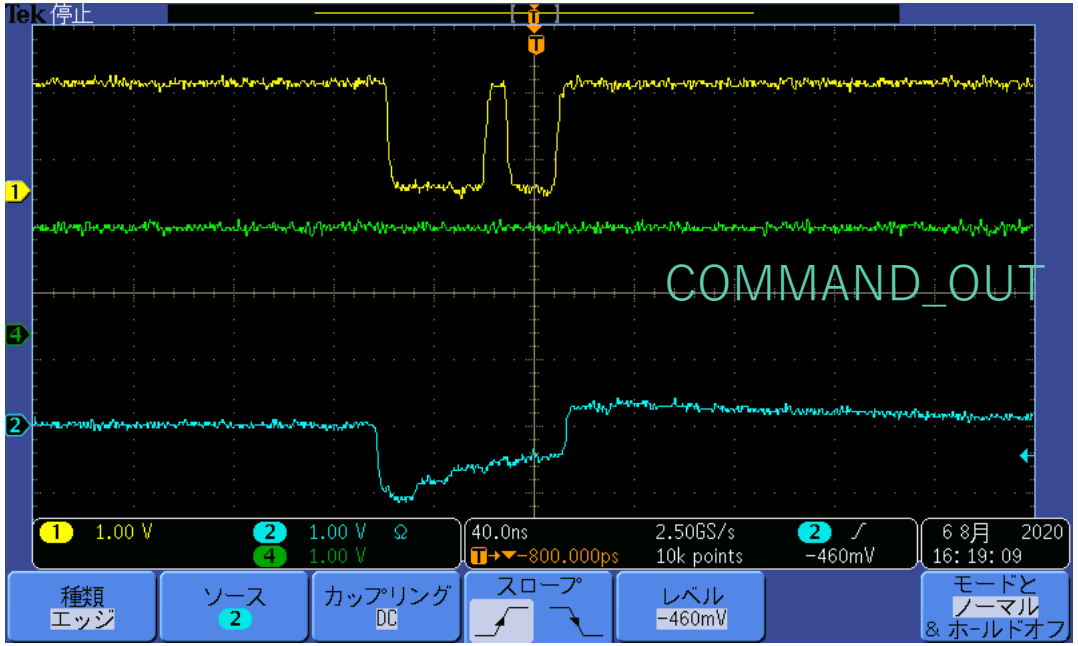


bad

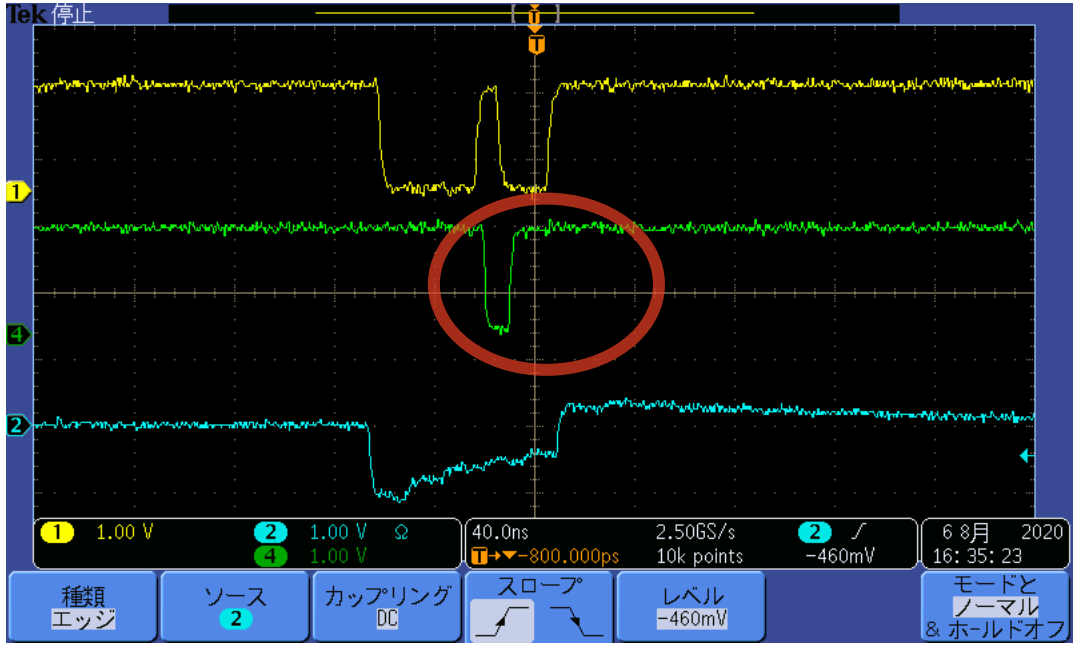


Detail: Data from FEM to ROC
Latch fpga

good

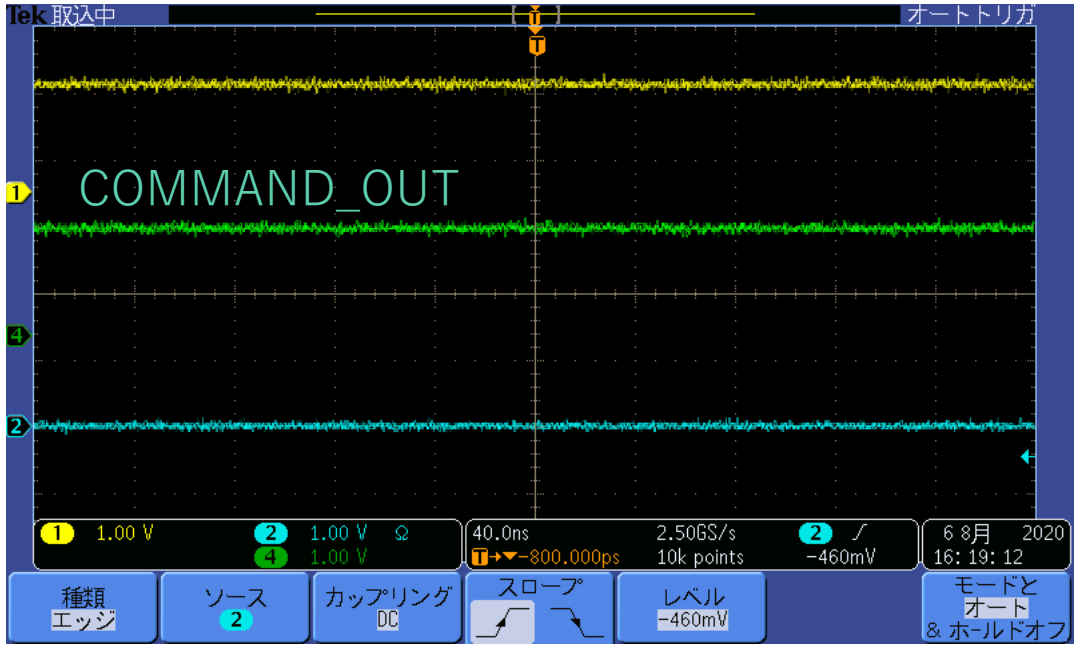


bad

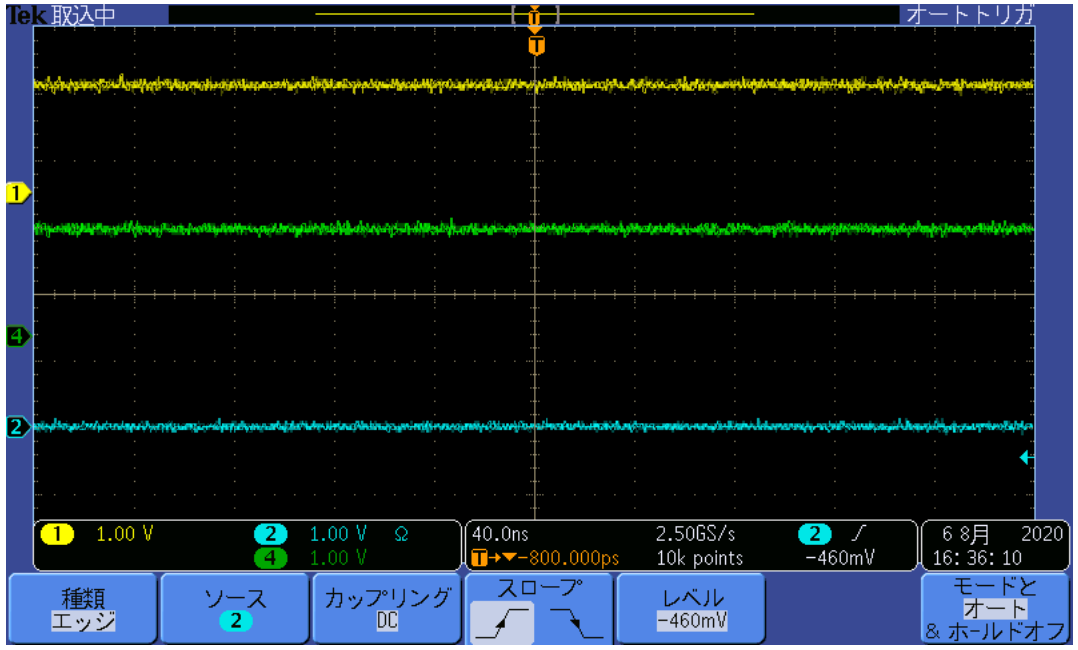


Detail: Data from FEM to ROC
Set l1 delay

good

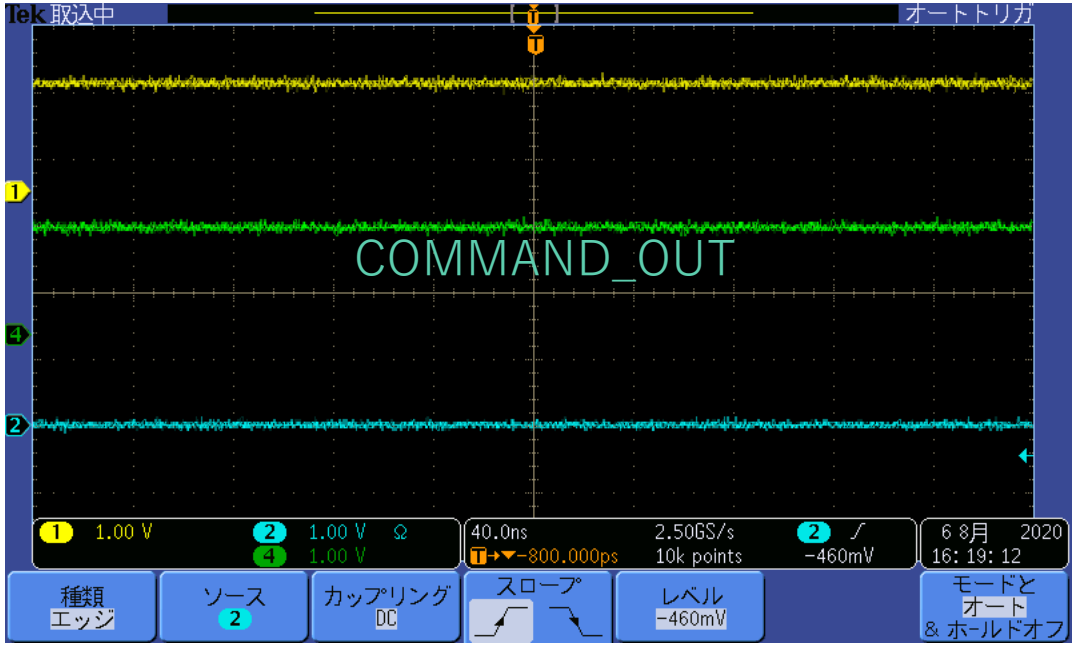


bad

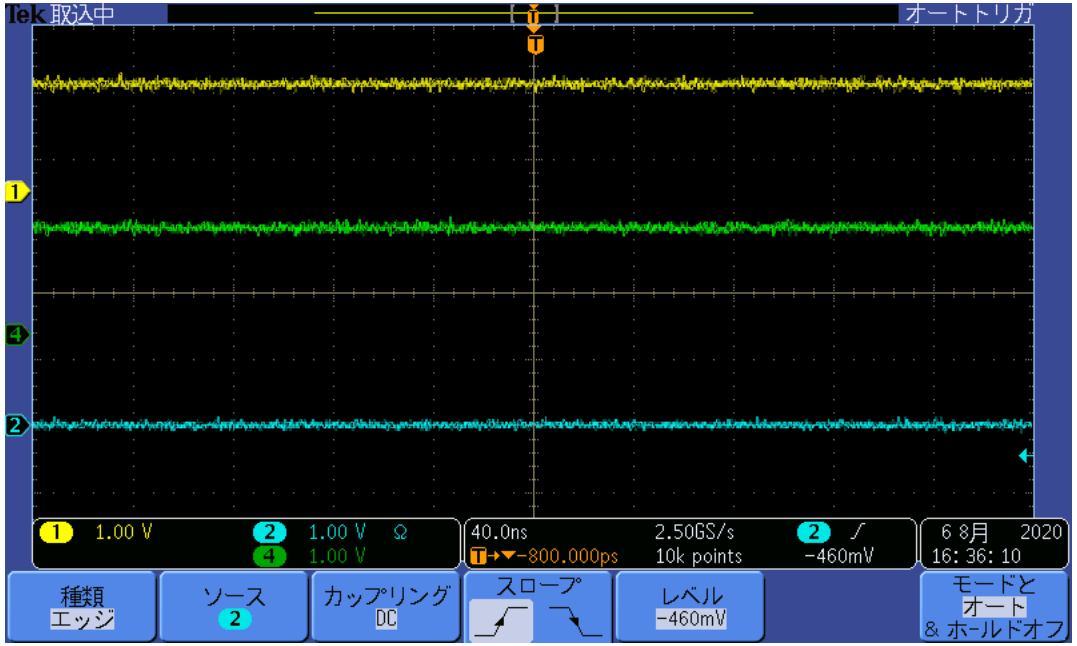


Detail: Data from FEM to ROC
Bco start

good

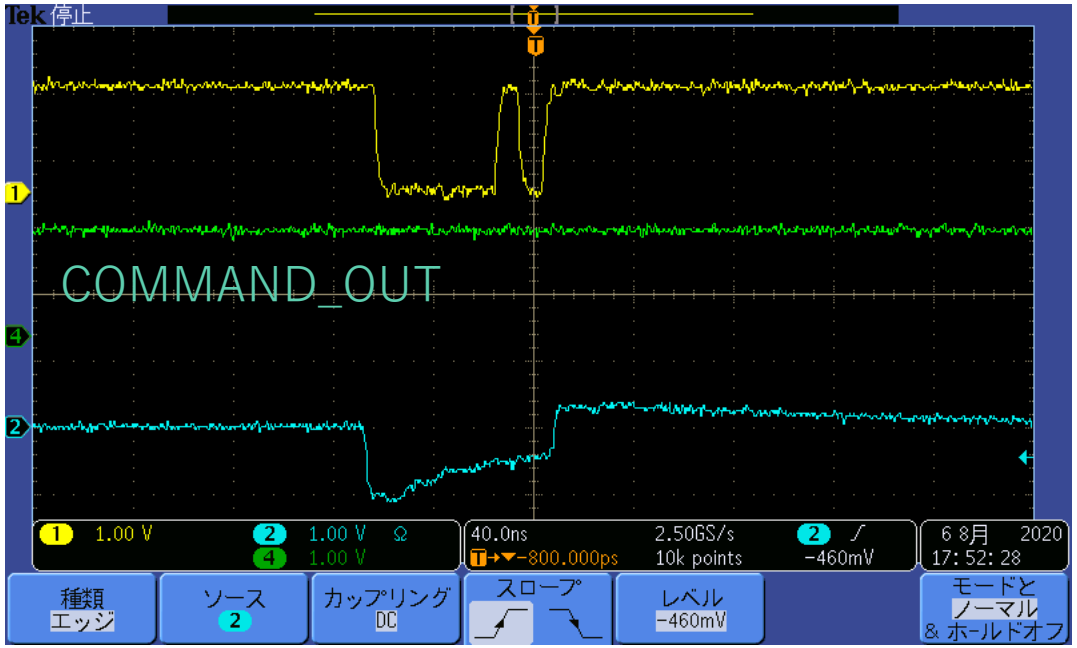


bad

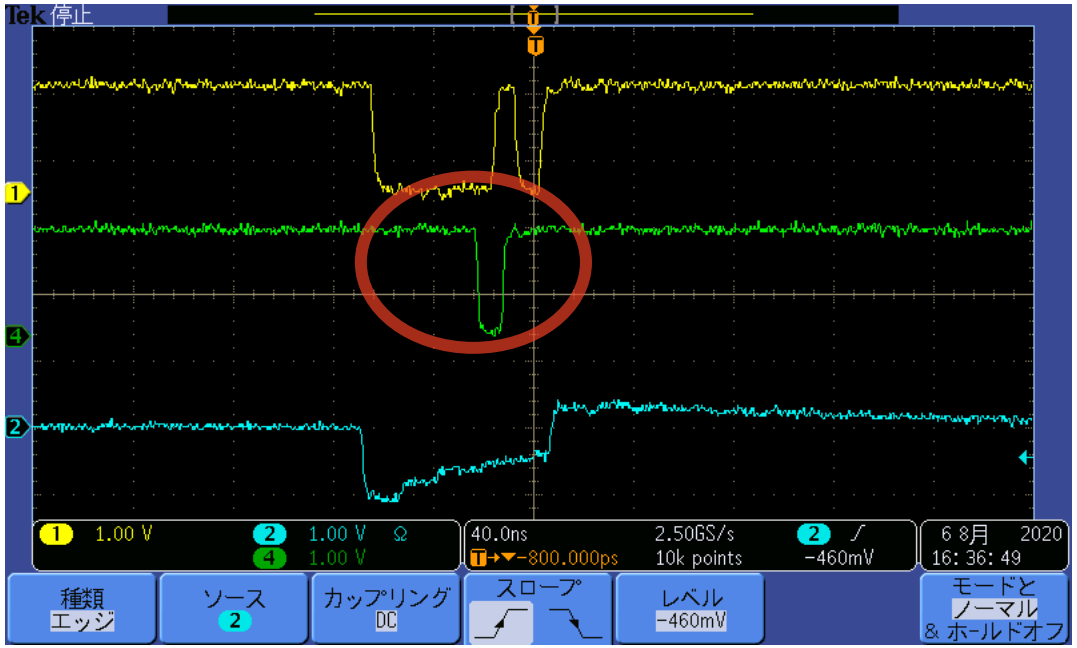


Detail: Data from FEM to ROC Calib

good

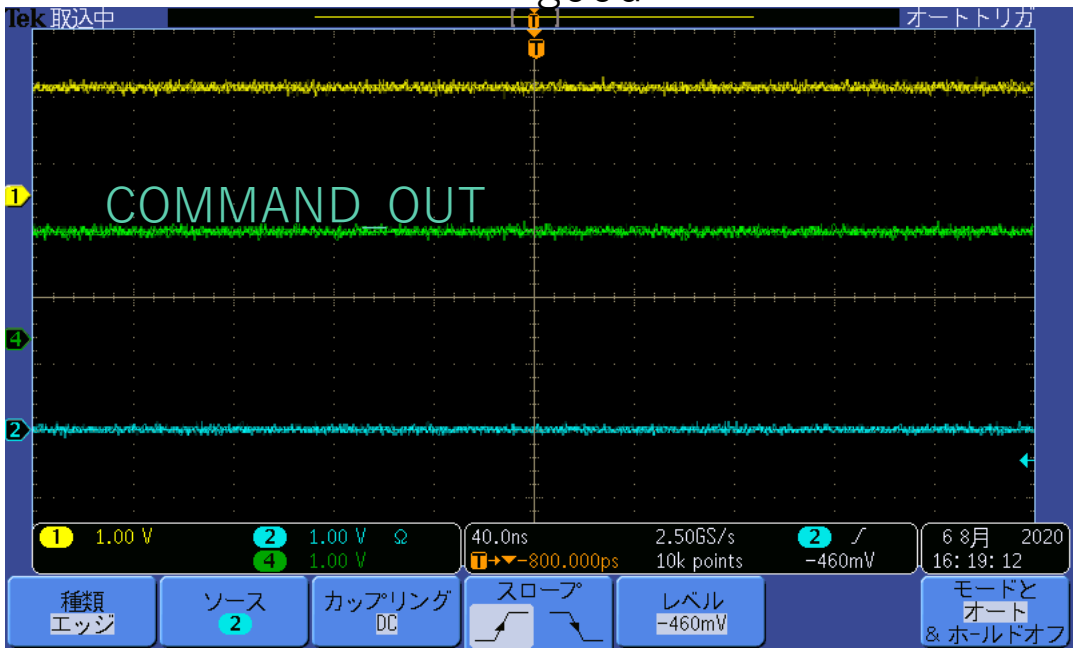


bad

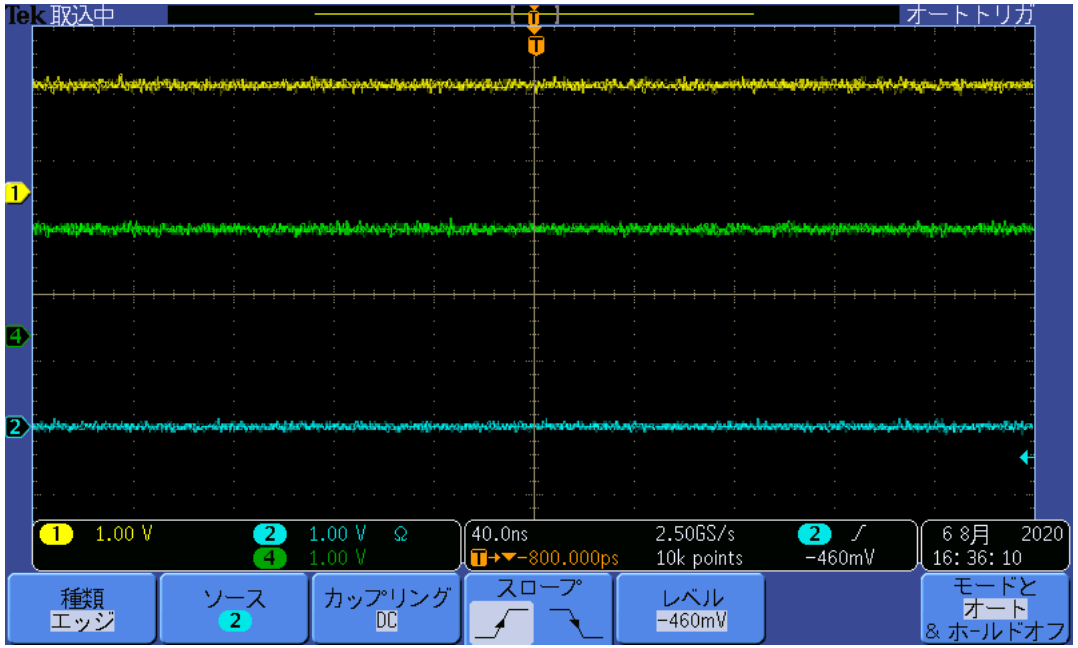


Detail: Data from FEM to ROC
Start DAQ

good



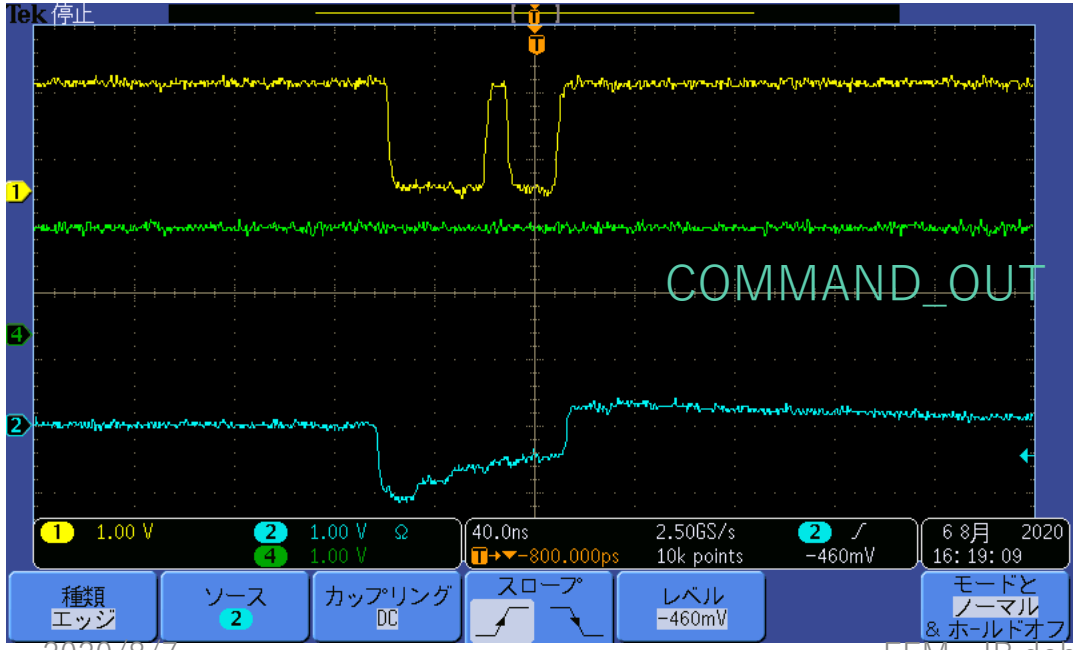
bad



Summary

- Commands' signals may break between FEM-IB and VME.
- Command signal is temporally drop off when we send command. (We expect that the signal must always be '1'.)

good



bad