INTT Full Readout Chain Performance

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Today's Report

About the measurement results
using testbench for INTT
by development of INTT and the Bus-extender

- Problem of Half Entry and Regulator
- Testbench Debugging
- Output Waveform
- Preparation of Source Test

Contents

- Problem of Half Entry and Regulator
- Testbench Debugging
- Output Waveform
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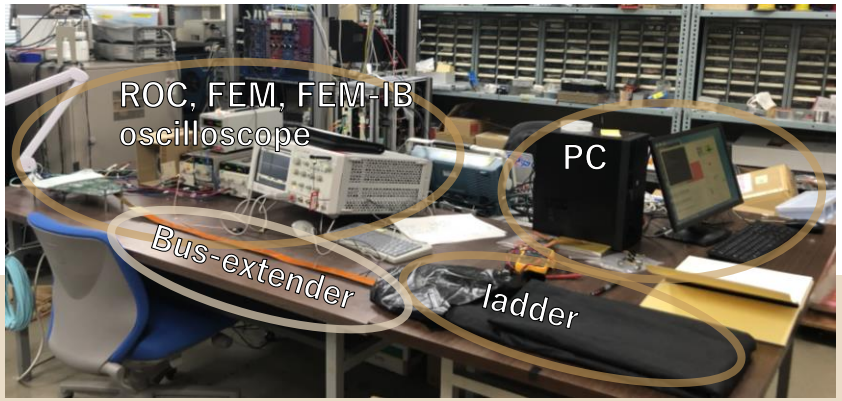
How to measure

Measurement using test pulse

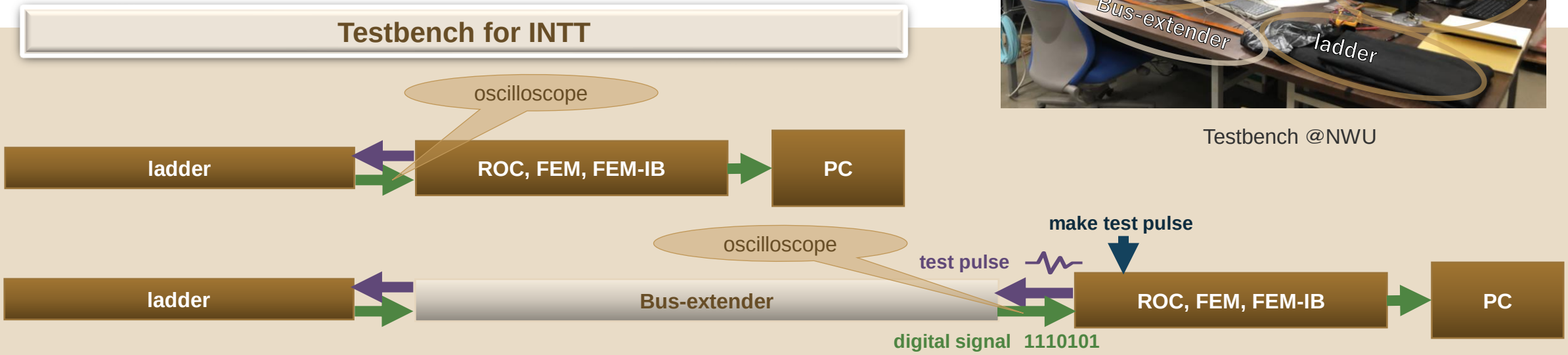
1. To receive data on PC
2. To observe digital output signal using oscilloscope

Bus-extender

Compare measurement ‘with Bus-extender’ with ‘w/o Bus-extender’

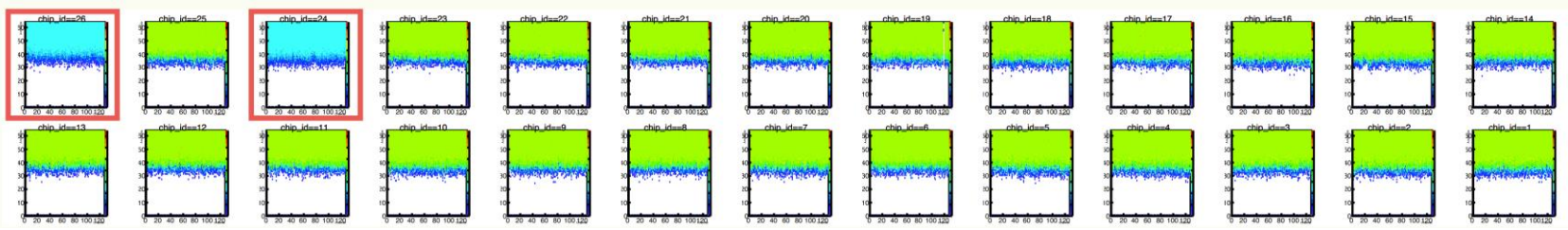


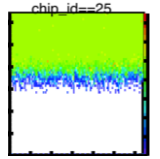
Testbench @NWU



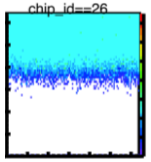
How to measure

1. To receive data on PC

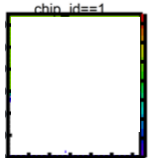




Good Result

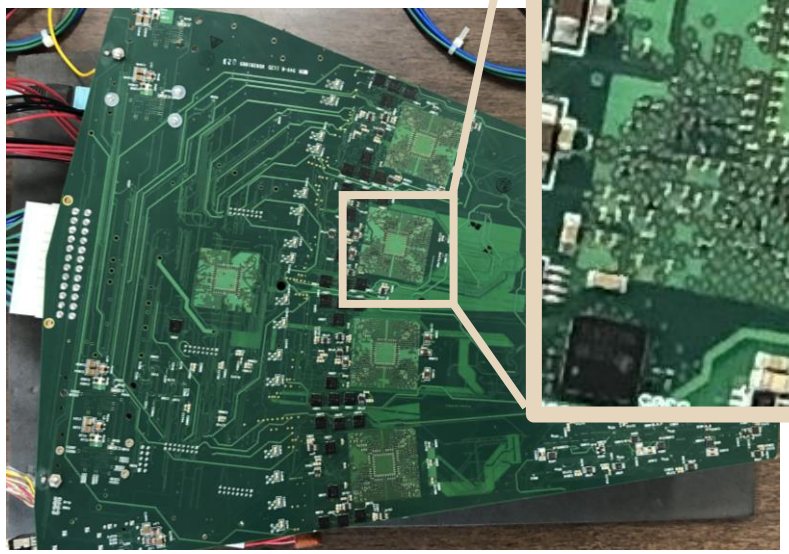


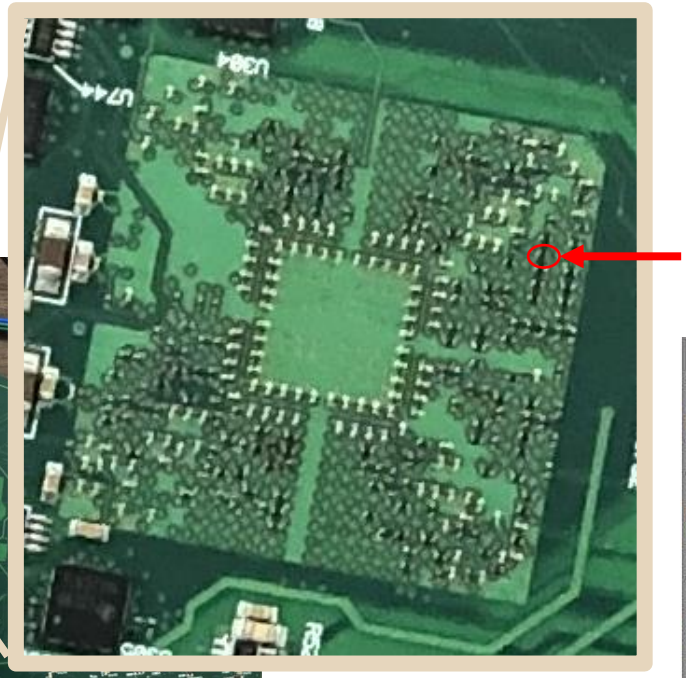
Half Result



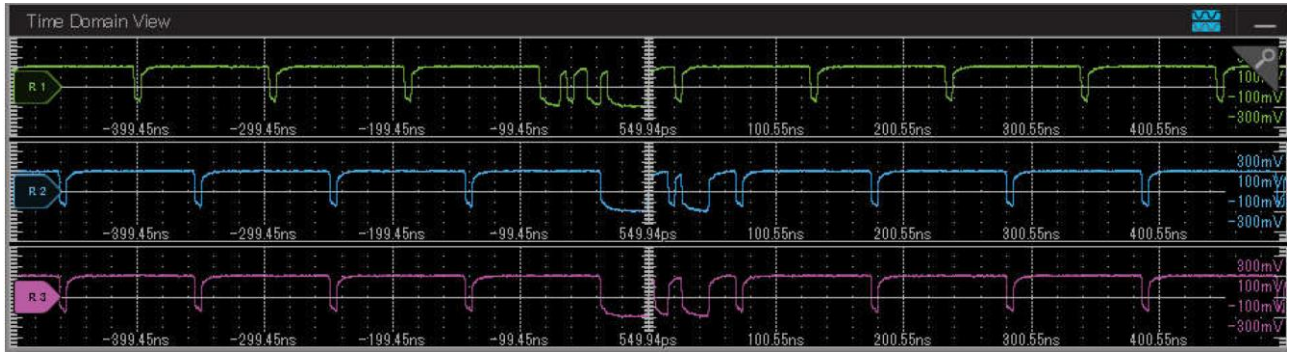
nothing

2. To observe digital output signal using oscilloscope





We observe output data signal with differential probe by oscilloscope.



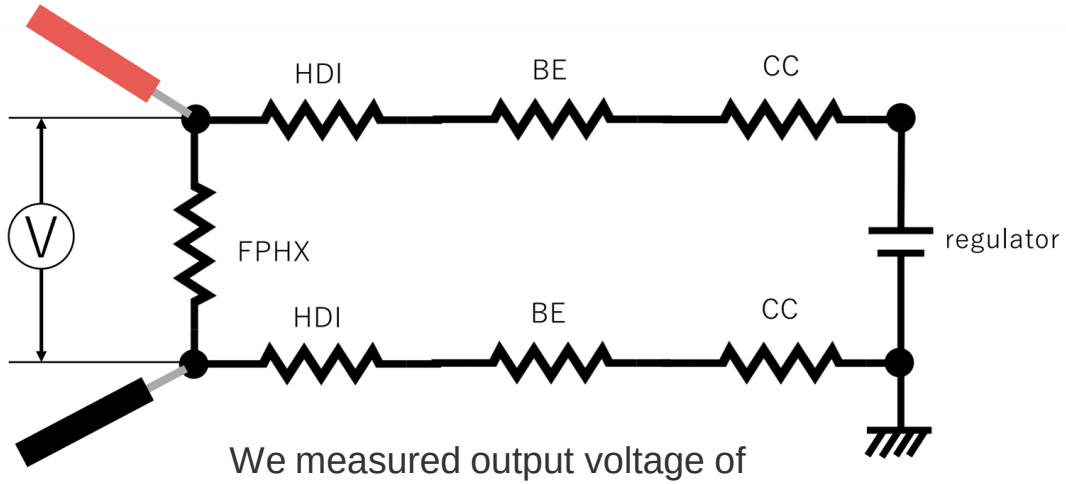
Output waveform measured with oscilloscope

Regulator

INTT

Voltage measurement for INTT with Bus-extender with 3.0V regulator (LVDS=8mA)

Chip	Line	Regulator out (Designed) (V)	Regulator out (Measured) (V)	Applied voltage (V)
14	Digital	3.0	3.005	2.841
14	Analog	2.8	2.812	2.729
26	Digital	3.0	3.005	2.838
26	Analog	2.8	2.812	2.688



We measured output voltage of regulator at FPHX chip with tester

FVTX

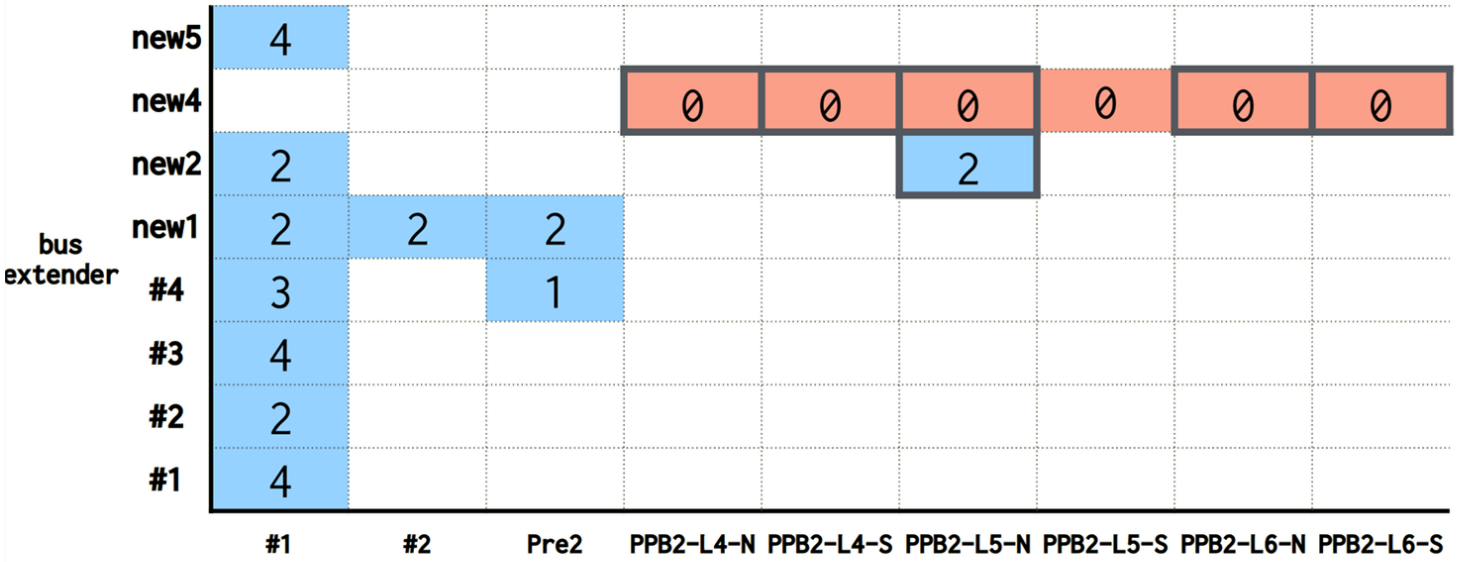
Voltage measurement for FVTX with 2.5 V regulator (LVDS=8mA)

Chip	Line	Regulator out (Designed) (V)	Regulator out (Measured) (V)	Applied voltage (V)
14	Digital	2.5	2.50	2.437
14	Analog	2.5	2.48	2.482
26	Digital	2.5	2.50	2.435
26	Analog	2.5	2.48	2.479

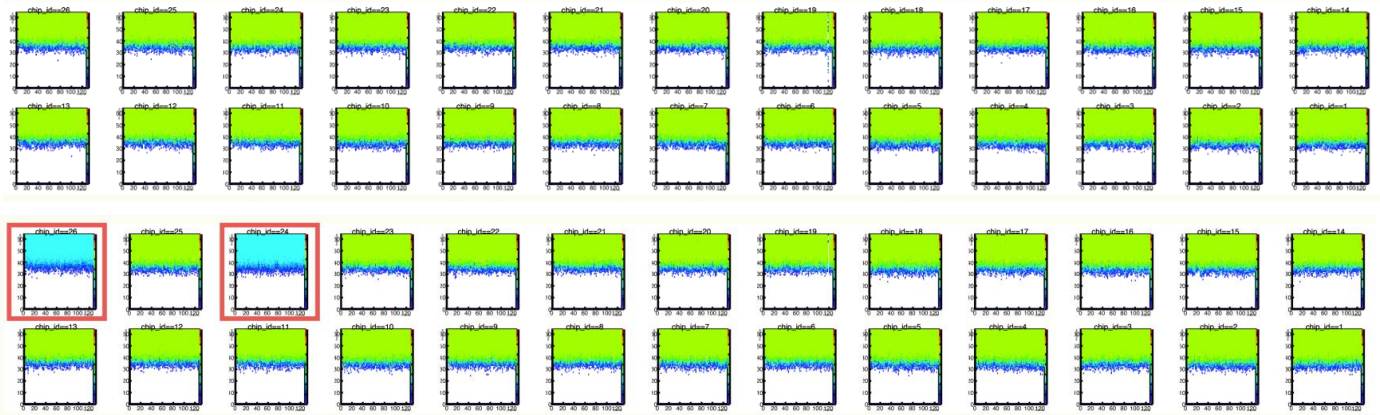
We have enough power supply using 3.0V regulator
FVTX was used in PHENIX so we were convinced that this result was sufficient.

Half Entry

#bad chips (x=ladder, y=bus ext.) with 3.0 V regulator



Bad means “half of expected entry”. **ladder**



We can see Good condition.
We could hardly see when we use 2.5V regulator.

We use 3.0V regulator but we have sometimes half entry chips.
The results didn’t change even if we use 3.3V regulator.

There are nothing bad chips(0).

There are two bad chips(2).

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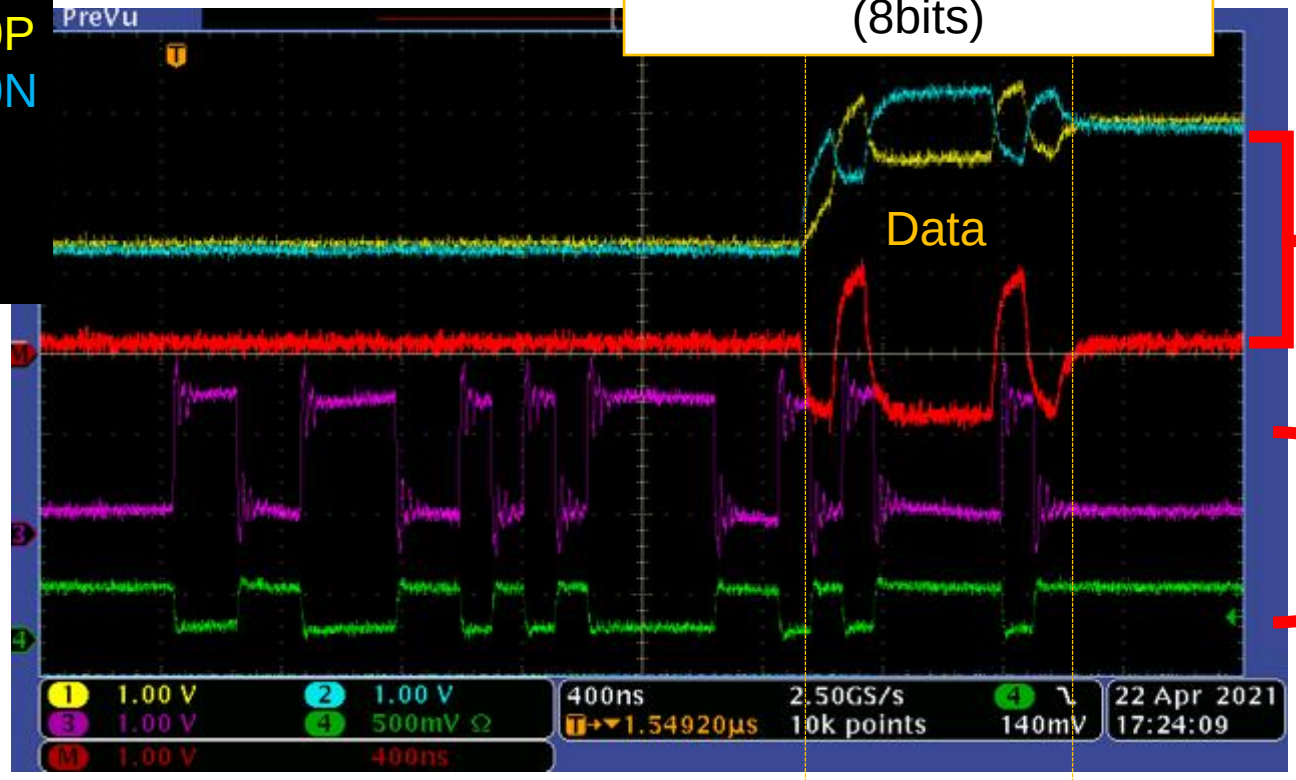
Observation of Register Readback 9

CH1: SC_OUT_0P
CH2: SC_OUT_0N
M: CH1-CH2
CH3: SC_IN_0P
CH4: SC_IN_0N



Readback Register Word (8bits)

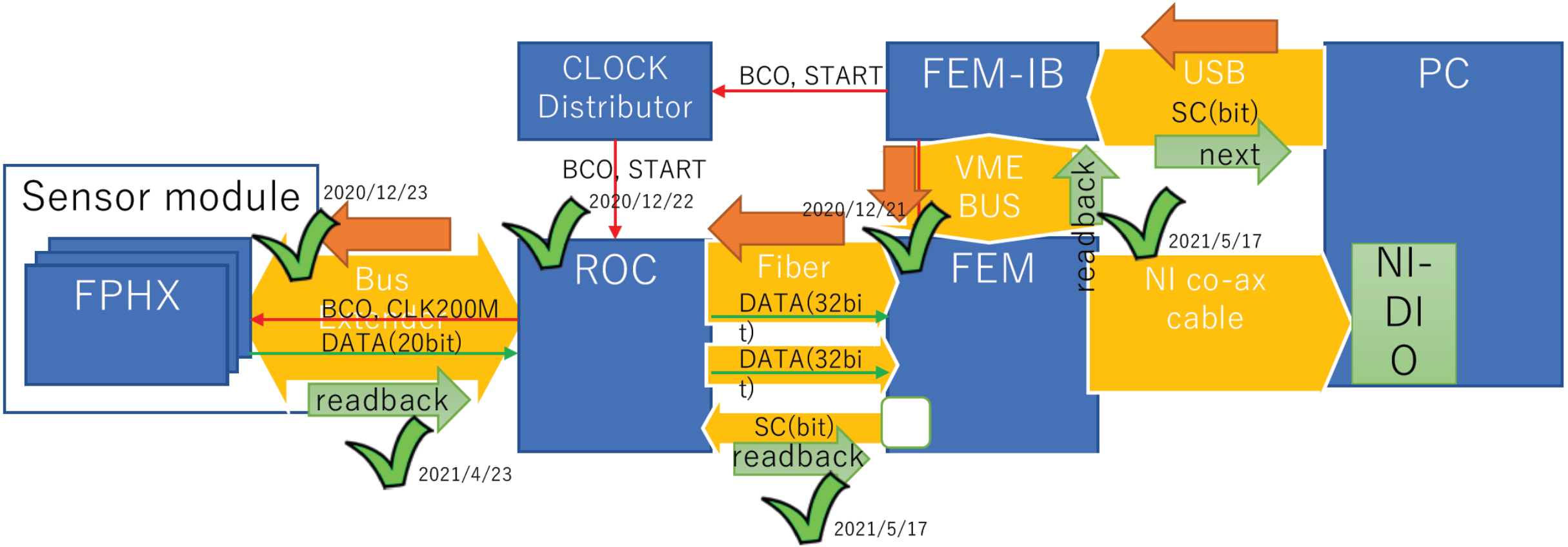
FPHX->FPHX Readback Register Word

ROC->FPHX Slow Control Command

Consistent pattern was observed.

GUI Setting				SC Word					
Module	Side	Chip	Gsel	Header*	Chip	Regist	instr	Data	Trailer
8	1	5	2	1100111	00101	01111	001	01000010	0000

Testbench Debugging



We can see good patterns as far as we currently measure.

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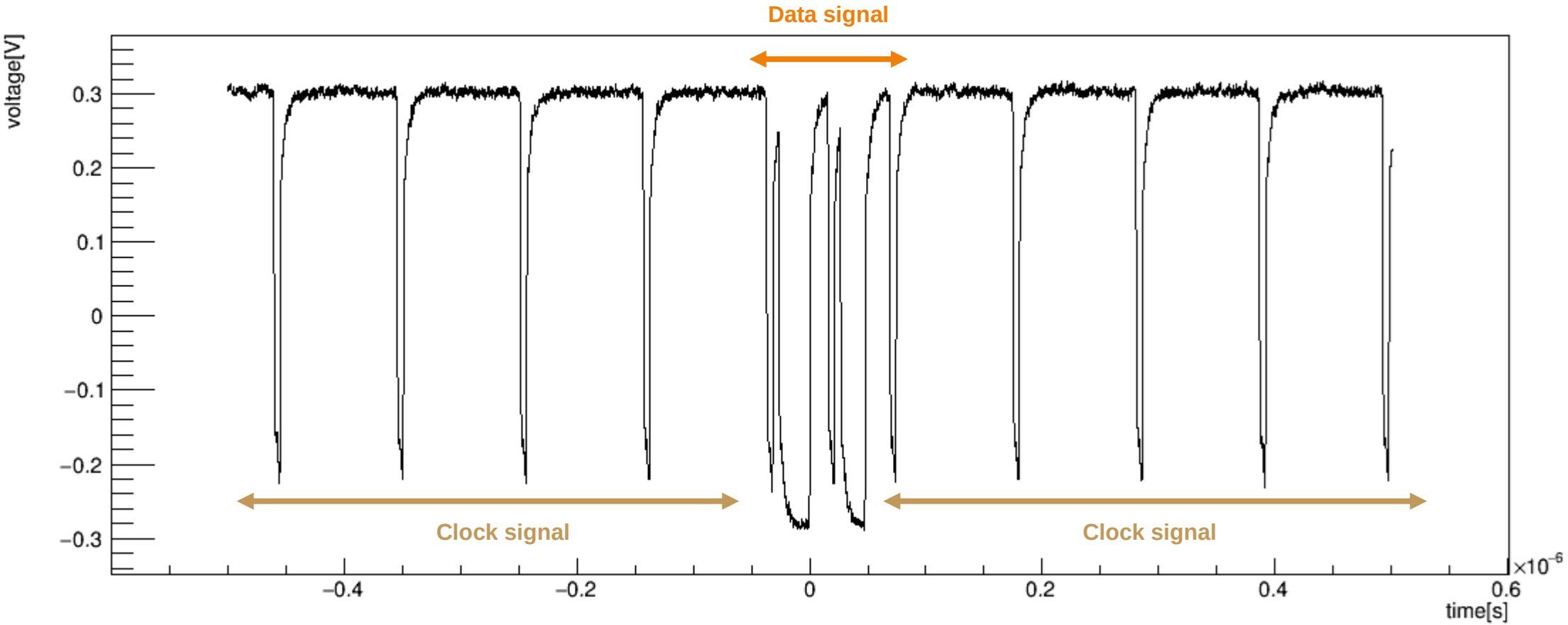
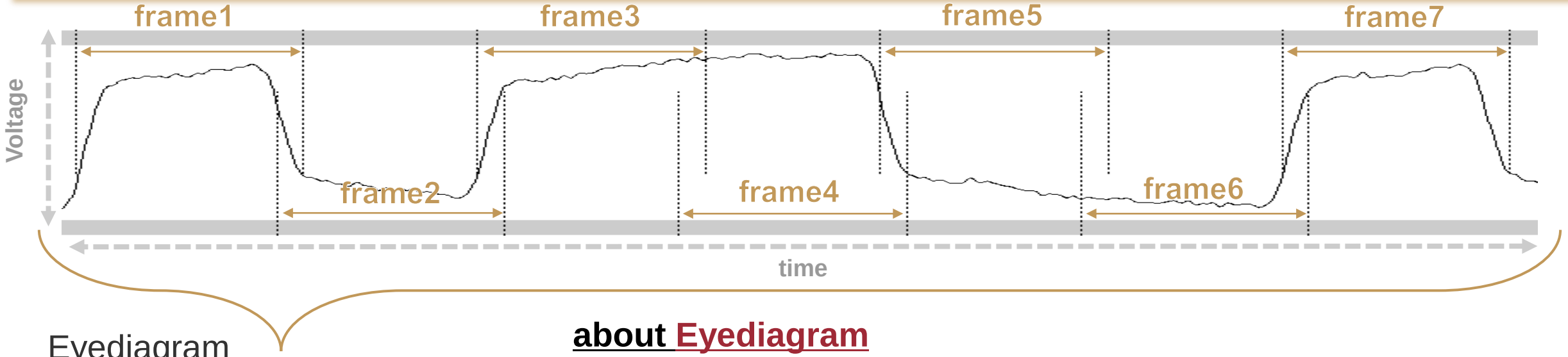
Output signal waveform

2. To observe digital output signal using oscilloscope

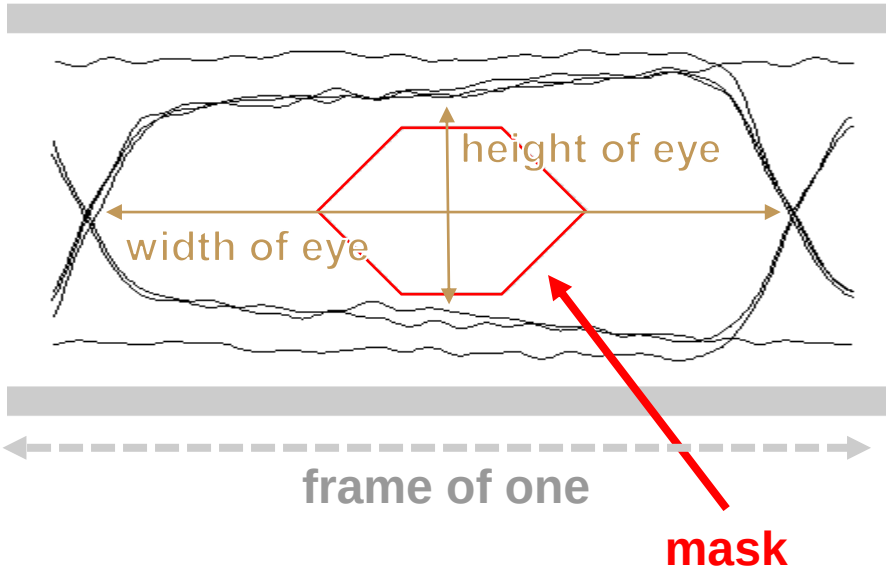
- This graph is output signal waveform w/o Bus-extender
- make eyediagram from this graph and analyze



About Eyediagram



Eyediagram



about Eyediagram

- **To visualize distortion of waveform when signal is sent**
- This is diagram to sample a lot digital signal waveform and show
  - It looks an eye ー＞「Eye」diagram
- We can evaluate voltage and margin of timing from eye height and width
- Mask indicate minimum height and width to need to judge correct data
  - We confirm weather signal observed touch mask
  - Mask is defined that error rate is lower than 10^{-12}

Compare low and high current 14

- There are low current in top, and high current in bottom.
- Left is w/o Bus-extender, and right is with Bus-extender.

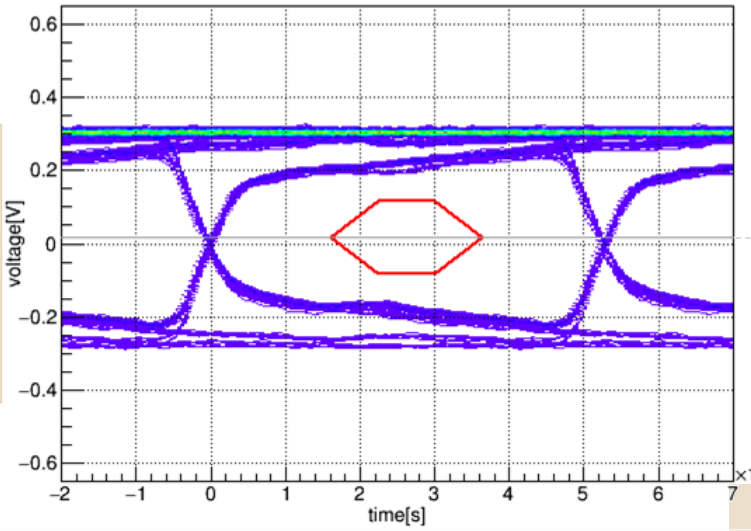
$$\text{Attenuation rate} = \left(1 - \frac{height\ of\ eye\ with\ BE}{height\ of\ eye\ without\ BE}\right) \times 100\ [\%]$$

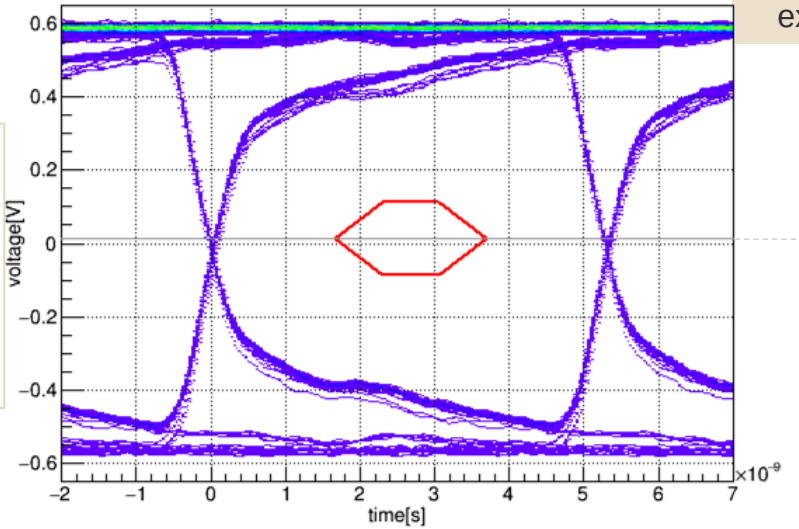
low

Height of eye
w/o 0.39 V
w 0.18 V
Attenuation rate
53.8%

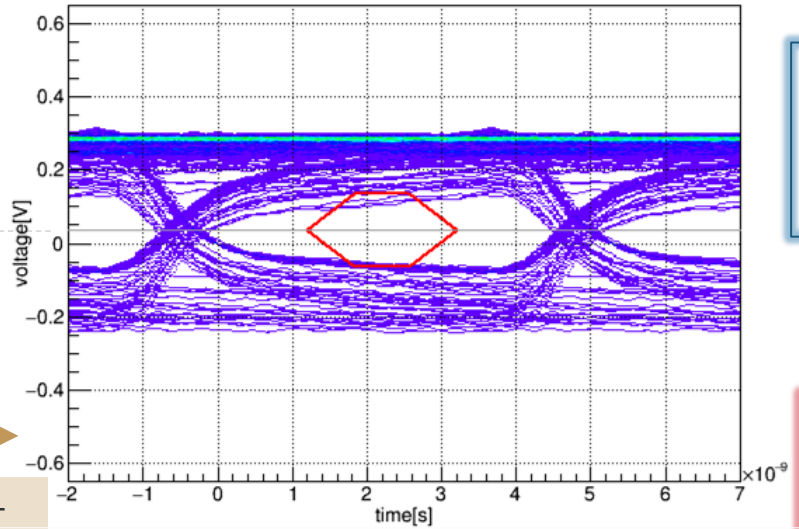
high

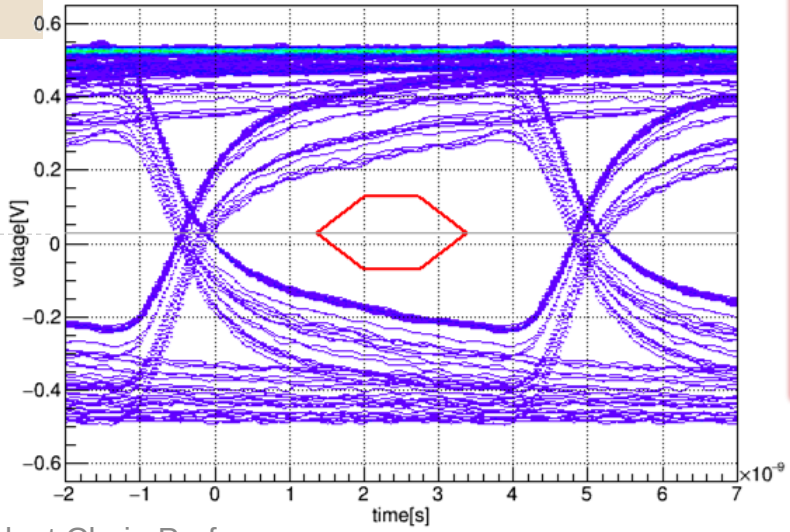
Height of eye
w/o 0.87 V
w 0.47 V
Attenuation rate
46.0%





Use Bus-extender





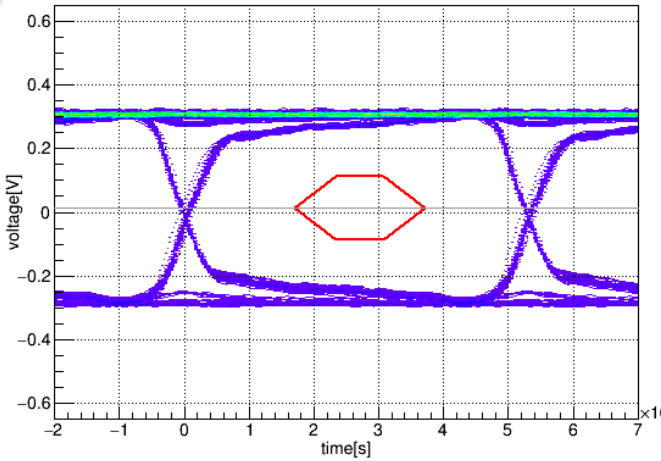
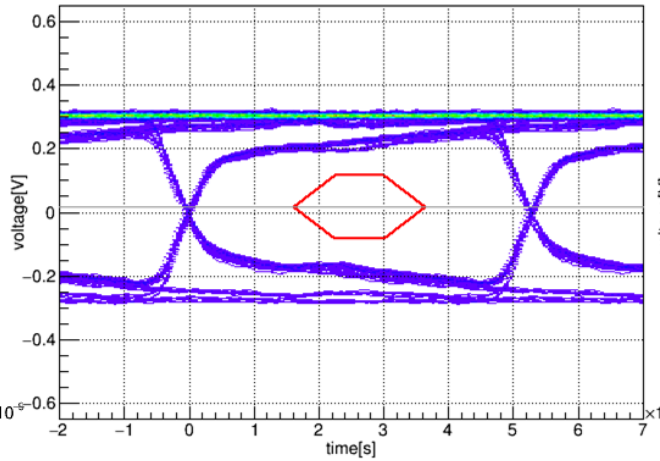
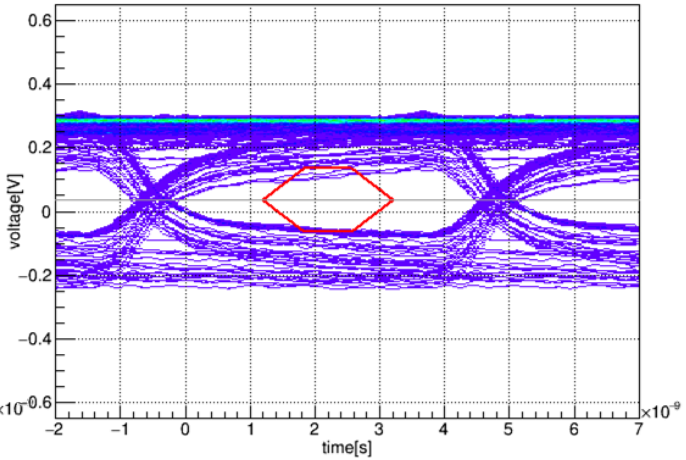
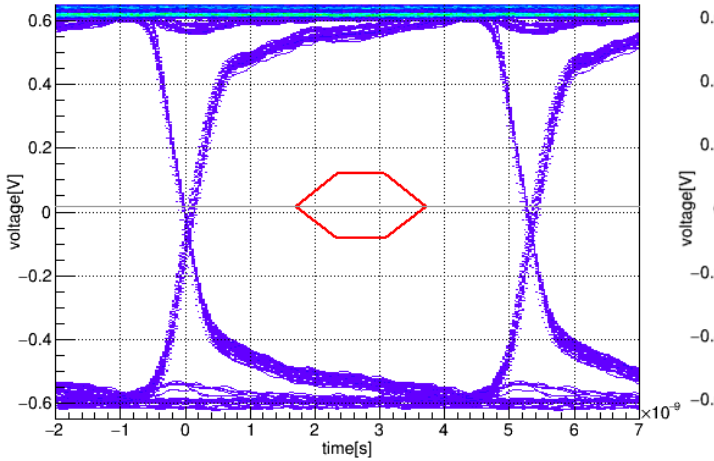
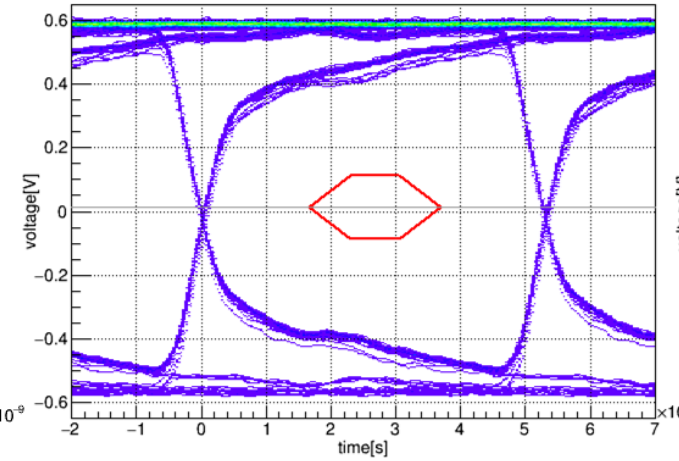
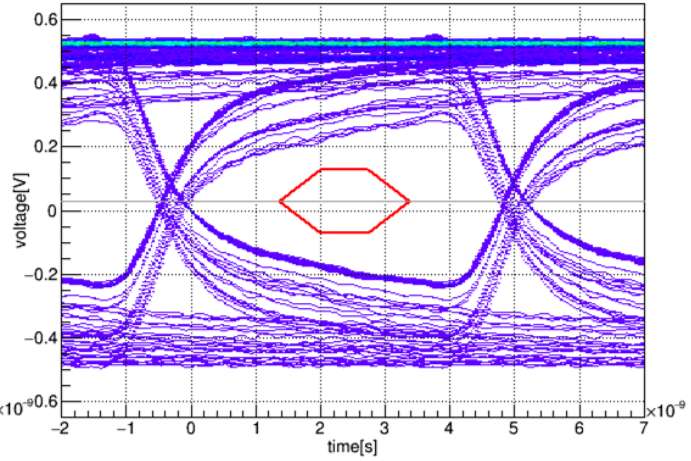
It's not enough when we use low current.

When we use high current, signal doesn't touch mask.

Attenuation rate of height of eye is less than 50%.

FVTX, INTT w/o, and with Bus-extender

It's distorted without Bus-extender comparing with FVTX

	FVTX	INTT w/o Bus-extender	INTT with Bus-extender
Low current			
High current			

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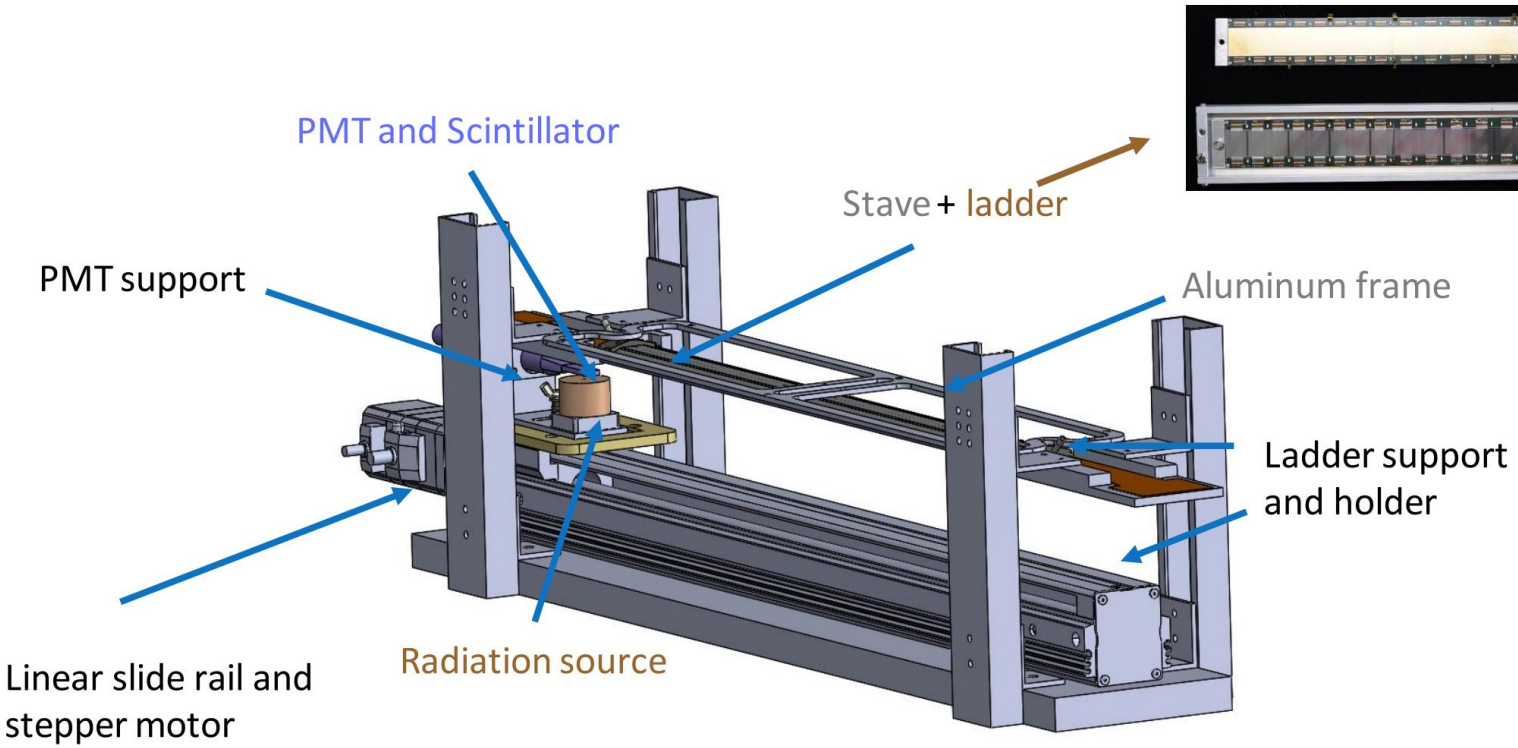
Preparation of Source Test

Source test fixture



We have ever measured source test at NWU so the updated measurement can be started as soon as the fixture is received.

Summary

- 3.0V regulator has enough voltage.
- However, there are sometimes half entry chips.
- Testbench debugging results is good at present.
- Output waveform from INTT is distorted.
- We are ready to measure source test.

Next Schedule

- To proceed with debugging
- To measure output waveform from INTT again with the updated Bus-extender and 3.0V regulator at the end of this month
- To begin source test after receiving fixture

Back Up