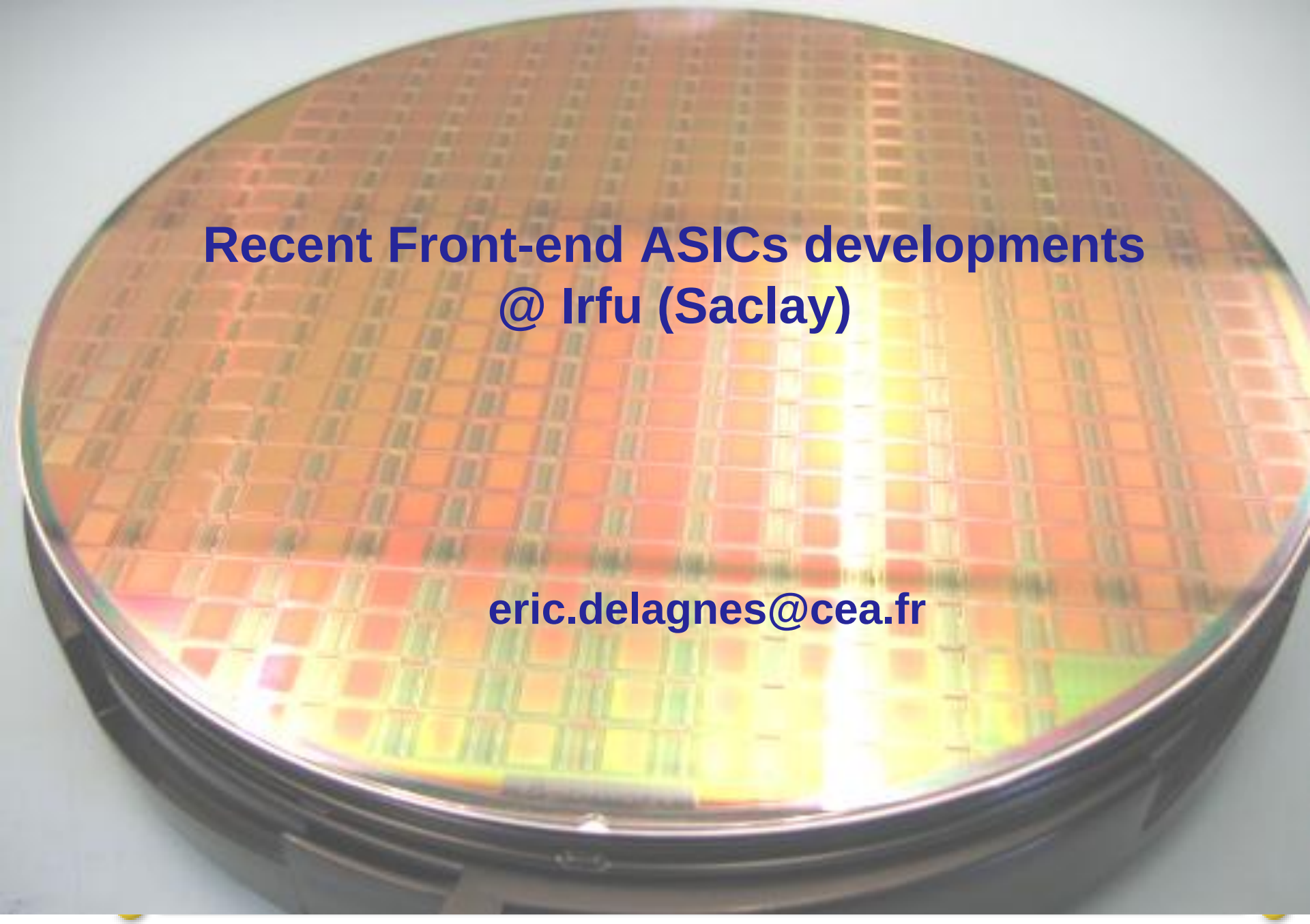


Recent Front-end ASICs developments @ Irfu (Saclay)

eric.delagnes@cea.fr

Outline

- Introduction
- FE chips for semiconductor detectors
- FE chips with analogue memory
- Ultra-fast analogue memories
- Future R&D

FE electronics group @ Irfu

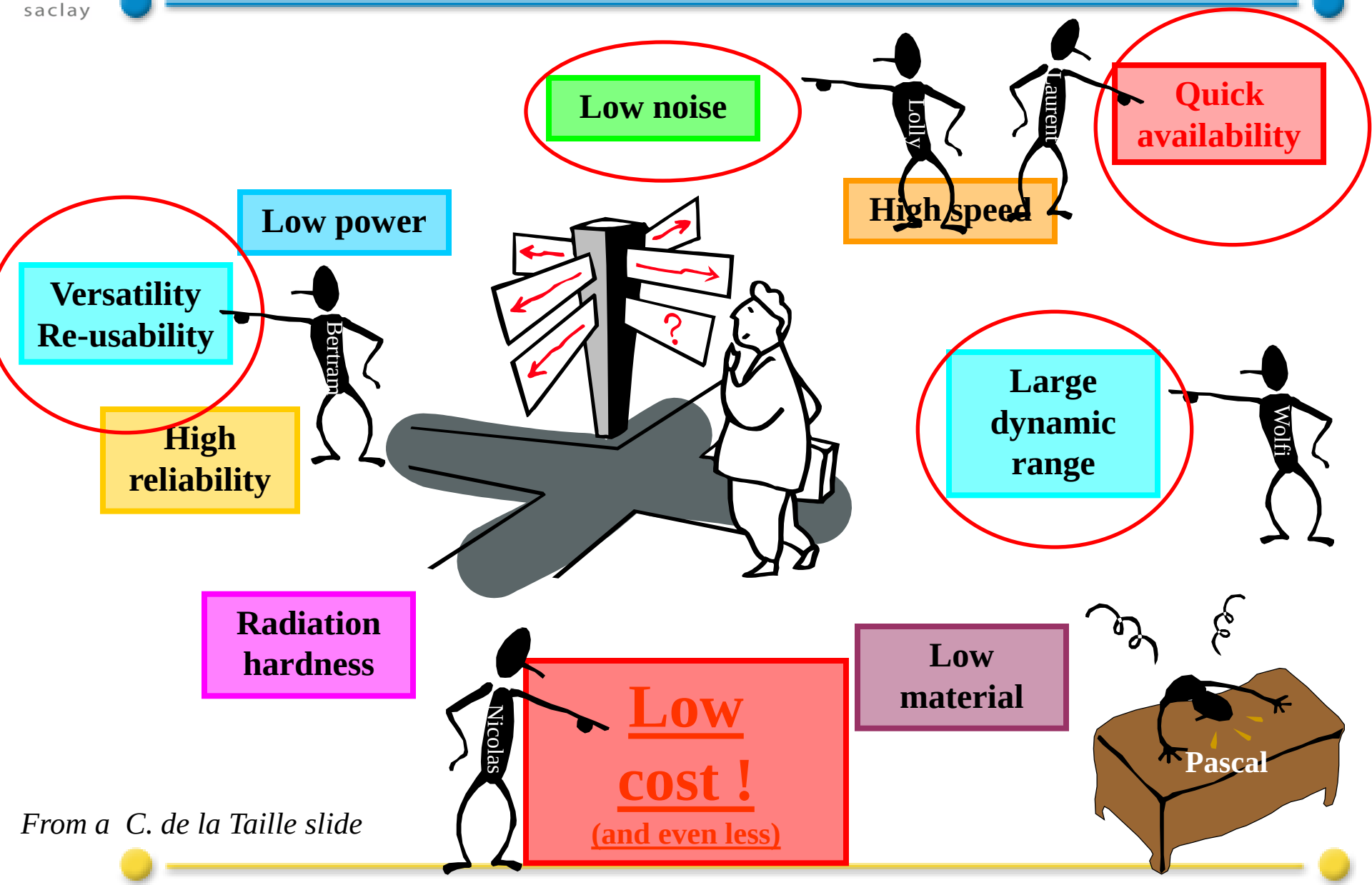
- Originally created in 1990 for LHC.
- Now working for all the physics divisions of Irfu (HEP, Nuclear Physics, Astrophysics (ground & space)).
- Cross Fertilization between projects.
- 400000 channels operating worldwide (100000 chips)

- 6 permanent microelectronics designers + 1 PhD +1 external collaborator.
- 5 electronics technician/engineers.
- 4-5 ASICs designed in parallel.

- Very strong interaction with the acquisition group (TRAPS) of Dr Denis Calvet: Asic seen as a part of the system and not as its heart.

  => joint teams on projects.

The Front-end electronics designer puzzle



From a C. de la Taille slide

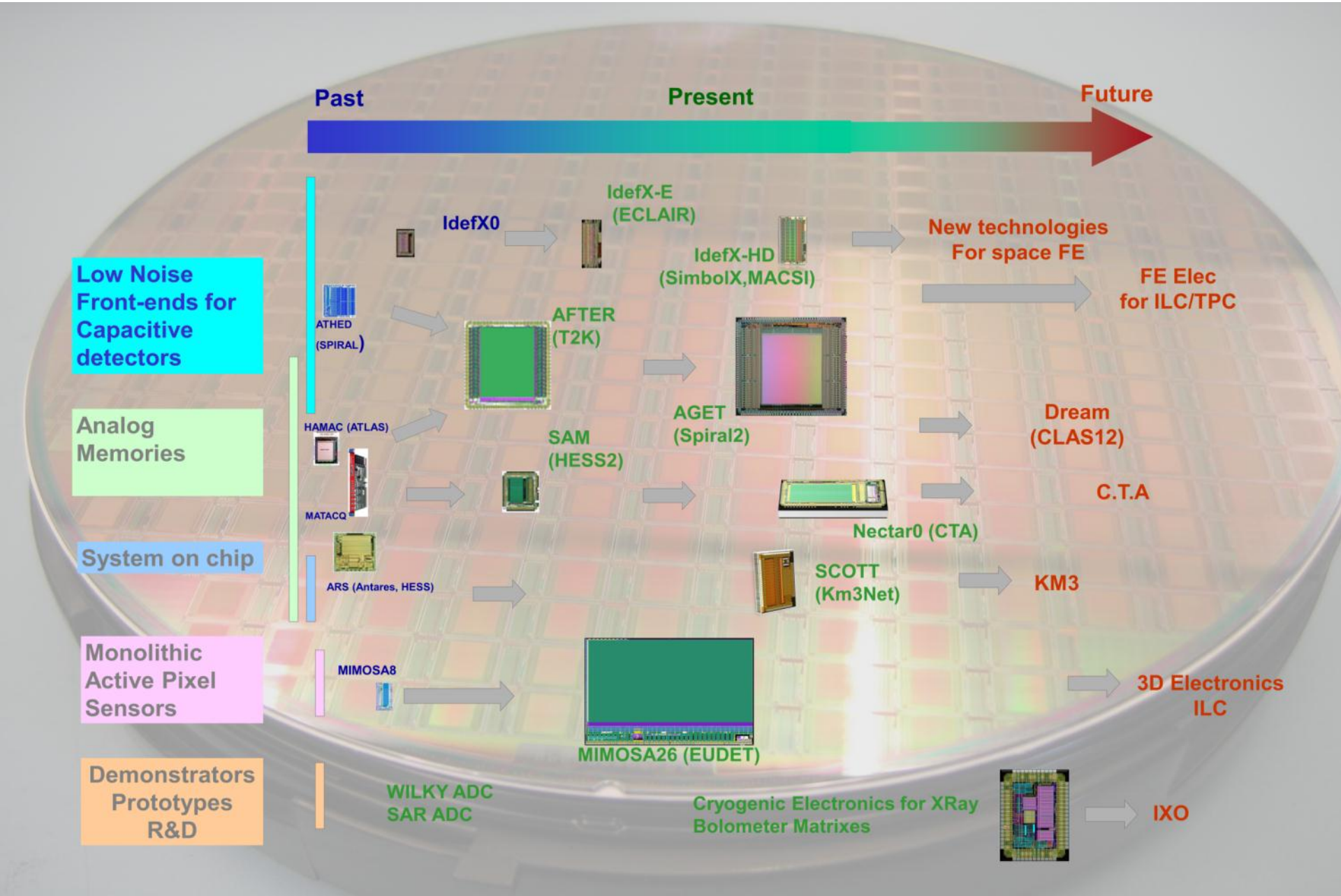
Philosophy & Technology:

- **Our Philosophy => Fast Design for high performances.**
  - **Not waste time testing several technologies or tools.**
  - **Conservative approach**

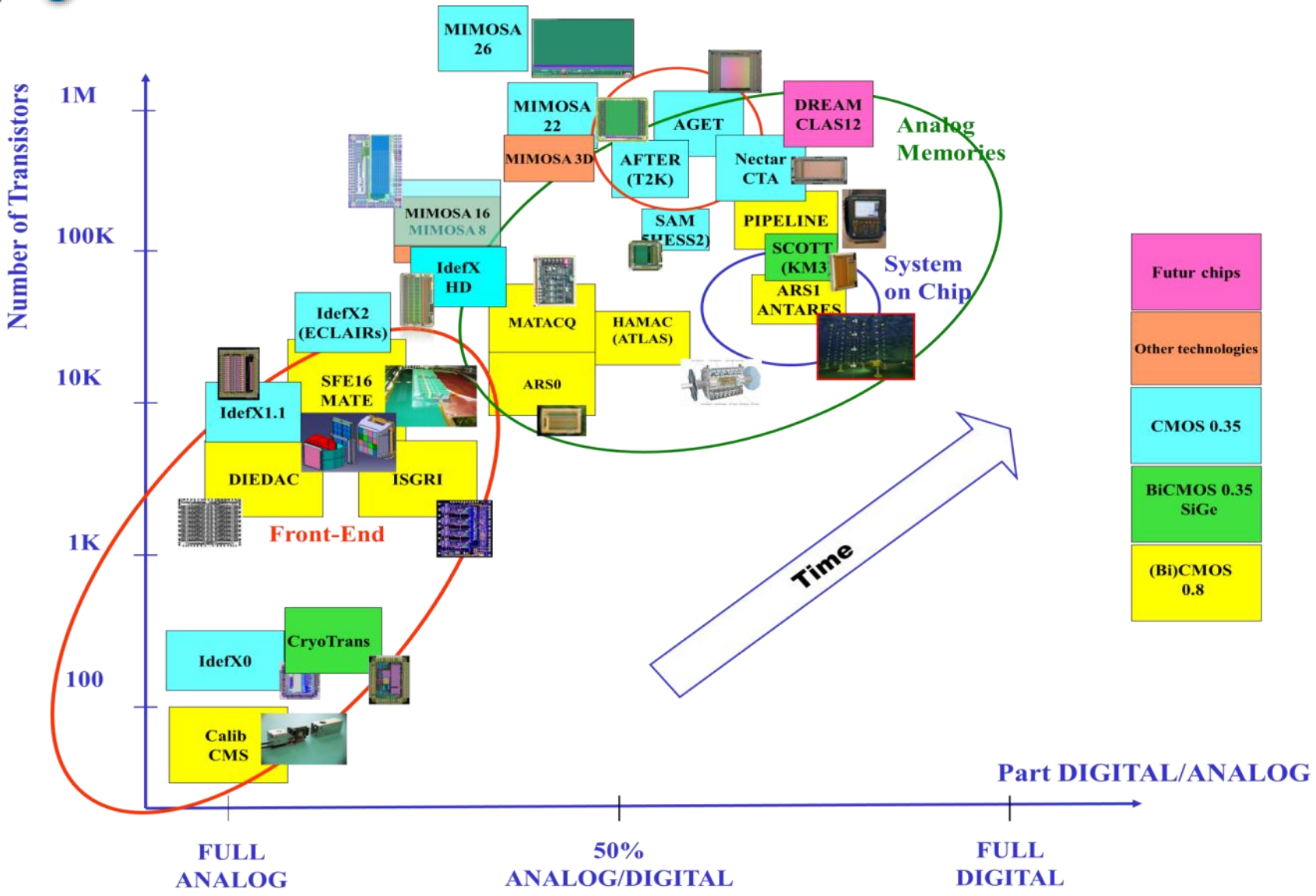
- **During the 6 last years , efforts mainly concentrated on one technology:**
  - **AMS 0.35 µm (Bi)CMOS :**
    - **Low cost.**
    - **Good Analogue technology.**
    - **Fast manufacturing time. Reliable.**
    - **Behavior in space environment well known.**
    - **Reuse of blocks**
  - **Some experience with TSMC 0.25µm and Tezzaron/Chartered 0.13µm 3D technology.**

- **Evaluation of next technology node in progress (0.13µm IBM or Chartered, 0.18µm XFAB or AMS…)**
- **Several ways to access to foundries at the best conditions : MPW, « private MPWs», engineering dedicated runs.**

Asic ROADMAP @ Irfu

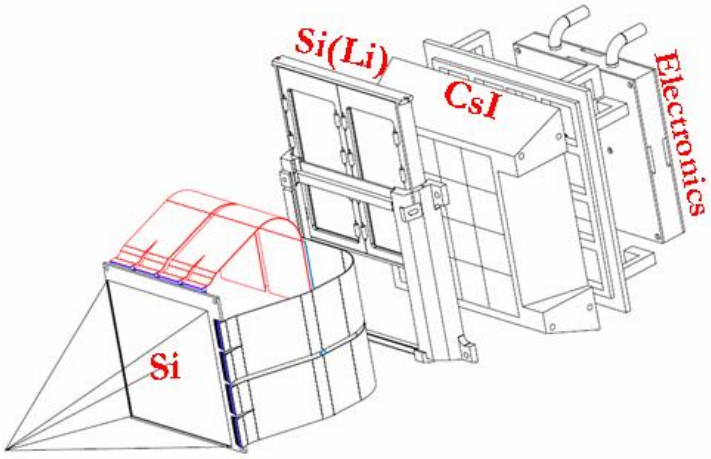


Chip Evolution: bigger & more digital



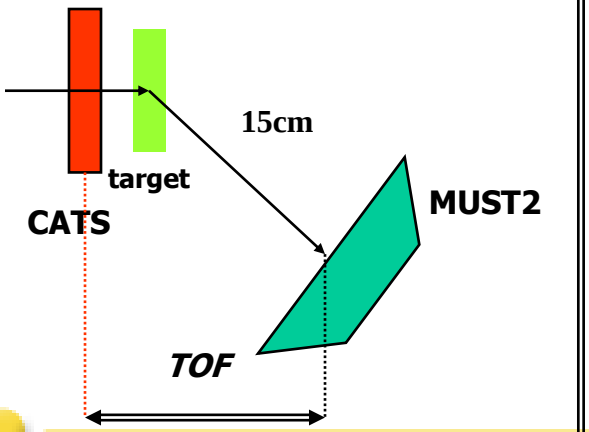
MUST2 : an hodoscope for SPIRAL at Ganil

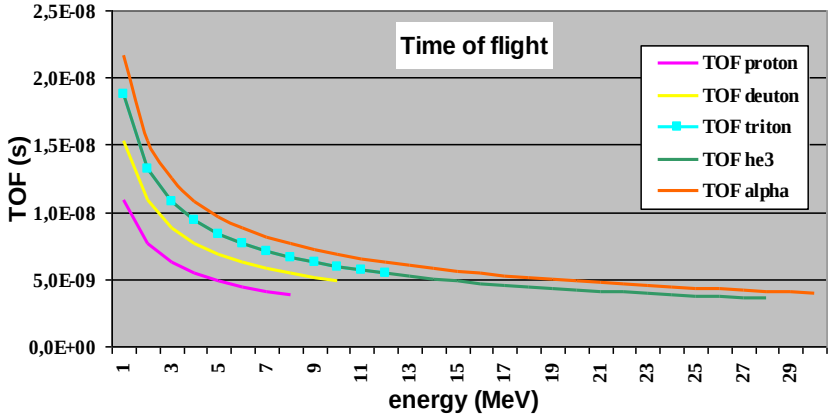
- **Goal:** For nuclear physic Study of nuclei far away from the valley of stability
- **Tools:** hodoscope MUST2 with a large solid angle coverage (2.6sr) = 6 telescopes
- **Purpose:** Identification of the particles (proton, deuteron, … alpha), Energy and Position
- **Collaboration with IPNO & GANIL**



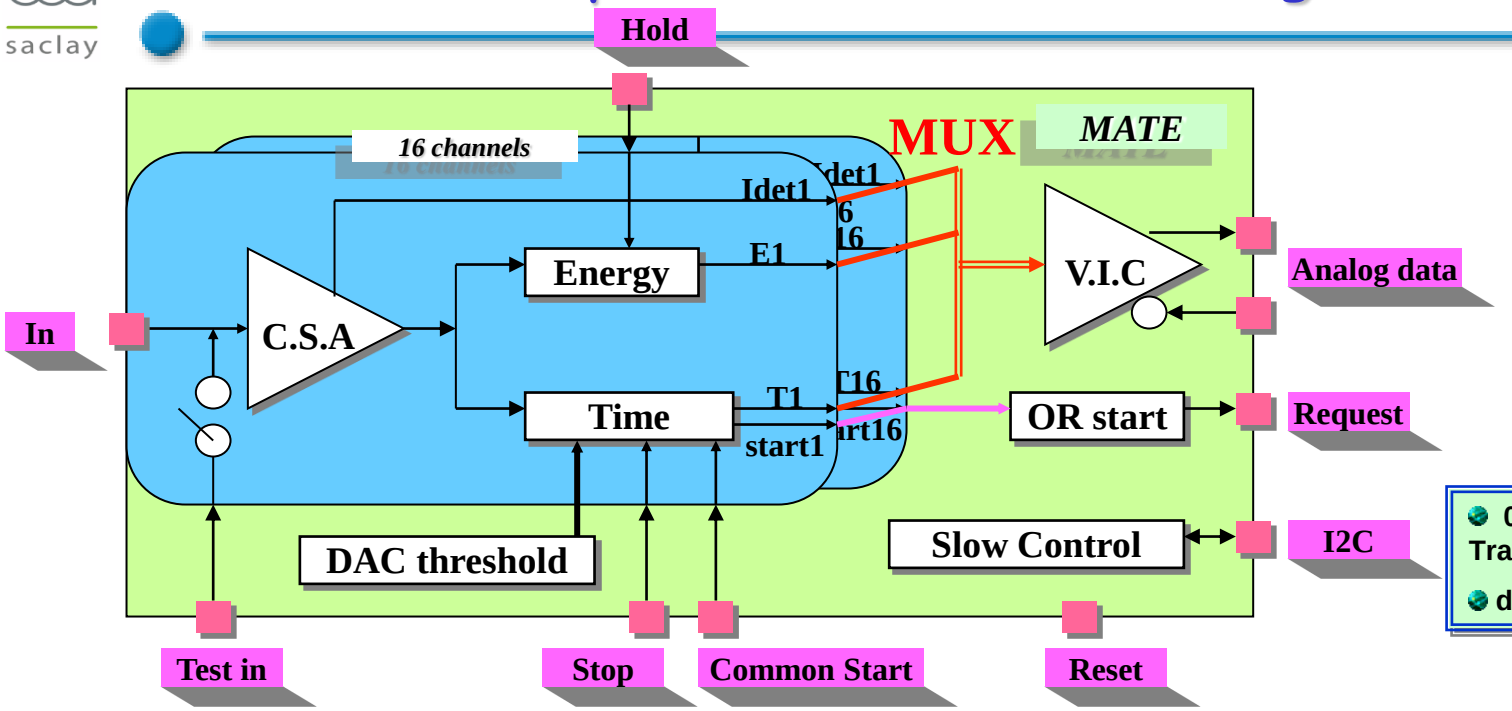
One single Asic (MATE): energy & time measurements for the three kinds of detectors with multiplexed output. Configuration by slow control

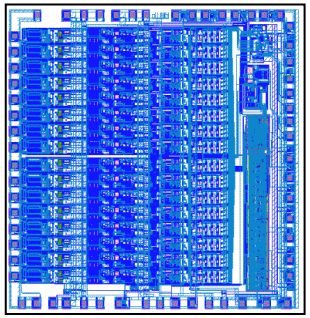
Time of fligth measurement





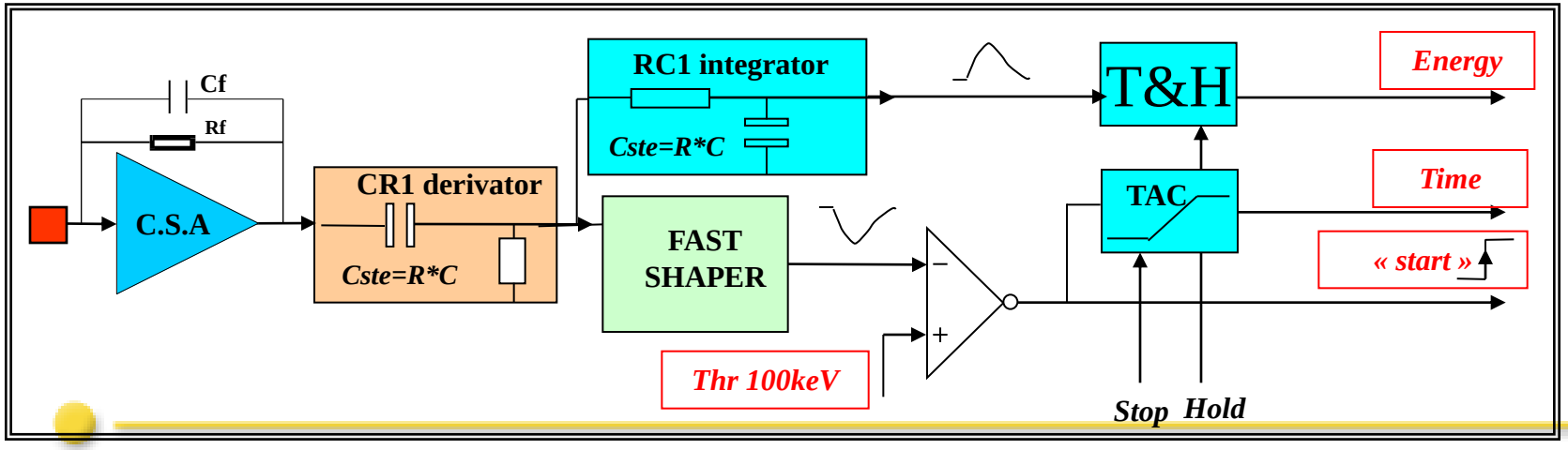
The MATE chip: 16 channels measuring time & energy



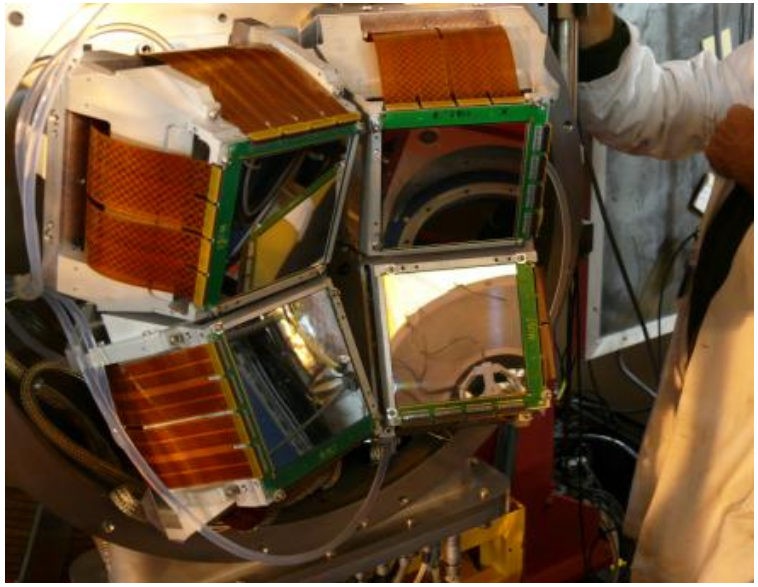


- 0.8µm BiCMOS AMS 16000 Transistors;
- die area 6 mm x 6 mm;

- **Sketch of one channel**



MATE : Summary & measured performances



- I2C slow control
- Optimized for Si Cd=68pF. IL=20nA
- 16 Channels (Time & Energy)
  - Energy (both polarity)

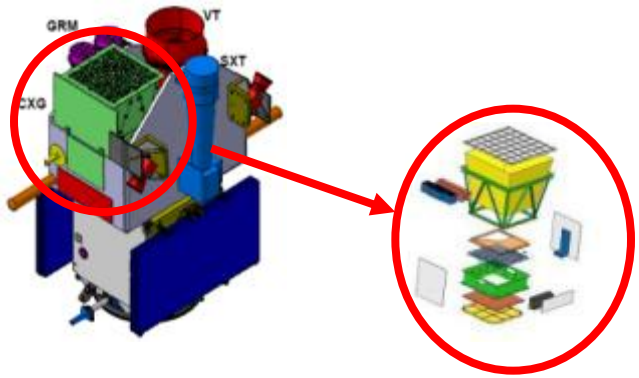
range	Si	SiLi
Shaping time (µs)	1	3
Range (MeV)	+/-50	250
Resolution (keV FWHM)	16	95

  - Time (TAC)
    - σ = 250 psec rms @ 6 MeV proton
- Serial output 2 MHz
- 28mW/channel

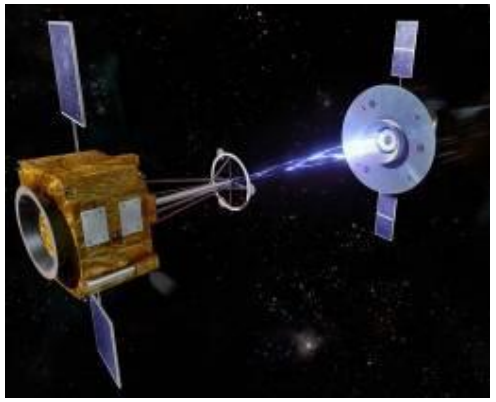
ATHED: improved MATE with higher dynamic range option used in the MUSET detector.

ASICS for CdTe Spaceborn CdTe Spectro-cameras:2 targets

- ECLAIRs/SVOM : Franco-Chinese satellite to study of gamma ray bursts
  - CXG gamma camera using coded mask
  - 6400 CdTe detectors, 200 asics.
  - **CdTe schottky 4x4mmx1mm**
    - **4-200 keV range**
    - **2.5mW/channel**



- Simbol X: Hard Xray observation of galactic center
  - Based on 2 satellites (mirror + focal plane):16000 pixels, 500 asics.
  - **Pixellated CdTe detector (500µm pitch)**
    - **FWHM=1% à 2% @ 60keV**
    - **4keV-80keV range**
    - **<1mW/Channel**
    - **Simbol-X aborted in 2010.**
    - **But Asic & microcamera proposed for 4 other projects**

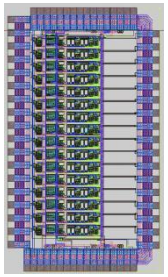


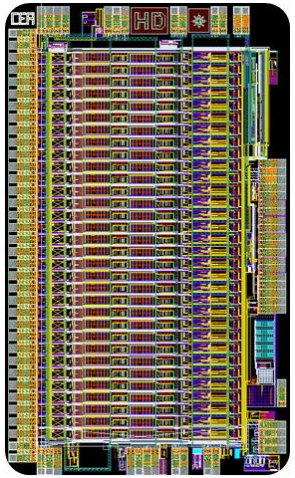
The Idef-X Family

COMMON BASIS => Idef-X family:

- **For low or very low capacitance detectors (CdTe , but also Si & LXe TPC*)**
- **Same CSA, PZ, Filter, (discriminator, peak detector) architecture**
- **Detector leakage current compliant.**
- **Use of a custom digital library for latchup free design.**
- **technology tested for space environment: AMS 0.35µm**

(*) D. Thers @ Subatech (Nantes)





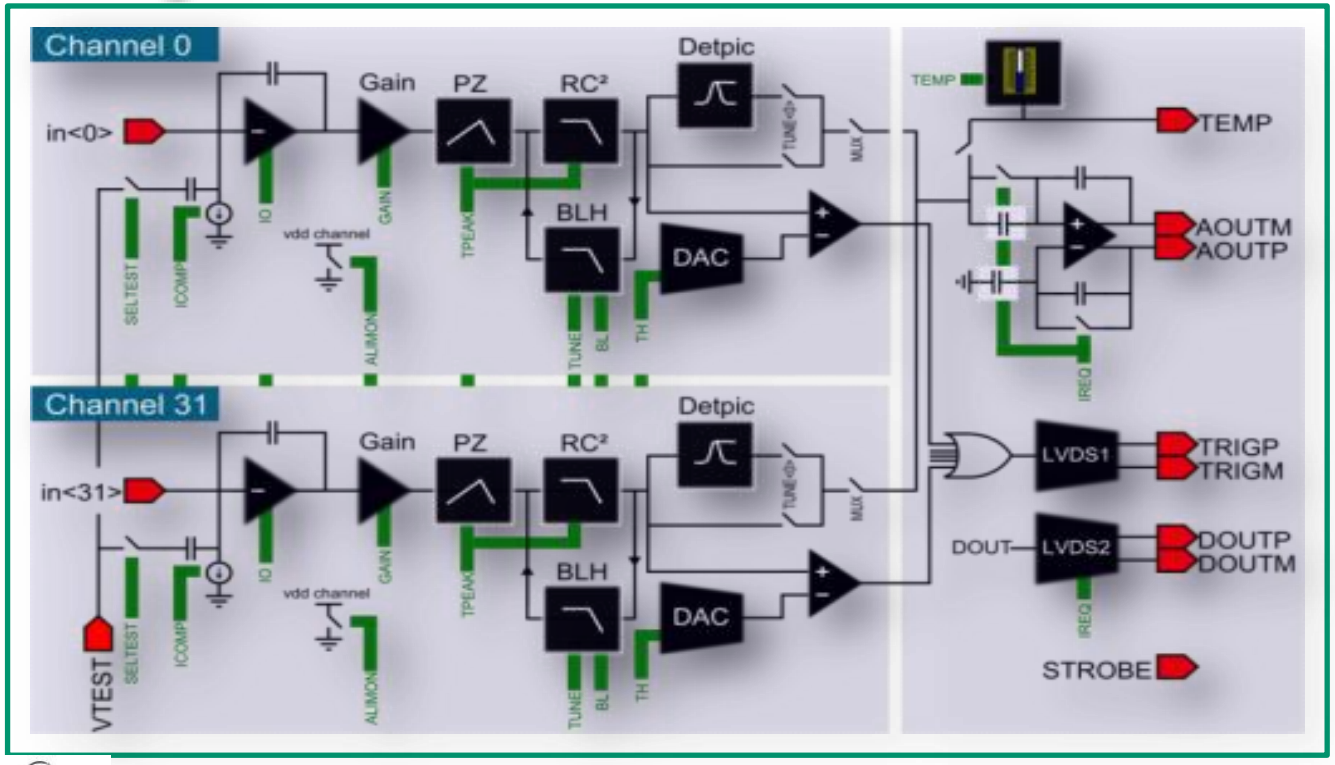
time

IdefX1.1:
16 channels.
Parallel analog outputs

IdefX-Eclairs:
32 channels.
Multiplexed outputs.
1 Range 200keV
<3mW/ch

IdefX-HD:
32 channels.
Multiplexed outputs.
4 Ranges up to 1.2MeV
Low power: 0.8mW/ch

IDeF-X HD (the more recent chip): Architecture



- Embedded temperature Sensor with absolute resolution of 0.5°C.
- Energy and T readout via differential output buffer.

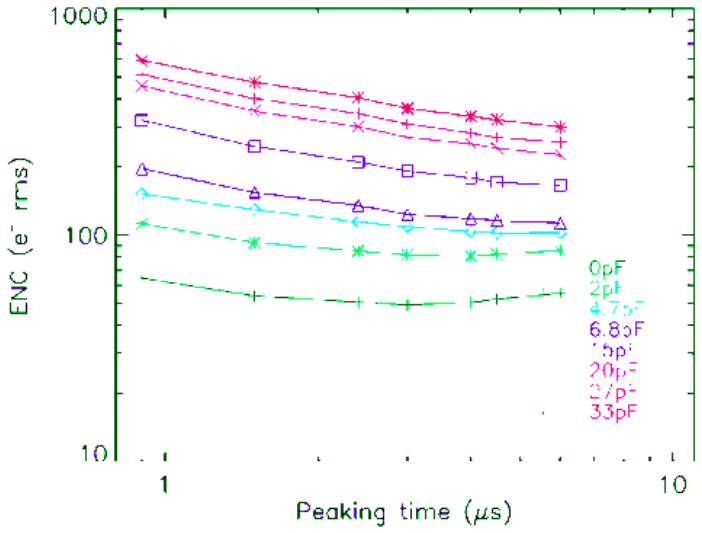
- Slow Control
  - ✓ Multi ASIC interface
  - ✓ Gain
  - ✓ T_{PEAK}
  - ✓ I_{CSA}(23-100µA)
  - ✓ I_{LEAK}
  - ✓ Channel mask
  - ✓ Test mask
  - ✓ AlimON
- Power on reset
- "smart" LVDS input/output
- Hardened digital standard cell

- 32 channels. Muxed output
- CSA (new concept)
- Gain (50, 100, 150, 200mV/fC)
- PZ cancellation
- RC² filter (T_{PEAK}=1 to 10µs)
- Base Line Holder (switchable)
- Peak detector

- 1 Threshold/ channel (6 bits)
- Dynamic up to 1.2MeV (CdTe).
- "OR" Trigger output.
- 3 modes of readout:
  - All channels.
  - Hit channels.
  - On demand

- **Low power: 0.8mW /channel**

Idef-X ECLAIRs: performances



Low Thresh. << 4keV

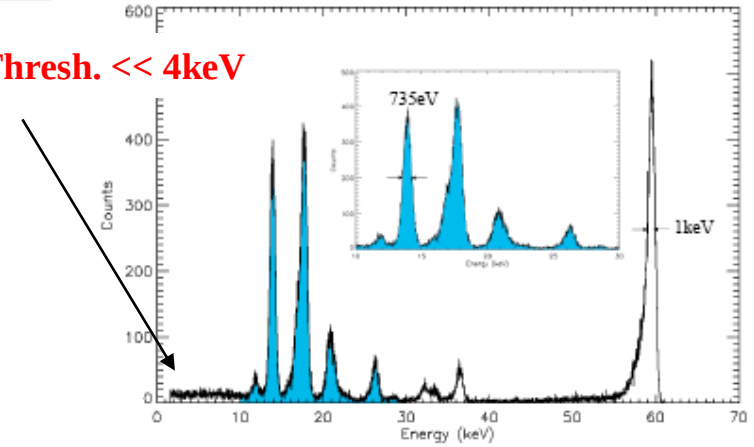


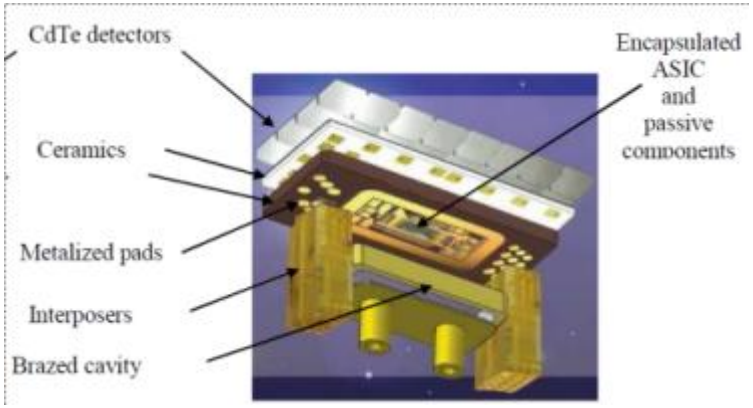
Fig. 6. Spectrum of an ^{241}Am source obtained with a 4.1 × 4.1 × 0.5 mm^3 CdTe detector equipped with a Schottky contact at the anode. The cathode is 2 × 2 mm² pixel surrounded by a 1 mm guard ring. The detector is biased under 330 V at 22°C and is connected to the channel #8 of IDeF-X V1.0 at a 6μs peaking time. The best spectrum is obtained at the highest peaking time because of the very low leakage current of the detector.

Ultra Low Noise

- < 55e- +7e-/pF (10pA det current, 6μs shaping)
- < (574eV+62eV/pF FWHM CdTe*)

(*) to be divided by 1.2 for Si

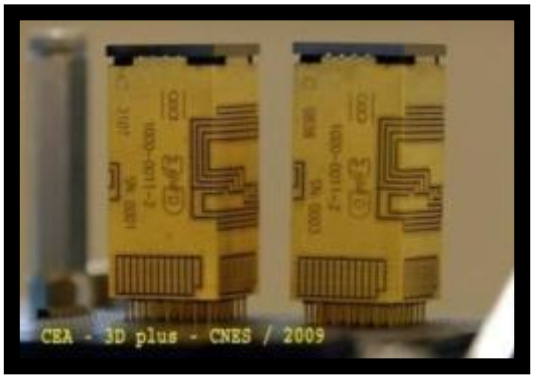
Flight model of the ASIC produced in 2008.
Space Qualification test OK (TID + SEL)
Integration on XRDPIX in progress @CESR Toulouse

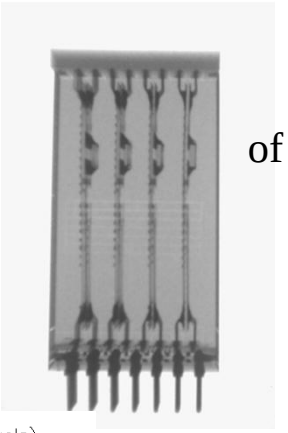


Idef-X HD for Caliste Module (SIMBOL-X, MACSI)

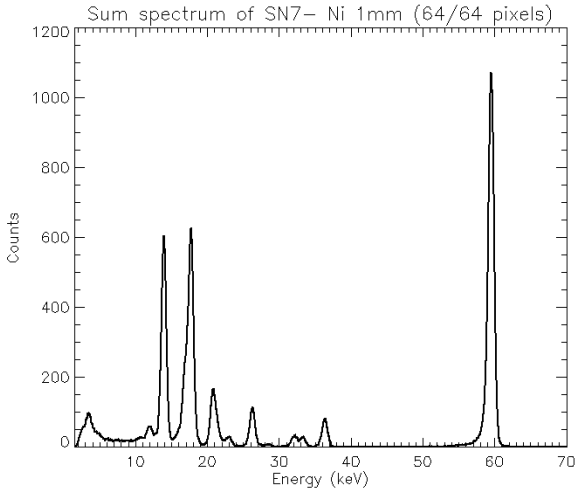
Caliste module houses 8 x 32-channel ASICs + pixelated CdTe (500µm pitch) inside a 1x1x2 cm^2 module:

Possible thanks power reduction in Idef-X HD < 200mW/Caliste.



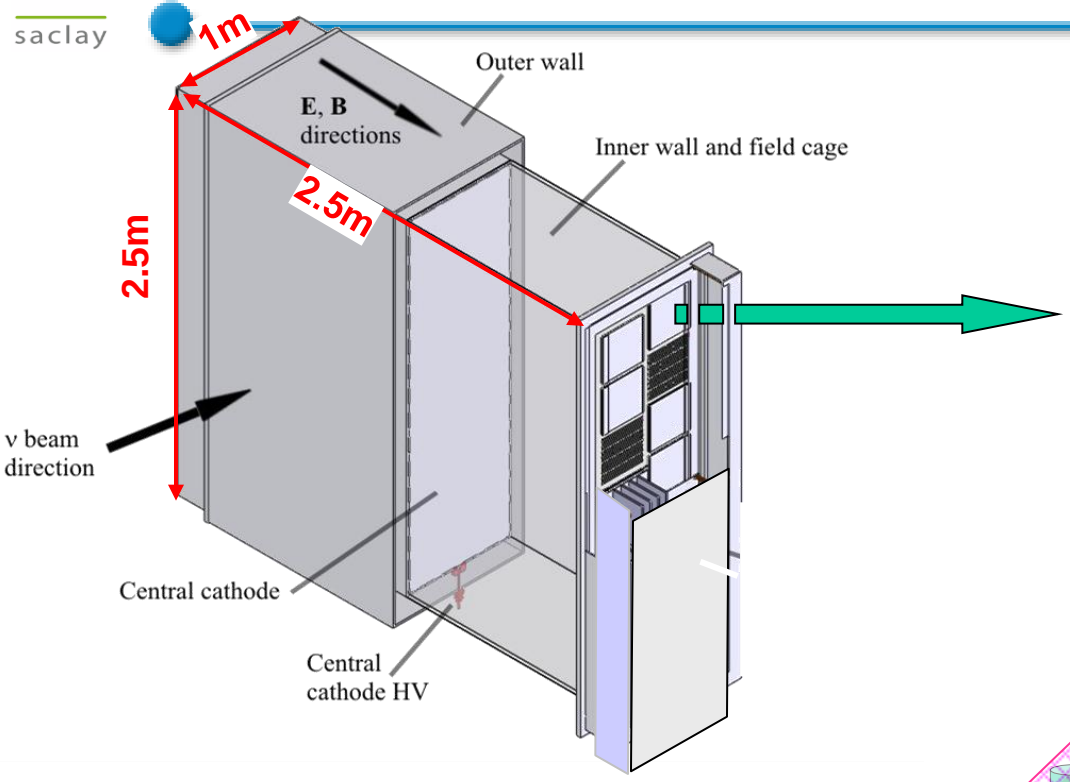


Xray Photography
of the 64-pixel version ofCaliste

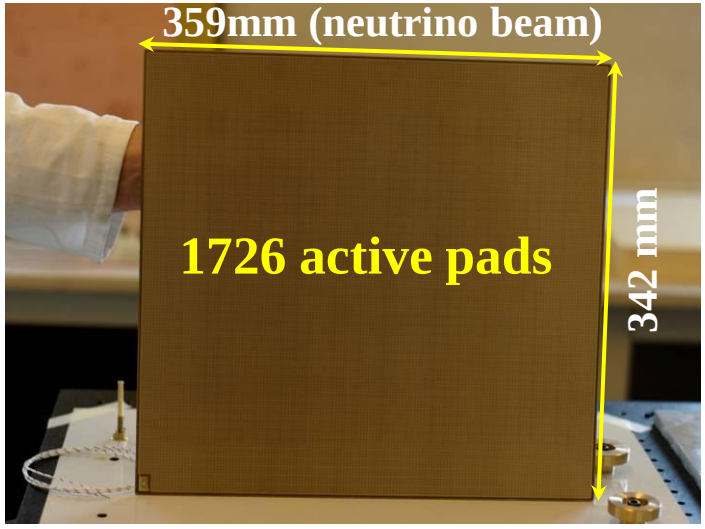


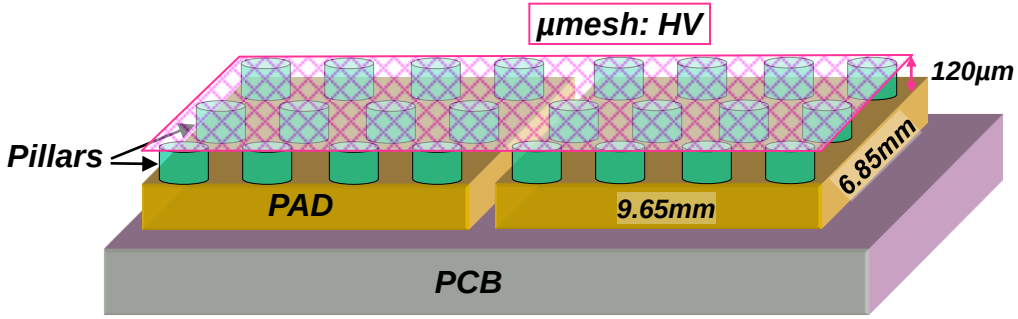
Sum spectrum of ^{241}Am.
Resolution:
800 eV FWHM@ 60keV
700 eV FWHM à 13keV
Threshold = 2keV

The T2K TPCs



Bulk MicroMegas detector





12 detector modules per TPC plane

3 TPCs: 72 modules; 124.272 pads

TPCs inside magnet :

Power Consumption

Cable between detectors & acquisition

X and Y coordinates => pads.

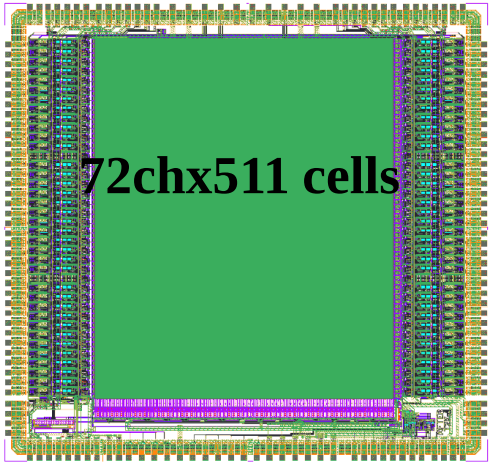
Z => time

Design of a new

compact readout electronics

AFTER: Asic For TPC Electronic Read-out

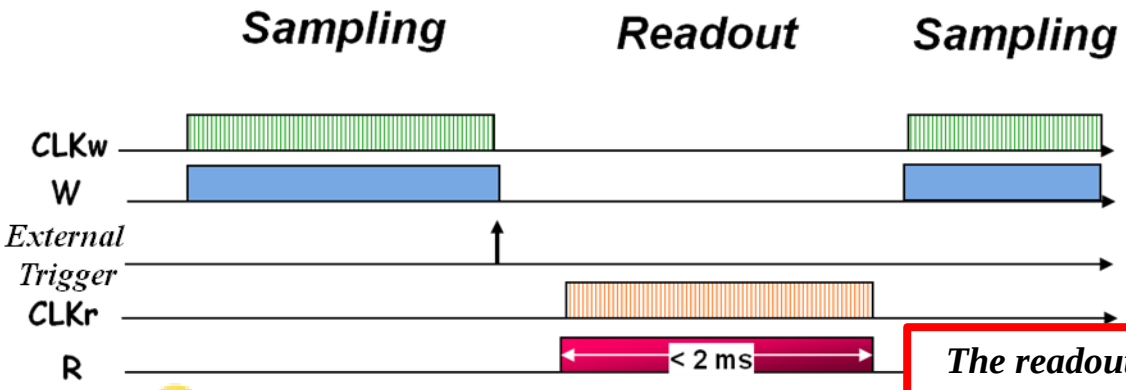
Technology: *AMS CMOS 0.35μm*
Area: *7546μm x 7139 μm*
LQFP 160 pins; Plastic
dimensions: *30mm x 30mm*
thickness: *1.4mm*
pitch: *0.65mm*
Number of transistors: *400,000*
Power consumption: *5-7 mW/ch*
6000 chips manufactured and tested

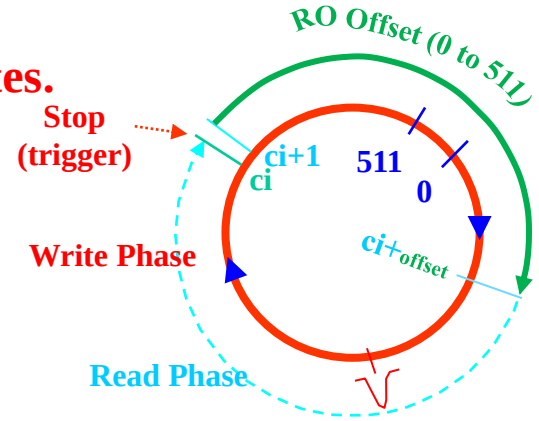


Purpose:

- Collect, preamplify and shape of the detector signal.
-Continuously sample the shaped signal in an 511-cell analog circular buffer (1MHz to 100MHz rate)
-After the sampling has been stopped **by an external request**, read back the analog memory (partially or totally) at a rate up to 20 MHz.

⇒Allows to de-correlate the sampling and digitization rates.
⇒An oscilloscope on each channel.

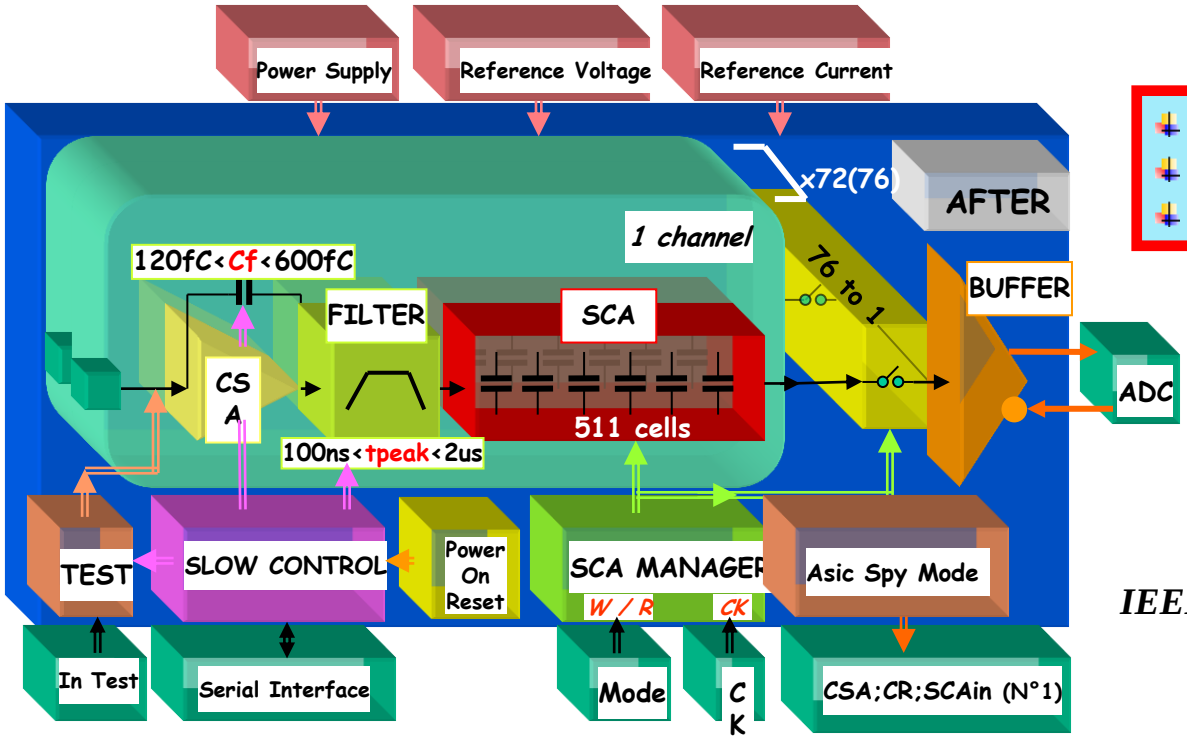




AFTER: ROOffset=0
AGET: ROOffset is programmable

The readout time is proportionnal to the number of sample read : 2ms is for 511 cells

AFTER Main Features: 72 low noise FE channels associated with a 511-cell SCA



- No onchip zero suppress.
- No auto triggering.
- No selective readout.

IEEE Trans. Nucl Sci, June 2008

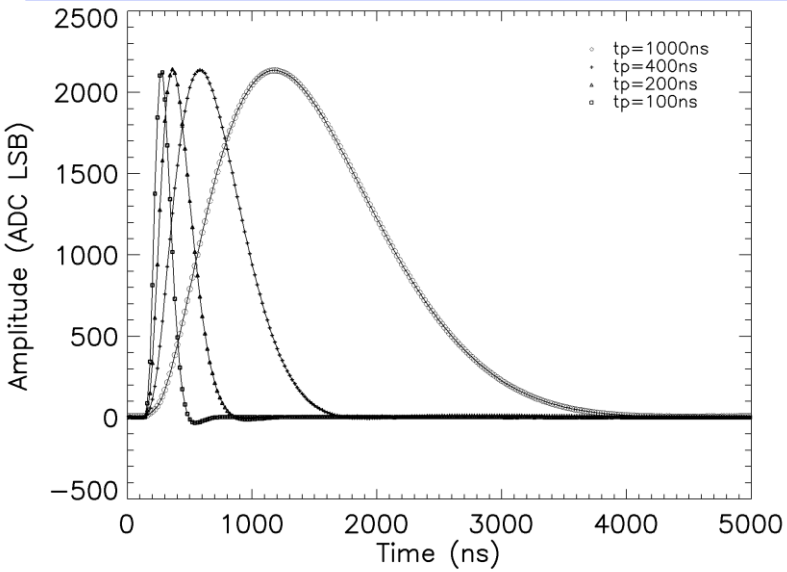
Main features:

- **Input Current Polarity:** positive **or** negative
- **72** Analog Channels
- **4** Gains: 120fC, 240fC, 360fC & 600fC
- **16** Peaking Time values: (100ns to 2µs)
- **511 analog memory cells / Channel:**
  Fwrite: 1MHz-100MHz; Fread: 20MHz

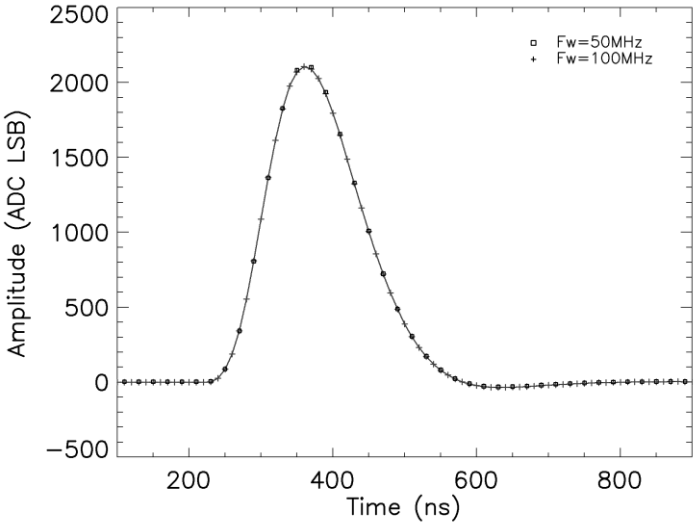
- **Optimized for 20-30pF detector capa**
- **12-bit dynamic range**
- **Slow Control**
- **Power on reset**
- **Test modes**
- **Spy mode on channel 1:**
  CSA, CR or filter out

Pulse Shape + linearity

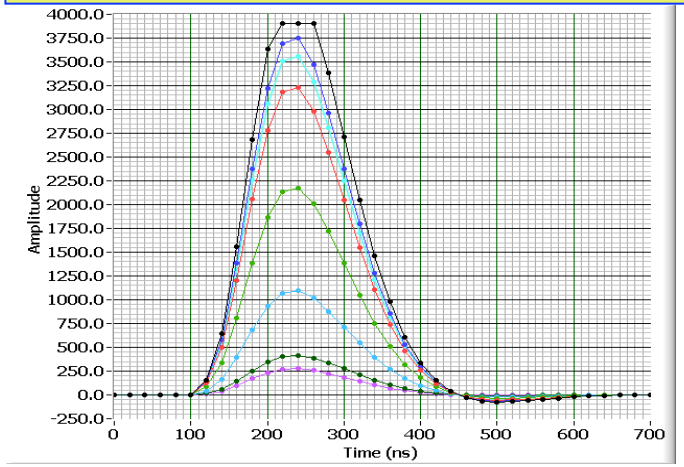
Digitized signal with various peaking time



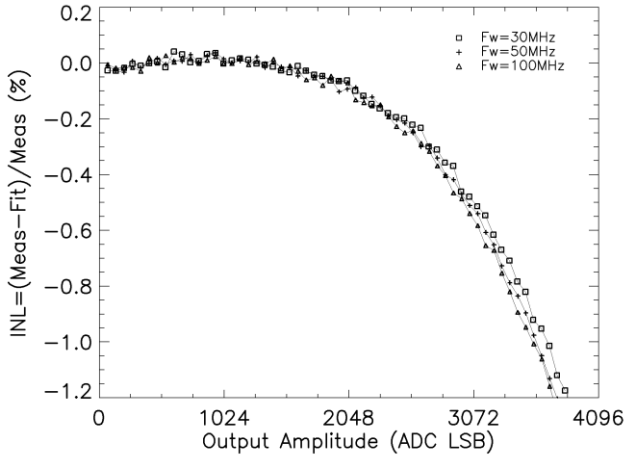
Perfectly working for a 100MHz wck



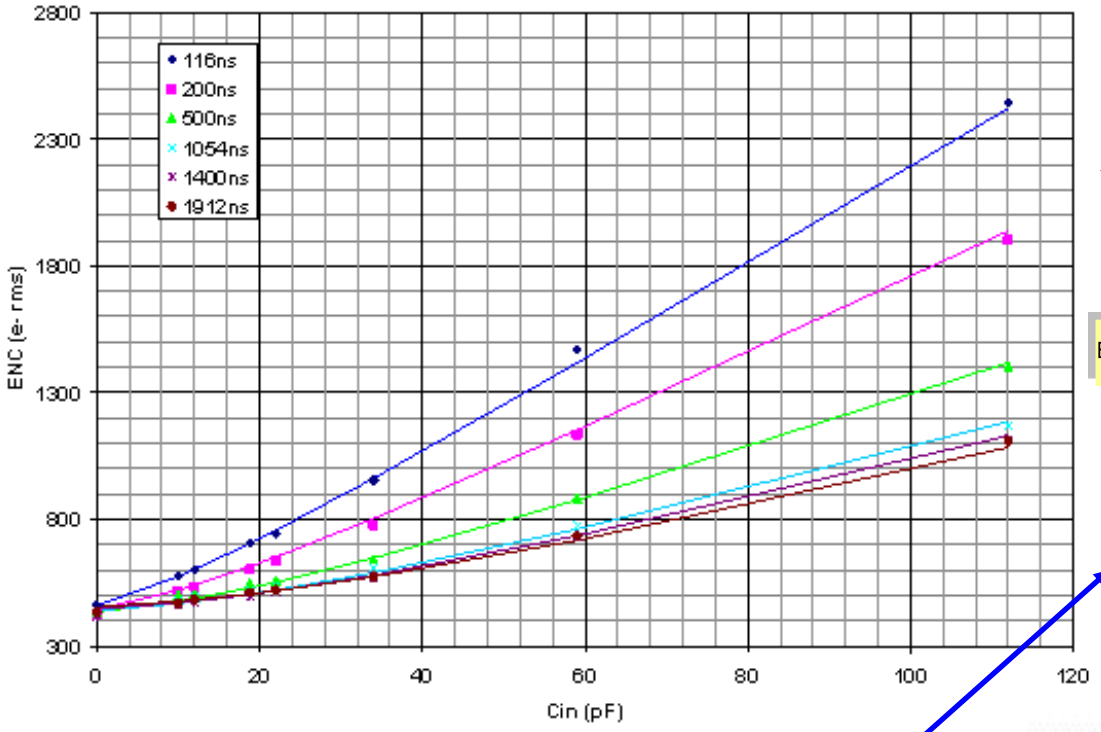
Pulse Shape Independent of amplitude



Integral Non Linearity <1.2%



AFTER: measured Equivalent Charge



dot= meas
line= quadratic parametrization

$$ENC^2_{AFTER} = \frac{\alpha^2 (I_{POLcsa}) \cdot (C_0 + C_{in})^2}{t_p} + \gamma^2 \cdot (C_0 + C_{in})^2 + \beta^2 . t_p + \frac{V^2_{n\_2ndstages}}{F^2_{CSA120} \cdot Gchain^2} \cdot Range^2_{CSA}$$

ENC = ENC0 (tp, ICSA) + a (tp, ICSA). Cin

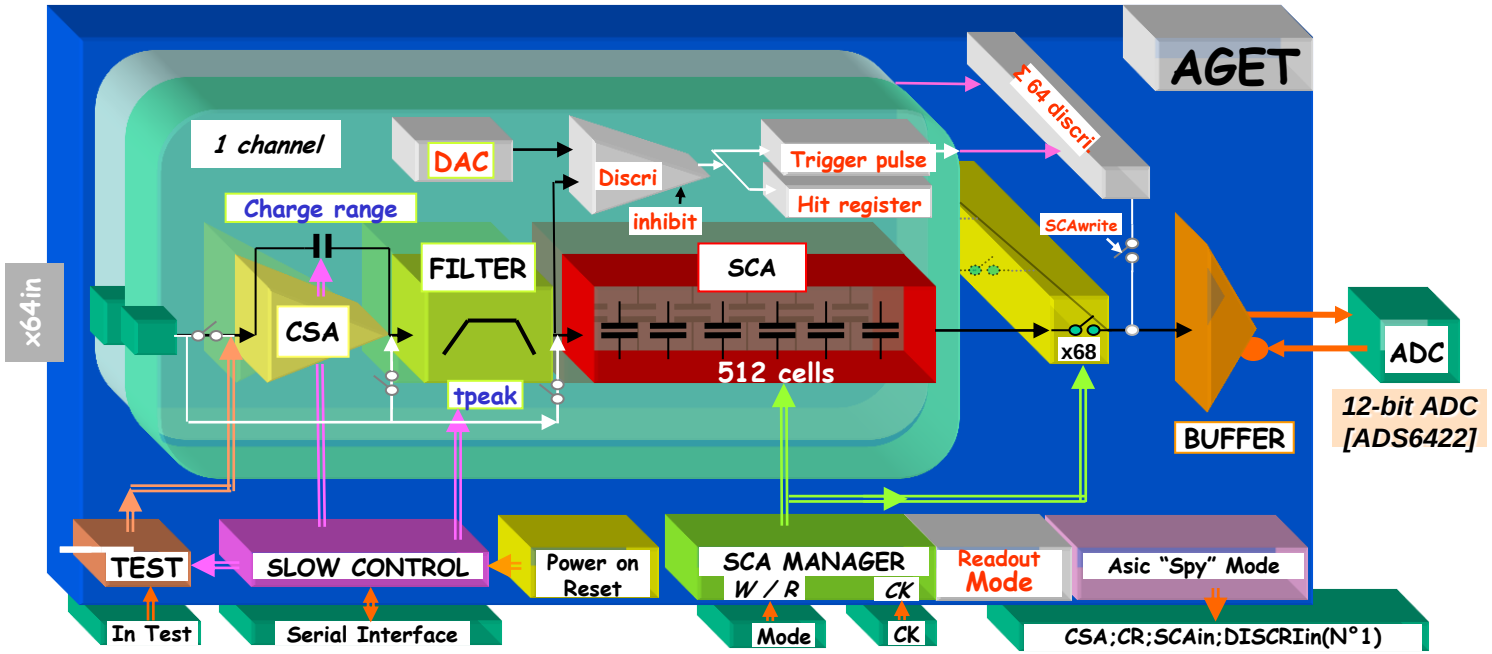
- Quadratic & linear Parametrizations extracted for all the conditions of operation.

		100 ns	200 ns	500 ns	2 µs	Unit
120 fC	*Offset*	*350*	*370*	*415*	*404*	*e-*
	Slope	22.2	14.6	7.8	5.3	*e-/pF*
240 fC	*Offset*	*690*	*700*	*775*	*750*	*e-*
	Slope	13	8.5	4.5	3.1	*e-/pF*
360 fC	*Offset*	*1015*	*1050*	*1135*	*1092*	*e-*
	Slope	10.7	5.6	3	2.8	*e-/pF*
600 fC	*Offset*	*1700*	*1740*	*1817*	*1780*	*e-*
	Slope	6.5	3.2	3.3	1.8	*e-/pF*

AFTER byProducts

- 6000 chips have been produced.
- The 120000 channels of T2K are now successfully working since end 2009.
- AFTER is used by other groups/experiments:
  - ILC-EUDET TPC, CLAS12, ACTAR, LLR, Saragossa , TU-Munich, MSU,…) :
    - kapton + cube of 1728 channels + DAQ boards (Ethernet readout)
    - 288 channels FEC board + interface for USB 2 readout.
    - 72 channels + Ethernet
    - Custom made boards

AGET: General ASIC for active target TPCs (ANR GET)



- 64 Analog Channels: Analog part + Sampling Capacitor Array.
- CSA + PZC + Filter (semi-Gaussian order 2).
- SCA: 512 analog memory cells.

NEW

- Programmable Readout Offset
- Discriminator + Threshold DAC/Channel + mask.
- Digital Trigger output (LVDS)
- Multiplicity Output [Analog sum of the discri outputs.].
- High Charge range (10pC)
- Several SCA readout modes (all, zero-supress, on demand)
- 2p acquisition mode: double buffer mode

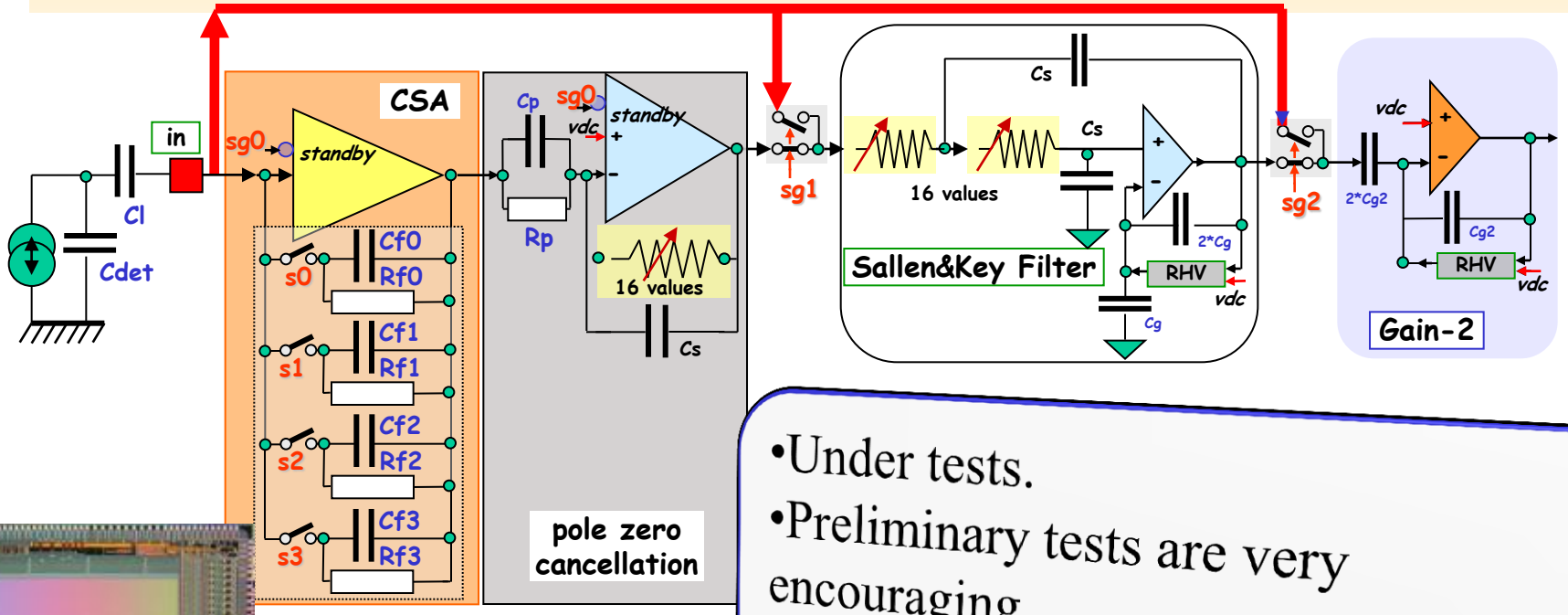
- Slow Control.
- Power on reset.
- Test modes.
- Spy mode.
- Channel inhibit

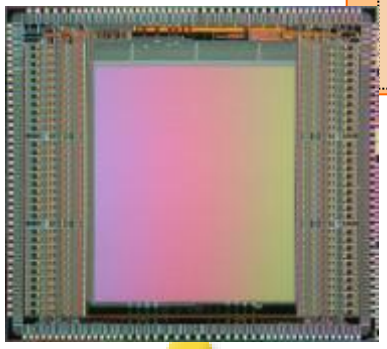
AGET: Analog Part

CSA : 4 Charge ranges; 2 bits register / channel: 120 fC, 240 fC, 1 pC & 10 pC.
saturation behavior improved

Shaper : tuneable from 50ns to 1µs.

Bypass: Possible bypass of the Preamp and/or of the shaper => open to other type of detectors.

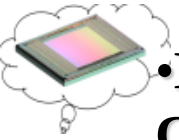




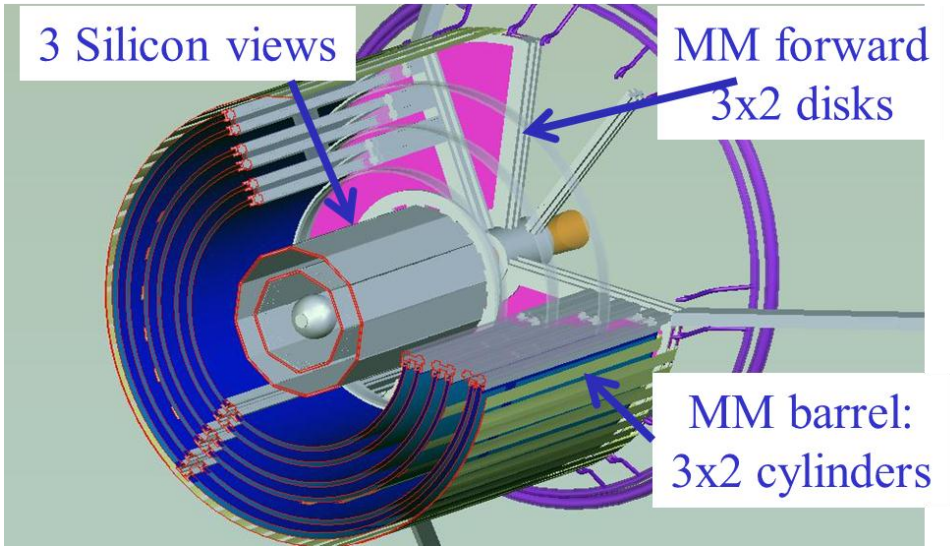
- **AMS CMOS0.35µm**
- 60 mm^2

- Under tests.
- Preliminary tests are very encouraging
- Performances: equal or better than AFTER expected

DREAM (Deadtimeless Readout Analog Memory)

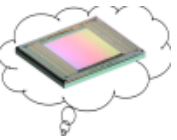


- **Designed to read the ~20000 channels of a Micromegas tracker for the CLAS12 upgrade @ JLAB.**
- **More than 5mm^2 of stripped detectors.**

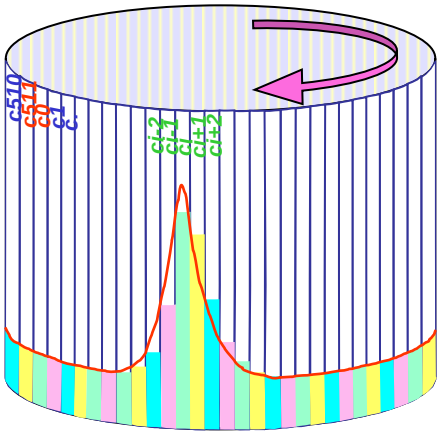


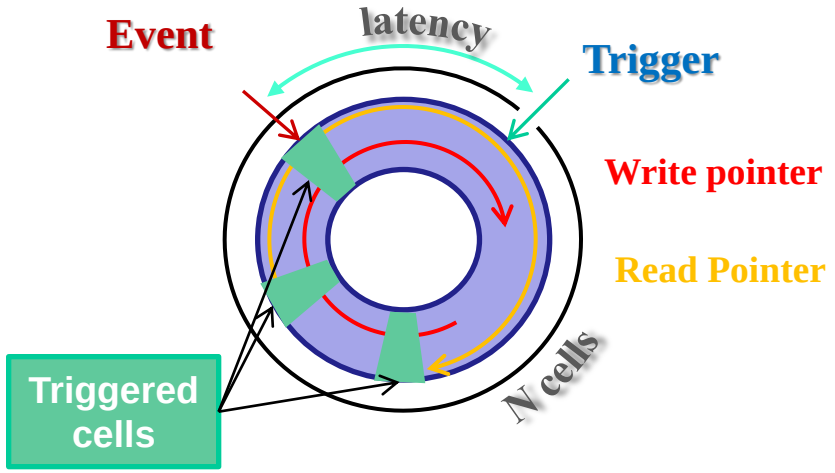
- **Based on AFTER/AGET structure, but:**
  - **Design for high detector capacity (ENC <2000 e- for Tp=150ns @150pF)**
  - **Dead Time "Free" readout:**
  - The 512 cell Switched Capacitor Array is used as a **circular analogue buffer** (both L1 latency buffer + derandomizing buffer)
- **Chip submission in Feb 2011.**

DREAM: Analog Memory L1 buffer solution (APV-like solution)



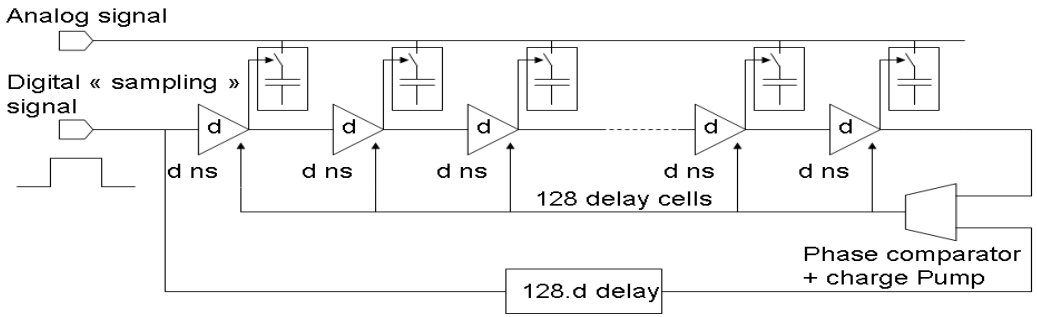
- The analog signals of all the channels is **continuously** sampled at F_s in a **Switched Capacitor Array** (analogue memories).
- When a L1-Trigger occurs it is sent to the chips with a CONSTANT LATENCY (T_{LAT}):
  - N (typ 4) samples on all channels are kept (frozen) for each triggered event.
  - They are read and multiplexed towards an external ADC @ Fread rate (externally defined) while continuing the write operation.
- Cells are **rewritten** after readout or if no trigger occurs after $T_{LAT.}$
- **Dead Time "Free"** architecture:
  - No interruption of writing during readout of a triggered event.
  - several (up to 40) triggered events can be stored in the SCA waiting for readout.
- **No on-chip zero suppress:** all channels are read for a trigger.





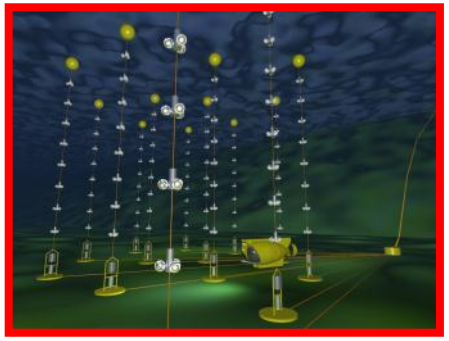
Ultrafast analogue memories

- **Same principle than in AFTER/AGET, but the clock is virtually internally multiplied by embedded Delay Line Loops (or a matrix of DLLs)**

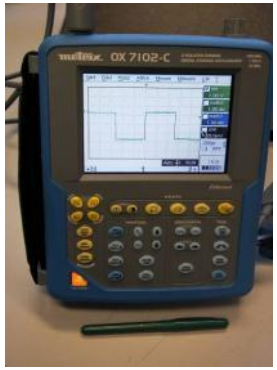


- **Sampling frequency up to several GS/s**
- **Slower readout (typ 10-20MHz) triggered externally.**
- **May be used as atime expanded and/or L1 buffer.**
- **Low power (compared to ADC), but deadtime due to readout.**
- **Data reduction before to go digital.**
- **Used in several Irfu's chips:**

ARS (ANTARES Neutrino submarine experiment)



Pipeline (heart of a commercial handeld oscilloscope)



MATACQ (heart of the Caen V1729)

SAM (HESS 2)

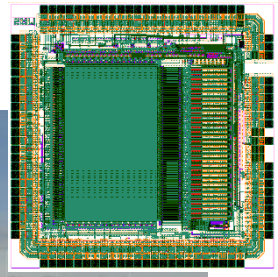
The SAM chip: an Ultra Fast analogue memory for PMT readout.

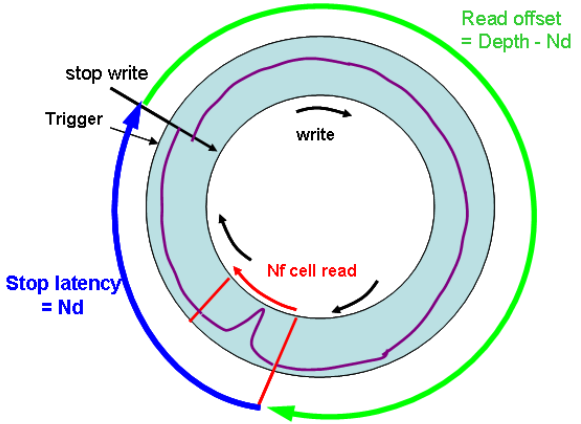
- **Read the 2000 PMTs of the HESS-2 atmospheric Cherenkov telescope in Namibia.**

- **Same functionality than the SCA of AFTER: used as a circular analogue buffer waiting for trigger return. Then "slow conversion" of the window of interest corresponding to the trigger**

- **Integrates 2 differential channels of 256 cells each**

- **Up to 3.2GS/s sampling**



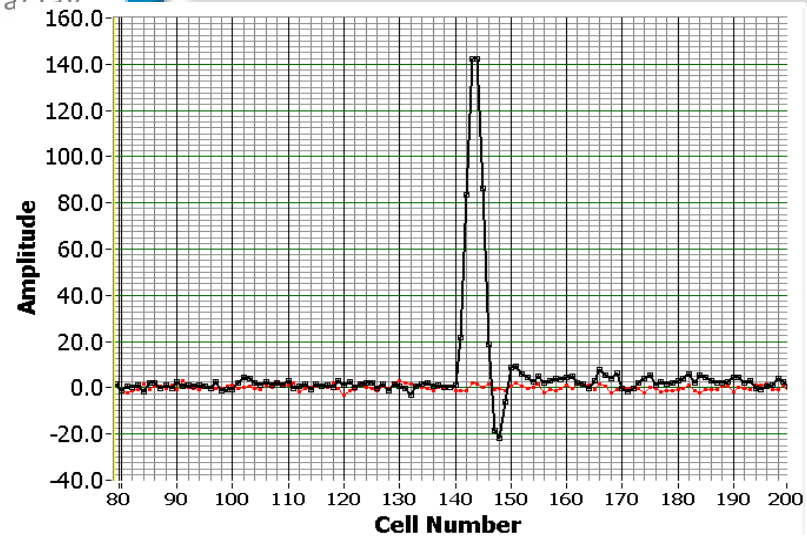


- **Techno AMS CMOS 0.35 µm.**
- **Size ~11 mm²**
- **~60k transitors.**

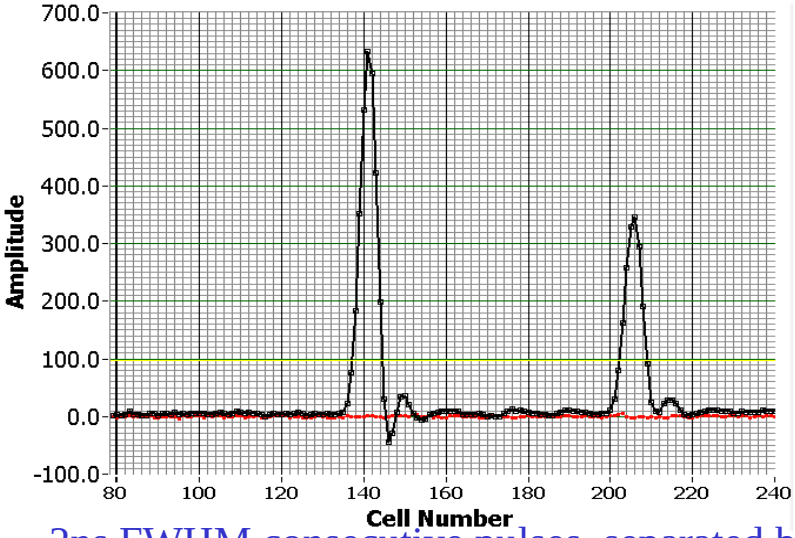
NIM A, Volume 567, I

ssue 1, p. 21-26, 2006

The SAM chip: perfomances



75 mV amplitude, 1ns FWHM pulse. 3.2GS/s



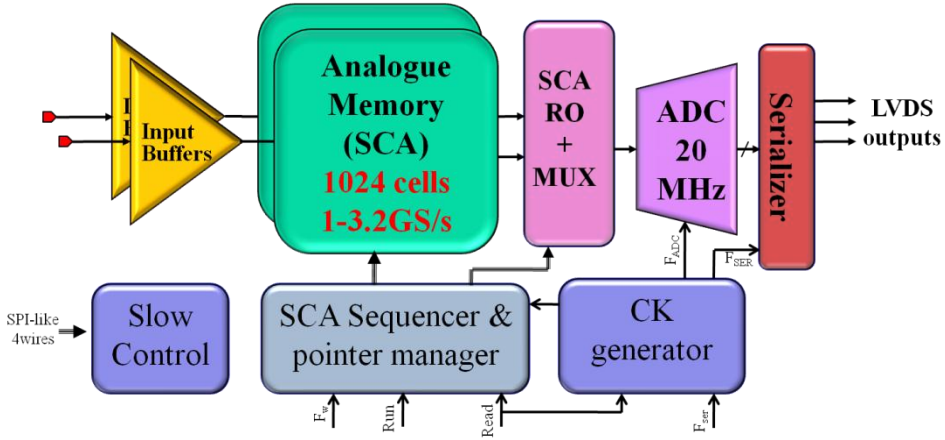
2ns FWHM consecutive pulses, separated by 22ns, (300mV & 170mV amplitude). 3.2 GS/s

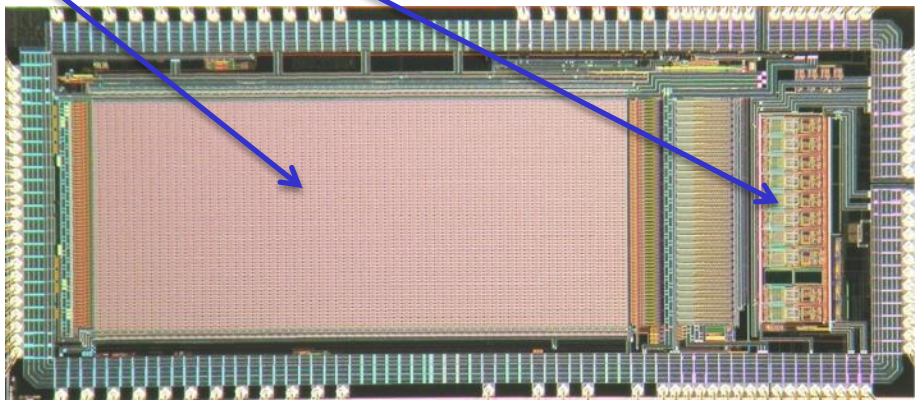
NAME	Value	Unit
Power Consumption	300	mW
Sampling Freq. Range	0.4 to 3.2	GS/s
Analog Bandwidth	>300 (450MHz)	MHz
Maximum event readout Frequency (16 cells)	>800	kHz
Fixed Pattern noise	0.4	mV rms
Total noise	0.65 0.55 if FPN cancelled	mV rms
Maximum signal (limited by ADC range)	2 (4)	V
Dynamic Range	>11.6 (12.6)	bits
Crosstalk	<3	per mil
Integral non linearity	< 1	%
Sampling Jitter	<15	ps rms

The Nectar0 chip for CTA (ANR NECTAR):

- **Our First chip with an integrated high performance ADC (IP block from IN2P3/ LPSC).**

Improved SAM (extended to 1024 cells) + on chip 12bit 20MHz ADC + serializer.





- Techno AMS CMOS 0.35 µm.
- Size ~21 mm²

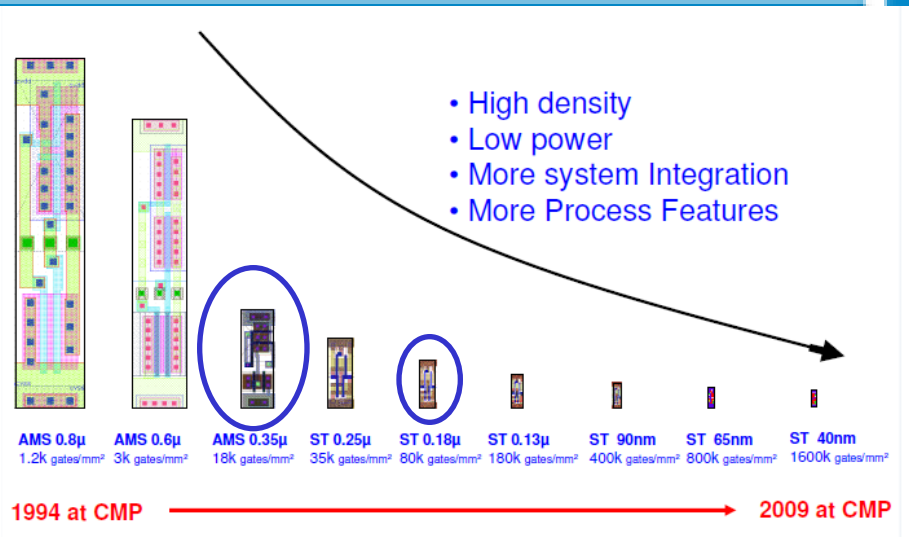
- **Received in July 2010.**
- **First tests on the analogue memory (with external ADC) show:**
  - **performances equivalent to those of SAM.**
  - **less power (<220mW).**
- **Tests with internal ADC expected within 1 month.**

What are the next steps.

- **Next technology node.**
- **The dynamic range problem**
- **ADC integration.**

Migration to the 0.18µm ?

-Decrease by 5 of the digital blocks size.
-More interconnection levels.
-Analog ~unchanged (still not real Deep Submicron)



ANALOG:

- Increase of the chips versatility/ programmability:

in 0.35µm: size of 6 bit slow control register =size of 6 bit dac becomes negligible in 0.18µm. Switches have lower Ron.

=> Move towards « analogue FPGA »: "LOLLY's DREAM"

- ADC: improvement of performances (digital correction and algorithmic ADC) .

Decrease of power consumptions.

DIGITAL:

- Integration of Digital treatment.

- Possibility to Integrate microcontrollers/processors blocks (only few mm^2) for control purpose ?

- Some Groups are studying FPGA integration on ASICs.

-EEPROM blocks are available on some technologies.

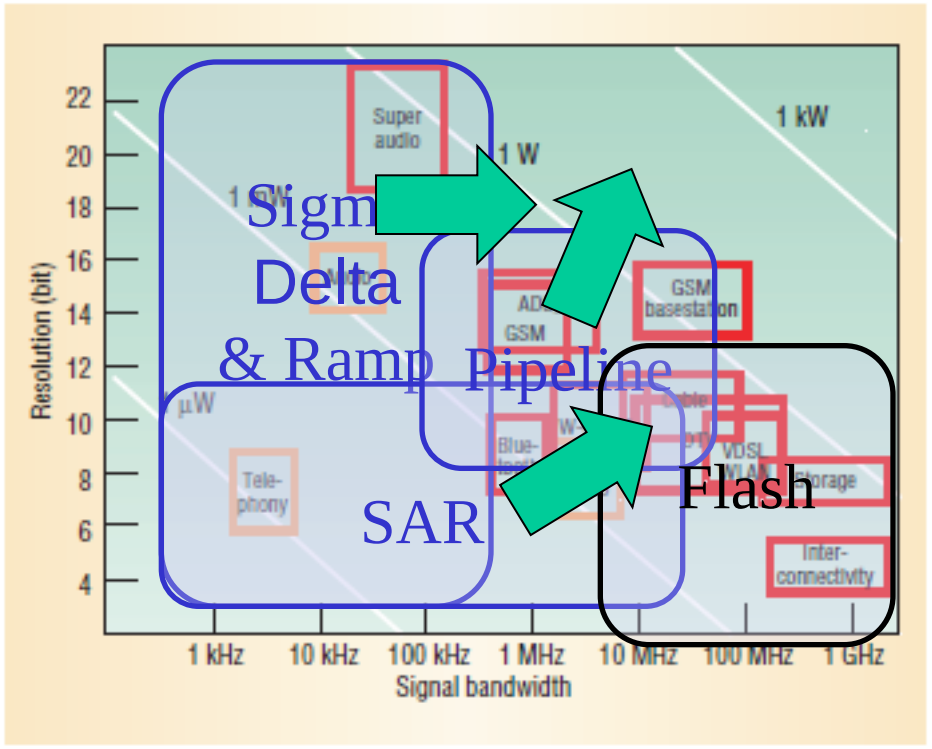
0.18µm from XFAB & AMS are under study , less expensive than 0.13µm from IBM (CERN's choice)

ADC integration ?

- Trend: Go Digital ASAP:
  - Digital treatment easy.
  - Infinite Digital memory.
  - Easy data transmission.
- Not so widely integrated in FE

Chips for physics:

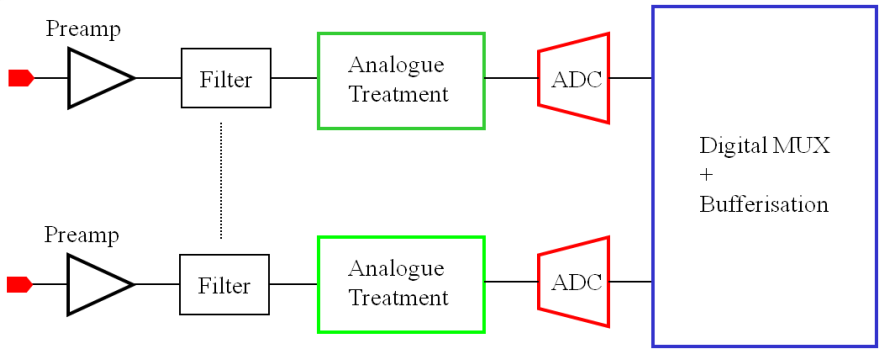
- Performances of commercial ADC are difficult to reach.
- Risk, lack of experience.



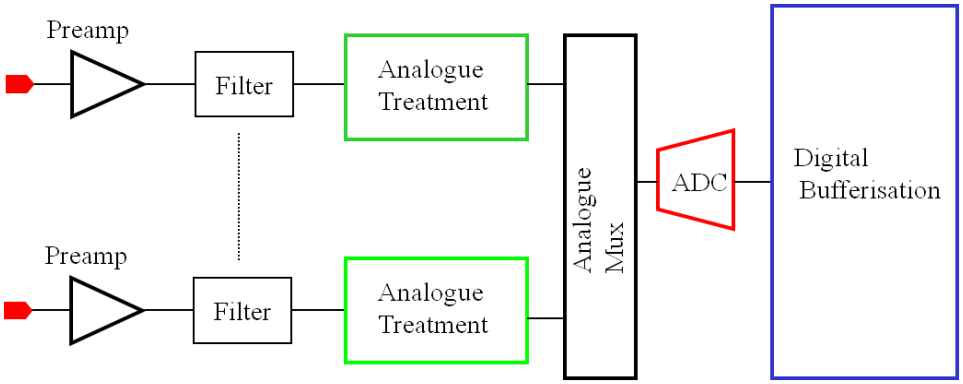
- ADCs take benefits of shrinking:

  => Especially architectures with larger digital par
  - Algorithmic : (SAR) => use several clock cycles for conversion. Fast low precisions analogue blocks and digital
  - Error corrections.=> use poor analogue blocks with redundancy.
- Several working ADCs are now available in the Labs
  - 12 bit/20 MSs, 40mW Pipeline ADC in 0.35µm (LPSC).
  - 12bit/1.5MSsSAR in 0.35µm (RAL)
  - 12bit / 1MSs, 1mW ramp ADC (Irfu)
  - 10bits/40MSs, 30mW Pipeline ADC in 0.13µm (CERN)

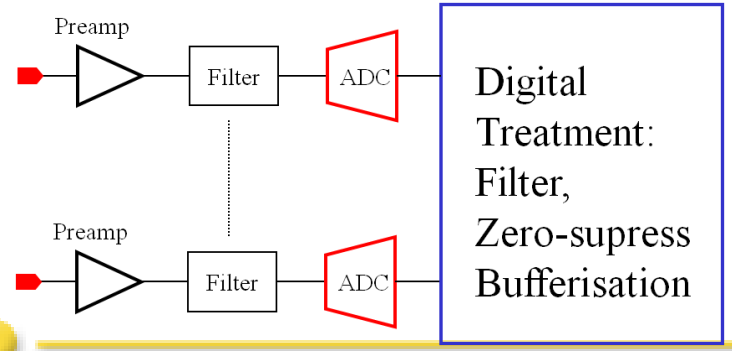
Several ways to go digital inside thechips.



ROC Chips From IN2P3/LAL ....



Nectar



(S)ALTRO (CERN)

ADC PERFORMANCE

Solving the problem of dynamic range in ASICs ?

- For Nuclear Physicis (excepted for HPGe detectors), the noise is not the main limitation.
- Strong limit : ASIC power supply = 3.3V max in 0.35µm CMOS. **Lower and lower in submicron technologies.**
- Practical dynamic range of complex integrated functions is ~12-13 bits. Not enough for some nuclear physics applications.
- This limitation is addressed by at least 3 groups (using the same techno).

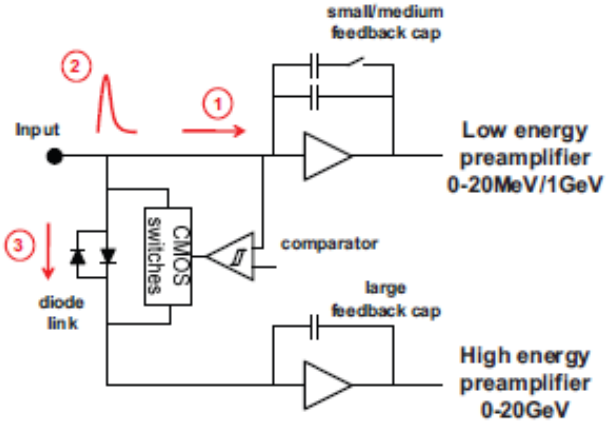
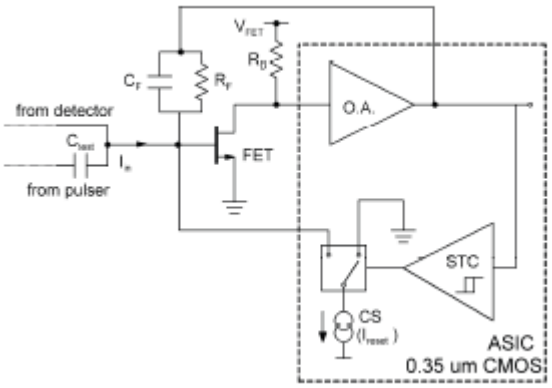
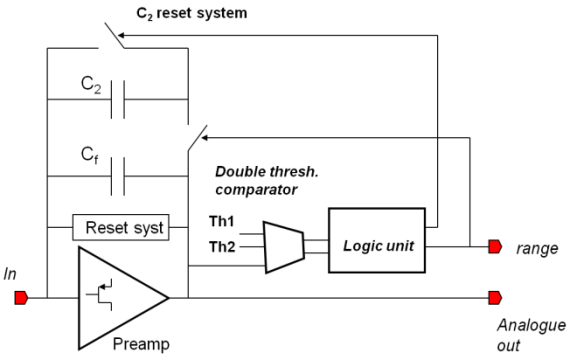


Fig. 1. Front end: each channel has two preamplifiers with different gains, linked by diodes and bypass switches. In normal operation the low-energy preamplifier is the only one connected to the detector (1), but when the energy deposited exceeds its input range, it saturates causing the voltage on the input to change (2) and activating the link to the high-energy preamplifier (3).





AIDA chip (RAL):
Automatic switching between 2 preamps
Successful results on first protype

« TOT » (Milano):
Prototype in fabrication.

Floating point preamp : Ganil + Saclay
Proto submission foreseen in feb 2011

Conclusion

- Strong experience of the Saclay group in FE design.
- ASIC design for HEP, Nuclear Physics and Astrophysics.
- ~100000 chips working worlwide.
- There is need of R&D on Nuclear Physics chips.
- Open to collaborate on R&D subjects on microelectronics for Nuclear Physics.

Spare slides

Use of Microelectronics for Nuclear Physics

- **Less widely used than in HEP, Astrophysics. Why ?:**

  - **Smaller number of channels, less density** => less & less true.

  - **Performance :**
    - Dynamic range limited to ~12 bits **=> possible architectural solutions.**
    - Noise: 1/f noise limitation of CMOS technology/JFET.

    (But not so bad: 3.9 keV resolution obtained on a « big » EXOGAM clover with SFE16 not-optimized preamp at room temperature.)

    => enough for a lot of applications.

    => possible use of external JFET for HPGe.

  - **Cost of development and production.**

    => Some « old » technologies are very affordable (CMOS 0.35µm AMS & XFAB) -> 0.18µm

    =>Think ASIC as a re-usable component.

General Use ASICs ?

- cost dominated by prototyping cost or/and cost of mask in case of engineering run => 1 ASIC for several applications = save of money.

- in CMOS/BiCMOS chips, it is easy to integrate :
  - Links for programming, programmable sequencers
  - Switchs, DACs and programmable components:

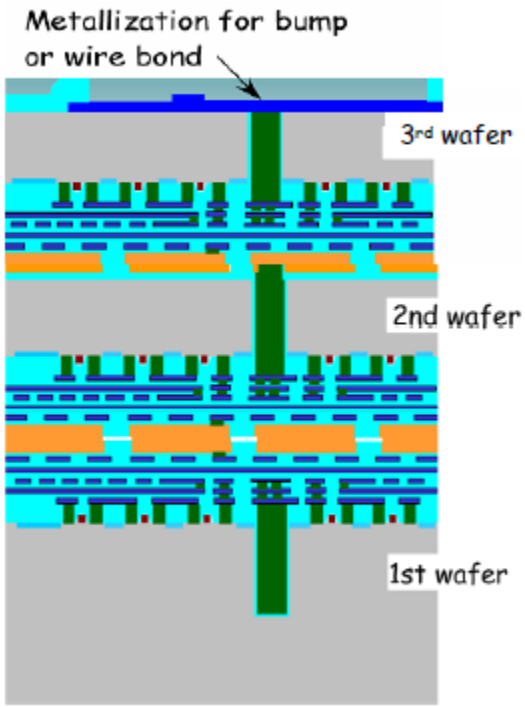
    ⇒ Gain & shaping control, threshold setting, program signal path.

- When we think about specifications :
  - think about other uses of the chip.
  - Needs of the other communities ?
  - Joined effort between groups => **consortium.**

- Limits of the exercise:
  - ASIC means “application specific integrated circuit” !!!
  - Adding a new options always degrades something.
  - More functions: more risk & more design effort.
  - Multi functions ASIC harder to test.

More futurist : 3D-Integration

- Less expensive than advanced CMOS.
- Now mature in industry.
- Some technologies are compatible with:
  - Heterogeneous stacking: best technology for each function
  - Edgeless electronics
- Some of them are now opened for prototyping=> (Chartered/Tezzaron):



VFE

ADC

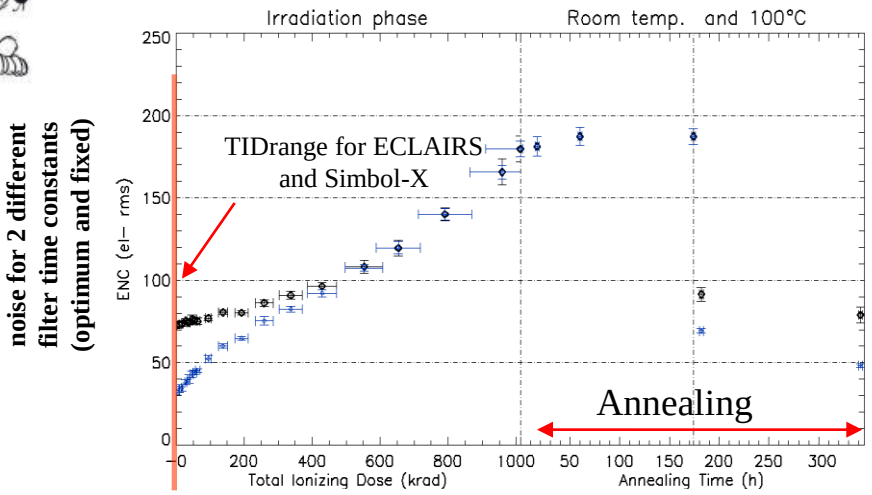
Digital

HEP consortium to evaluate this technology (Fermilab,IN2P3,INFN,CEA)

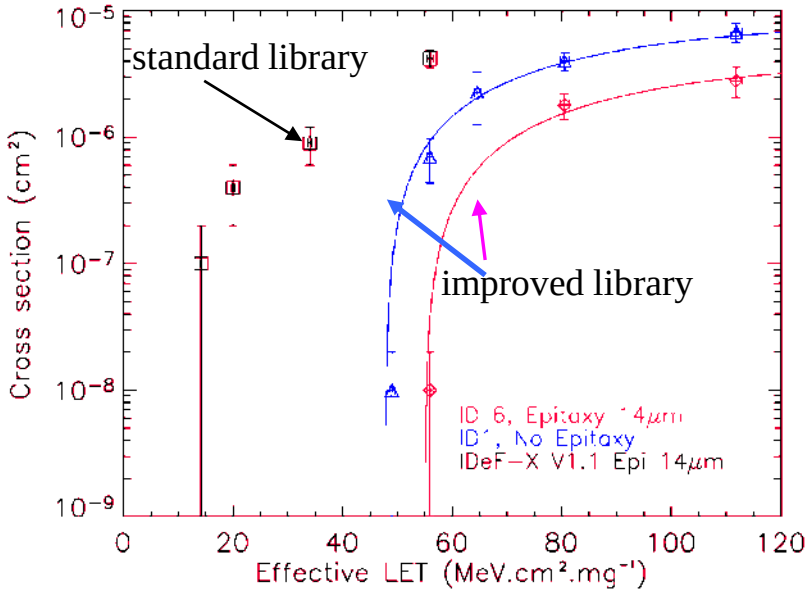
A first demonstrator has just been receveid.

IDeF-X family : radiation hardness

- TID: Irradiation with ^{60}CO @ 500rad/h (on IdeFX V1)



- Up to 1 Mrad: no visible effect excepted noise increase (cleared by annealing)
- Spec for ECLAIRs and SIMBOL-X :(TID<10krad)



New digital library to improve hardness against Single Event Latchup:

Test on Idef-X V2.E => no anti latchup circuit required for the ECLAIRs mission.

FE Chips Based on analog memories: Few comments

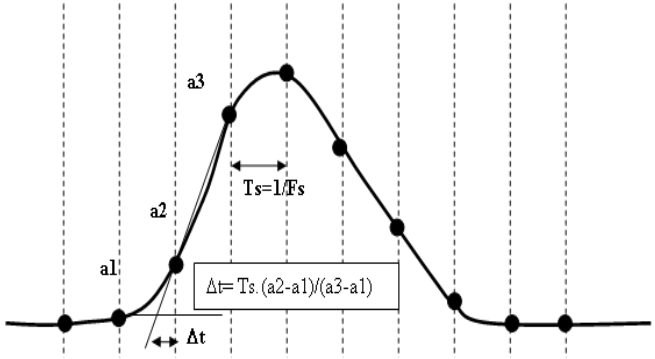
Timing:

- Modest needs for T2K ~ 20ns: no interpolation or complex argorithm
- Timing precision of 1.5ns demonstrated (for high S/N ratio) with interpolation (no calibration required)

Possible Use with semiconductor detectors:

- As it is: Enc = 400e- <=> 3.4 keV FWHM (Si) resolution.
- With the external preamp input of AGET

Dream SCA: Key parameters



Fs> 2/Tp (2 samples in the trailing edge)

=> Fs = 20 MHz for T_{peak} =100ns

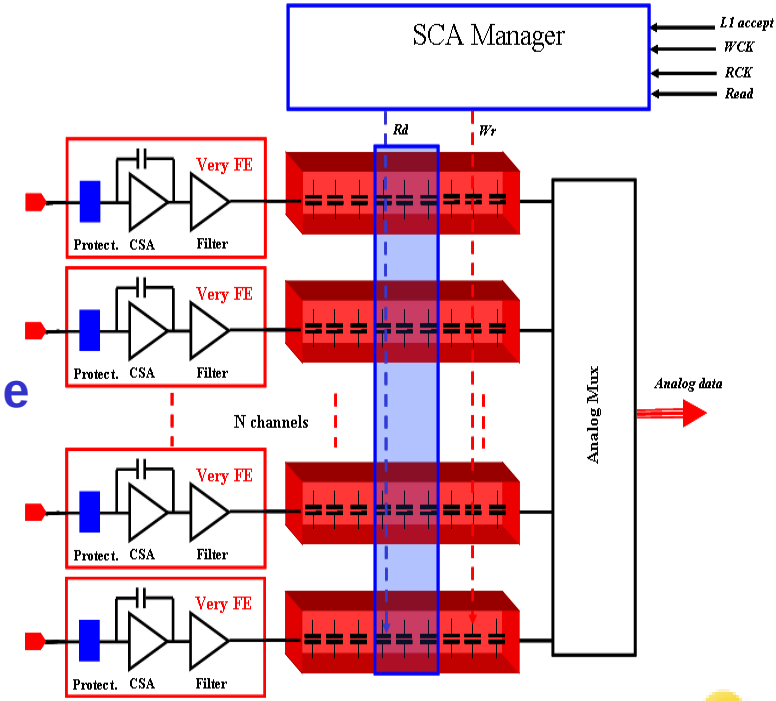
SCA DEPTH = Latency + buffer + extra cells

- **Min 8 µs latency => 160 cells.**
- **Min 10 events derandomizing buffer**

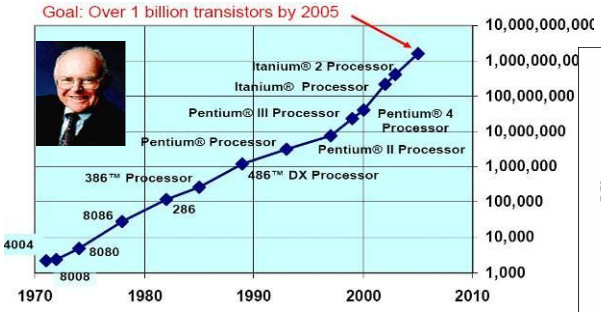
  => 40 cells

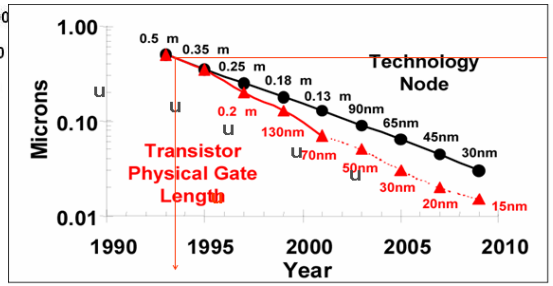
⇒Min SCA depth > 256 => 512 cells is feasible

- **20 MHz readout Frequency**



First trend: Moore's law





ITRS	2004	2007	2010	2013	2016
Technology Node [nm]	90	65	45	32	22
Transistor count [Mtr]	1-200		1500	3092	6184
Transistor Density [Mtr/cm2]	77	154	309	617	1235
Chip Size	140				280
Clock freq [GHz]	3		15		53
Vdd	1.2	1.1	1.0	0.9	0.7
DRAM half pitch	90	65	54	32	22
Signal IO Pads	512	1024	1024	1024	1024
Power Pads	1024				2048

Moore's law : doubling every 2 years

Technology evolution first driven by the computer market:

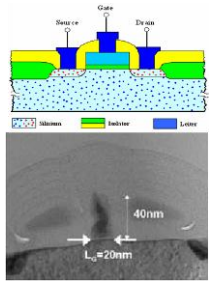
Effect of CMOS shrinking to deepsubmicron.

-=> improve (all the digital performances)
- **-speed.**
- **-dynamic power consumption.**
- **-integration of digital => high volume cost**
- **-Radiation hardness**

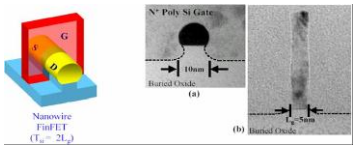
-=>But degrade:
- **-dynamic range (supply voltage).**
- **-Leakage.**
- **-Noise (new sources of noise)**

- No reduction of analog block size.

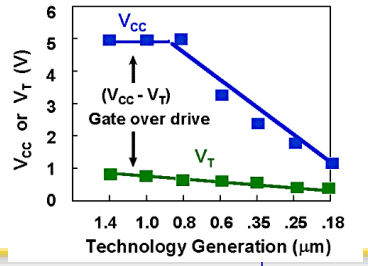
-=> design tools difficult to use.
-=> Need new analogue dessigns



Already In lab in 2005



Possible future for 2015



Cost of foundry increases
Number of foundry decreases
Acces to technolog re and more d

Short Timeli tal technologies

Pro re & more expensive:
650E/mm² x5 in 0.13µm

Price of mask set:
0.35µm: 65kE >x7 in 0.13µm

Wafer size increases

END OF ASICs ???

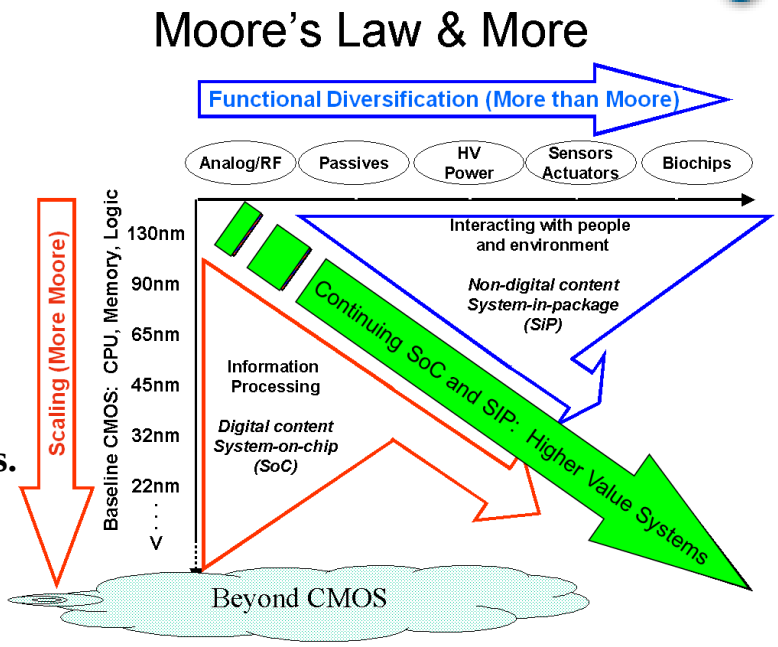
New trends: More than Moore.

New markets appeared in 2000th with « added values »:

- **-telecom**
- **-automotive**
- **-health.**

For these markets 2/3 of the costs in not « digital »

Based on System of chip concept.
Need for integration of RF, HV,Analog,BJT, EEPROM.
Does not required last generation agressive technologies.
Less expensive foundries.
Less Volume => easier access.
Longer technology lifetime.



1 technology node / 3 is kept

- **=> extra modules added to standard CMOS**
- **=> optimized for analogue.**
- **=>lower cost (old infrastructures).**

Perfect situation for our applications.

Our goal : catch the right node: **=> 0.35µm was one (but lifetime is ~5 years)**
=> 0.18µm appears to be the next one (AMS or XFAB).

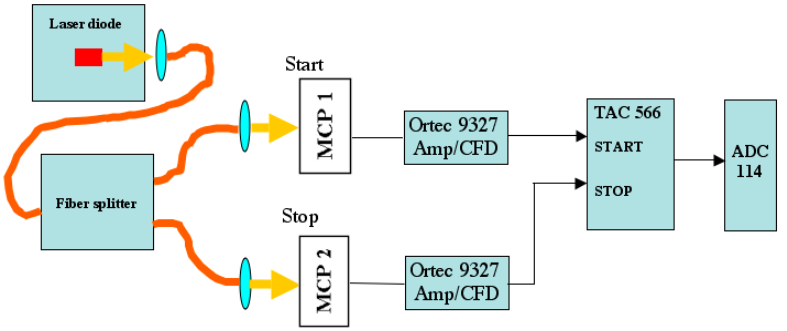
IBM 0.13µm selected by CERN (required for vertex detectors)

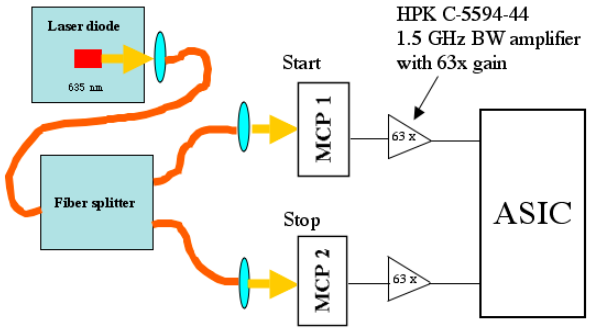
Timing measurements performed with SAM based chip.

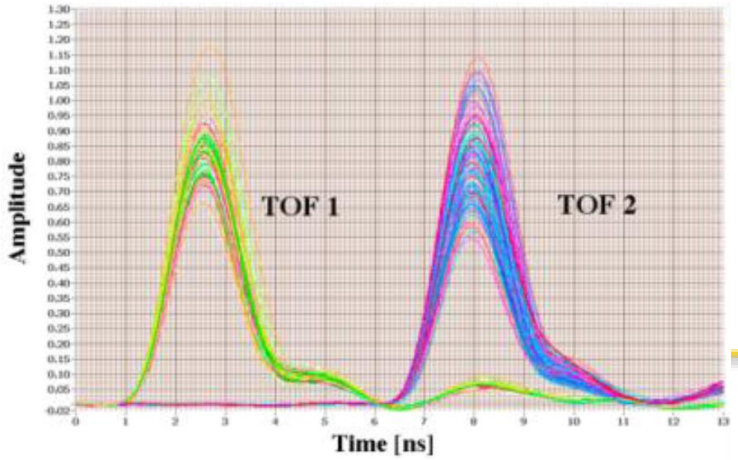
Goal: Replace expensive CFD (hard to design in microelectronics) + TAC by low cost analogue memories (J. Vavra et al, submitted to NIM A)

Test setup @ SLAC:

-2 fast Microchannel plate PMTs (2-3E4 gain) + large BW amplifiers
- Laser pulse split : 35pe +/- 5pe sent to the 2 PMTs
- Direct connection to SAM sampling @ 3.2GS/s.







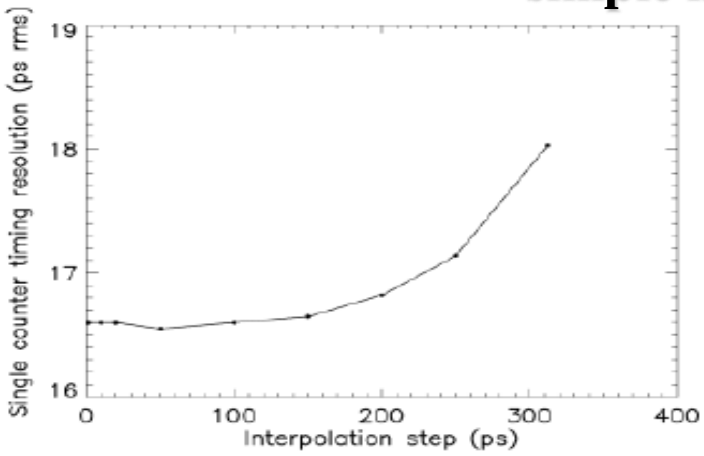
Timing resolution better than 10ps rms demonstrated with pulser

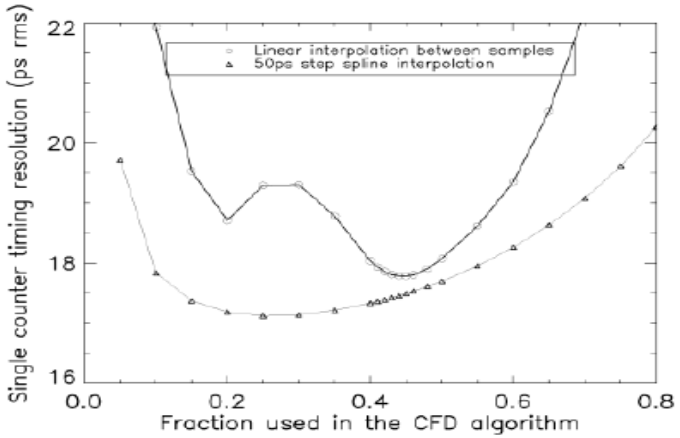
Timing measurements performed with SAM based chip.

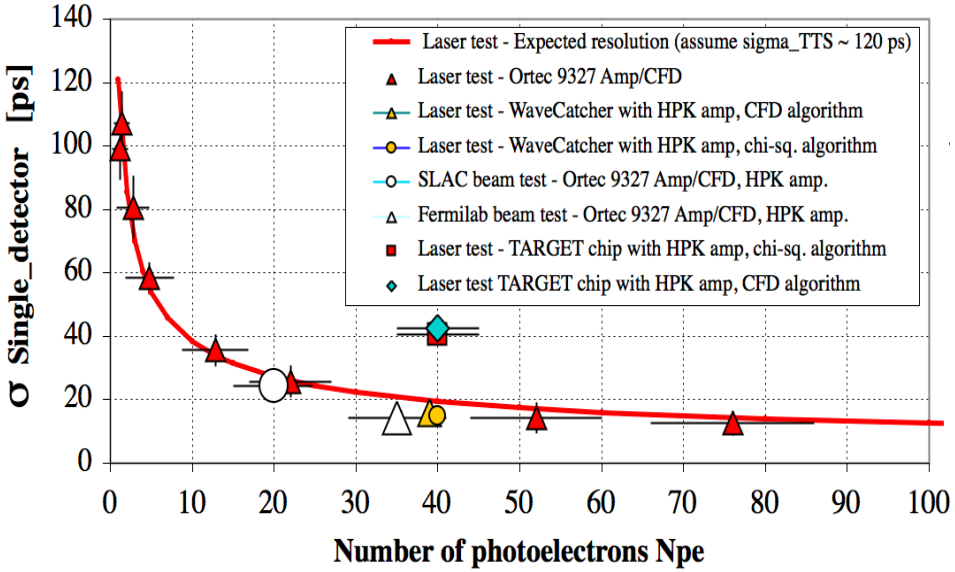
Result = or better than with CFD and consistent with theory

Several strategy tested, but quite similar results:

- **« Chi2 » = fit of an averaged pulse (best results 15 ps rms).**
- **Digital CFD with :**
  - **spline interpolation: various step sizes. 16ps rms)**
  - **simple linear interpolation (easyier to compute, 17 ps rms)**

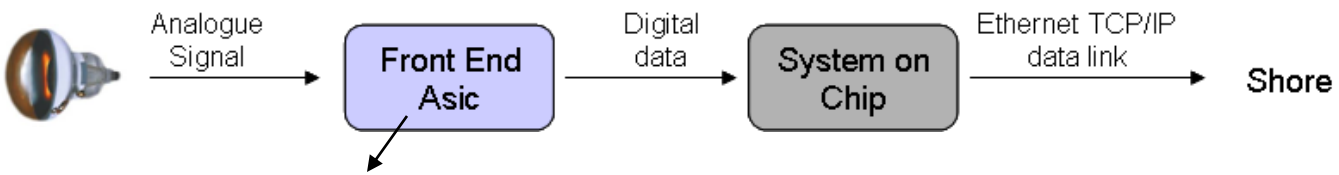




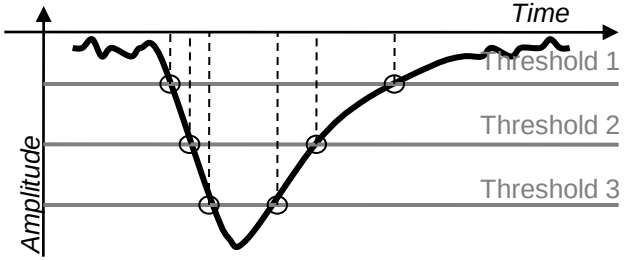


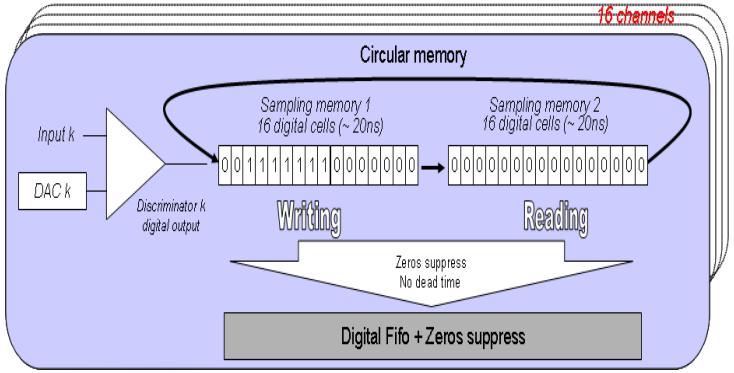
SCOTT: RO chip for the PMT of the Km^3 neutrino submarine detector

-In the frame of KM3NET: (FP6 & FP7): baseline design



-SCOTT: based on the generalized TOT (time over threshold) concept:





•No amplitude coding, but:

• Time coding for each threshold crossing (1ns precision)

•16 independent discriminators channels with threshold set by 10 bit DACs.

• Versatile design, can be configured by slow control:

-1 PMT => 16 coding channels (~1 GS/s 4bit ADC(linear or nonlinear scale depending on the thresholds)

- 16 PMTs => 1- coding channels: (~TDC)

•Zero supress

•Derandomization (FIFO).

•Data driven readout

•SCOTT0= SCOTT single shot version prototyped in dec 2008 => concept validated.

•AMS BiCMOS 0.35µm.

•SCOTT2 (with final RO) submitted sept. 7th 2009.