2021/06/29 INTT 日本語ミーティング

理研テストベンチでの Half entry 問題の検証

理研、RBRC

中川格、**糠塚元気**

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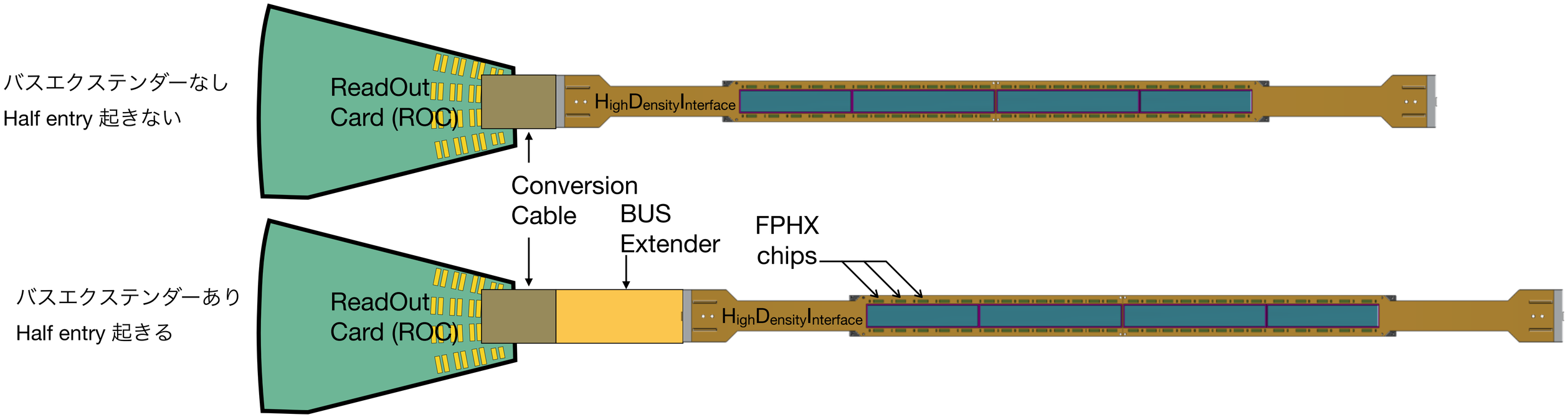
状況

バスエクステンダーを接続してキャリブレーションデータを取ると、想定の半分しかデータが得られないことがある

Half entry は奈良女、台湾テストベンチで確認されている

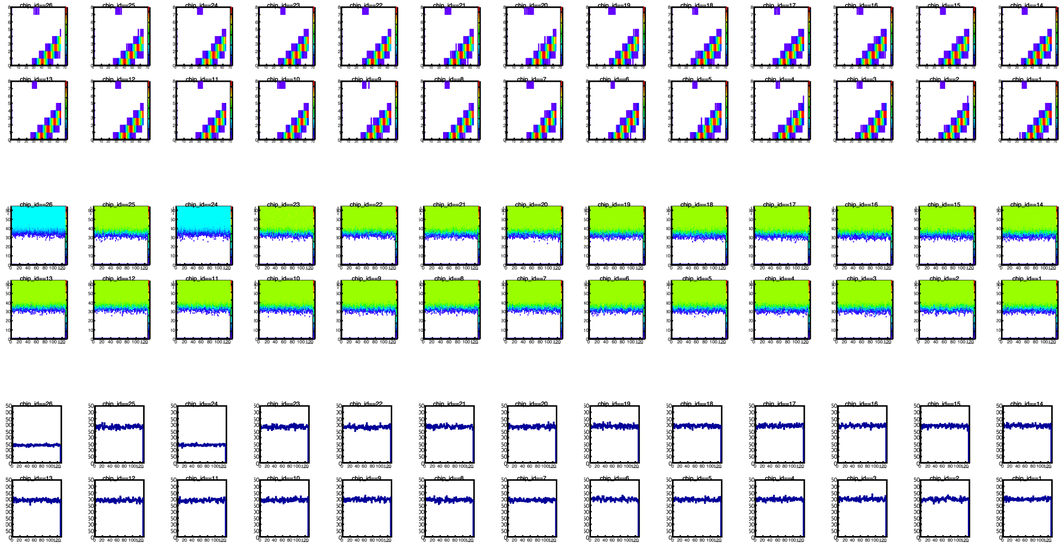
理研テストベンチでは（ほぼ）half entry は起こっていない



理研テストベンチ

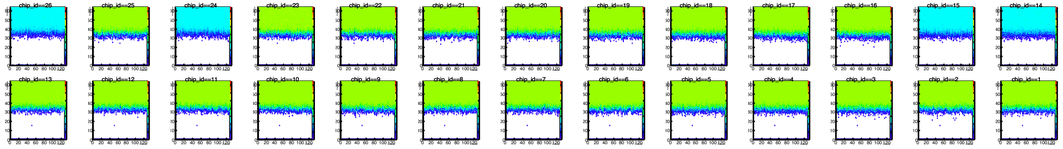
基本的に理研テストベンチではhalf entry は起こっていない

riken_fphx_raw_20210621-2331_0.dat



LVDS = 2 mA (デフォルト)
INTT：Pre2
ROC：NW1
ROC ポート：C3
conv. cable：small8
Bus extender: new 2
(chip24, 26 のラインがショートしてる)

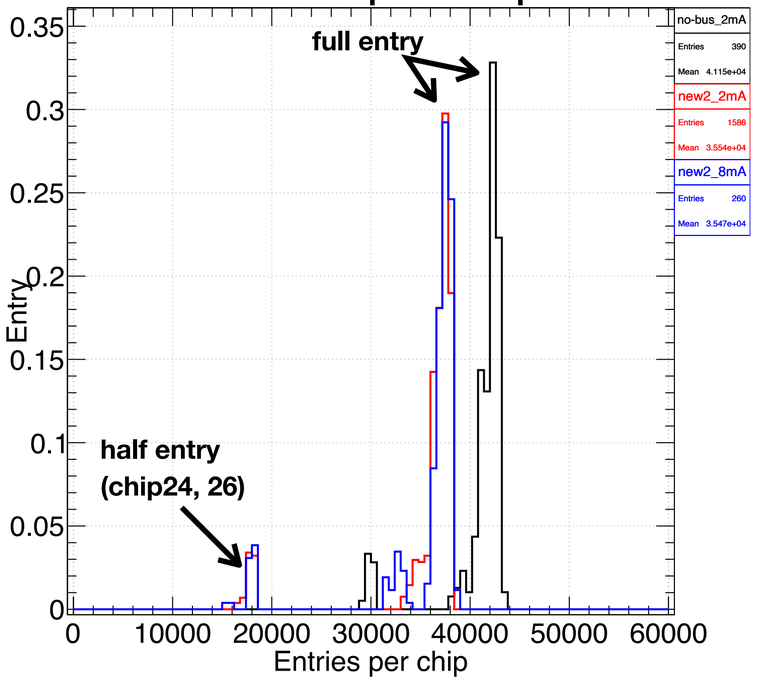
例外) nwu_fphx_raw_20210615-1858_0.dat



※ ファイル名に nwu がついているが、
理研テストベンチで取得したデータ

- バスエクステンダーなし、2 mA
- バスエクステンダーあり、2 mA
- バスエクステンダーあり、8 mA

Entries per chip



※ヒストグラムは面積で規格化している

バスエクステンダー new2, LVDS=2mA で
6 0 回連続でキャリブレーション成功
（除 chip24, 26）

奈良女で new2 を使ったときの結果

2021/4/5 - 2021/4/6 の間に 61 回測定した記録が手元のデータベースにあった

data	lab	roc	roc_port	bus	type	quality	replace(comment, char(10), ",")
nwu_fphx_raw_20210405-1507_0.dat	NWU	9	N/A	new2	Calib	N/A	chip24, 26: half entry,
nwu_fphx_raw_20210405-1510_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	parameter scan: regulator, bas extender, LVDS, and number of init when started.,chip24, 26 have half data,
nwu_fphx_raw_20210405-1517_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26 half entry,
nwu_fphx_raw_20210405-1527_0.dat	NWU	9	N/A	new2	Calib	N/A	chip24, 26: half entry,
nwu_fphx_raw_20210405-1534_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip 24, 26: half entry,
nwu_fphx_raw_20210405-1541_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	LVDS=7mA,chip24, 26: half entry
nwu_fphx_raw_20210405-1543_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip6, 23, 24, 26: half entry,
nwu_fphx_raw_20210405-1551_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1554_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1556_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1604_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	Init done twice at the beginning of run.,LVDS=8mA,chip24, 26: half entry,
nwu_fphx_raw_20210405-1607_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1611_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1613_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chi24, 26: half entry,
nwu_fphx_raw_20210405-1623_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1628_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	check what is executed in calibration test actually since I expected that Init command is done twice at the beginning of the run, but it's not true. Only one time as usual.,data taking itself is fine (I mean as usual),chip24, 26: half entry,
nwu_fphx_raw_20210405-1642_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	Absolutely the init command is done twice at the biginning of this run.,chip24, 26: half entry,
nwu_fphx_raw_20210405-1649_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1652_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1654_0.dat	NWU	9	N/A	new2	Calib	N/A	chip6, 24, 26: half entry,
nwu_fphx_raw_20210405-1657_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	Init is done 3 times at the biginning,chip24, 26: half entry,
nwu_fphx_raw_20210405-1701_0.dat	NWU	9	N/A	new2	Calib	N/A	FFR twice, Init one time,chip6, 24, 26: half entry,
nwu_fphx_raw_20210405-1704_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx2, Initx2,chip6, 7, 24, 26: half entry,
nwu_fphx_raw_20210405-1720_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx2, Initx2,chip24, 26: half entry,
nwu_fphx_raw_20210405-1723_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx2, Initx2,chip24, 26: half entry,
nwu_fphx_raw_20210405-1725_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx2, Initx2,chip24, 26: half entry,
nwu_fphx_raw_20210405-1727_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx2, Initx2,chip24, 26: half entry,
nwu_fphx_raw_20210405-1730_0.dat	NWU	9	N/A	new2	Calib	N/A	FFRx1, Initx2,chip24, 26: half entry

奈良女で new2 を使ったときの結果

2021/4/5 - 2021/4/6 の間に 61 回測定した記録が手元のデータベースにあった

data	lab	roc	roc_port	bus	type	quality	replace(comment, char(10), ",")
nwu_fphx_raw_20210405-1801_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx2, Initx1,chip24, 26: half entry,
nwu_fphx_raw_20210405-1806_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx2, Initx1,chip24, 26: half entry,
nwu_fphx_raw_20210405-1811_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx2, Initx1,chip24, 26: half entry,
nwu_fphx_raw_20210405-1814_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx2, Initx1,chip6, 7, 24, 26: ,
nwu_fphx_raw_20210405-1825_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx3, Initx3,chip24, 26: half entry,
nwu_fphx_raw_20210405-1827_0.dat	NWU	9	N/A	new2	Calib	N/A	FFRx3, Initx3,chip24, 26: half entry,
nwu_fphx_raw_20210405-1830_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx3, Initx3,chip24, 26: half entry,
nwu_fphx_raw_20210405-1832_0.dat	NWU	9	N/A	new2	Calib	N/A	FFRx3, Initx3,chip24, 26: half entry,
nwu_fphx_raw_20210405-1835_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx3, Initx3,chip24, 26: half entry,
nwu_fphx_raw_20210405-1850_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	INTT PPL5-N, FFRx1, Initx1,chip24, 26: half entry,
nwu_fphx_raw_20210405-1858_0.dat	NWU	9	N/A	new2	Calib	N/A	chip6, 23, 24, 26: half entry,
nwu_fphx_raw_20210405-1914_0.dat	NWU	9	N/A	new2	Calib	N/A	chip24, 26: half entry, bit noisy,
nwu_fphx_raw_20210405-1916_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1919_0.dat	NWU	9	N/A	new2	Calib	N/A	chip24, 26: half entry,
nwu_fphx_raw_20210405-1922_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	LVDS=7mA,chip6, 24, 26: half entry,
nwu_fphx_raw_20210405-1927_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip6, 24, 26: half entry
nwu_fphx_raw_20210405-1931_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1933_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1936_0.dat	NWU	9	A3	new2	Calib	missing chips/channels	chip24, 26: half entry
nwu_fphx_raw_20210406-1216_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=8mA,chip24, 26: half entry
nwu_fphx_raw_20210406-1221_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=8mA,chip24, 26: half entry,bit noisy
nwu_fphx_raw_20210406-1224_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=8mA,chip24, 26: half entry
nwu_fphx_raw_20210406-1228_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=8mA,chip24, 26: half entry
nwu_fphx_raw_20210406-1232_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=8mA,chip24, 26: half entry
nwu_fphx_raw_20210406-1236_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=7mA,chip24, 26: half entry,
nwu_fphx_raw_20210406-1240_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=7mA,chip24, 26: half entry
nwu_fphx_raw_20210406-1245_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=7mA,chip24, 26: half entry,
nwu_fphx_raw_20210406-1249_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=7mA,chip24, 26: half entry,bit noisy
nwu_fphx_raw_20210406-1253_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=7mA,chip24, 26: half entry
nwu_fphx_raw_20210406-1257_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=6mA,chip12, 24: half entry,chip26: no data
nwu_fphx_raw_20210406-1302_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=6mA,chip24, 26: half entry,noisy,
nwu_fphx_raw_20210406-1307_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=5mA,chip24, 26: half entry,chip12: no data,
nwu_fphx_raw_20210406-1312_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=4mA,chip12, 24: half entry,chip26: no data

奈良女で new2 を使ったときの結果

2021/4/5 - 2021/4/6 の間に 61 回測定した記録が手元のデータベースにあった

結果

Perfect: 0
Fine: 0
missing chips/channels: 51

- chip24 and/or 26 のみ half entry: 40
- chip24, 26 以外のチップも half entry: 11

No data: 0
quality の記載なし: 10

- chip24 and/or 26 のみ half entry: 7
- chip24, 26 以外のチップも half entry: 3

奈良女では 47 / 61 = 0.77 が成功

理研の成功率 60 / 61 = 0.98 は明らかに状況が異なる

ROC FPGA の電源

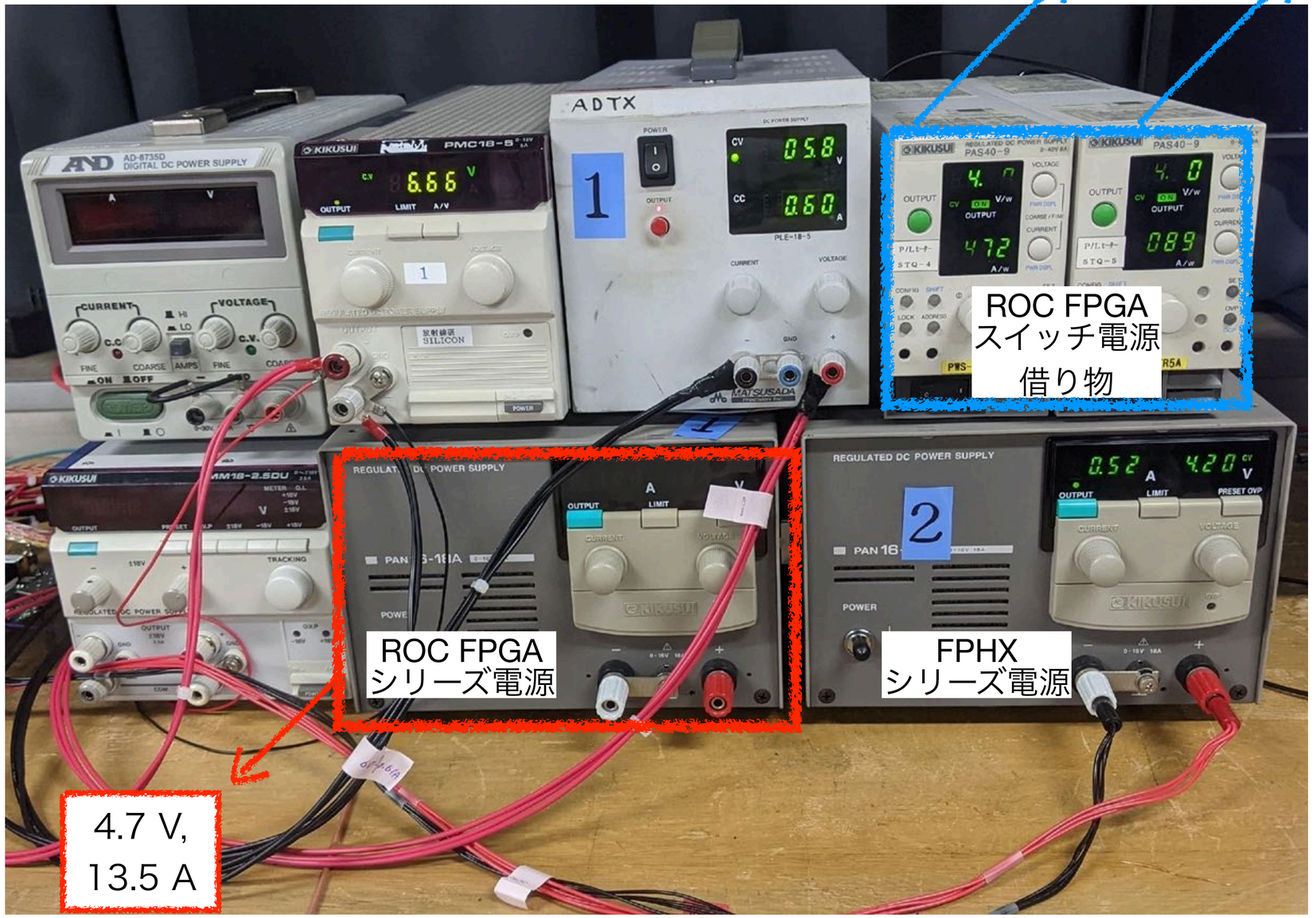
	ROC FPGA 用	FPHX 用	FPHX 用
奈良女	GW Instek SPS-1230 スイッチング電源 	PMX19-5 シリーズ電源 	PMM18-2.5 DN シリーズ電源
理研	PAN 16-18A シリーズ電源	PAN 16-18A シリーズ電源	
理研 （借り物）	PAS40-9 スイッチング電源		

理研セットアップで
スイッチング電源を使ってみる

4.7 V,
5.5 A

4.7 V,
8.1 A

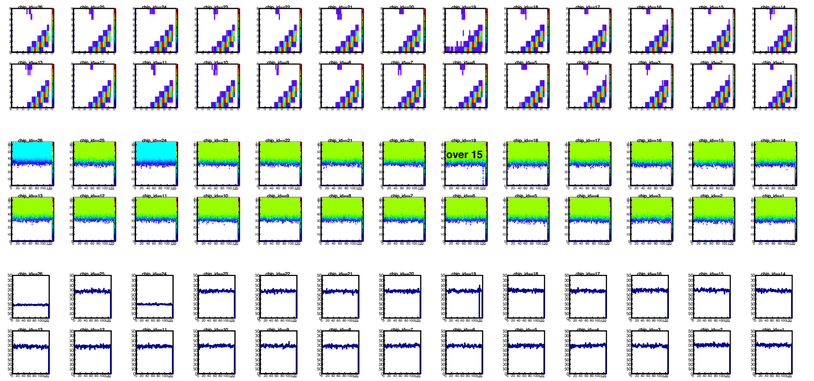
→13.6 A



ROC FPGA 用電源をスイッチ電源 2 台に変更

Ladder: PPB2-L4N
ROC: NW1 port C3
Conversion cable: small #8
Bus extender: new2
LVDS: 2 mA

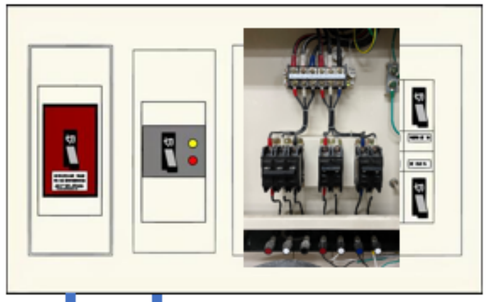
結果：10 / 10 回 が

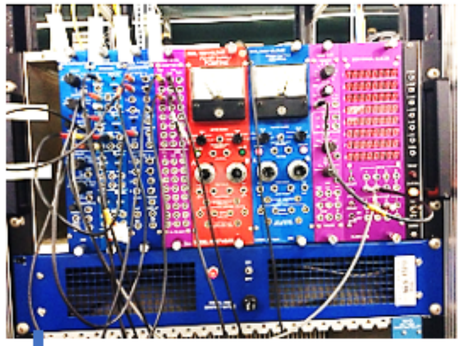


のようにchip24, 26 以外で良好な結果が得られた

奈良女テストベンチの電源まわり

電源の接続



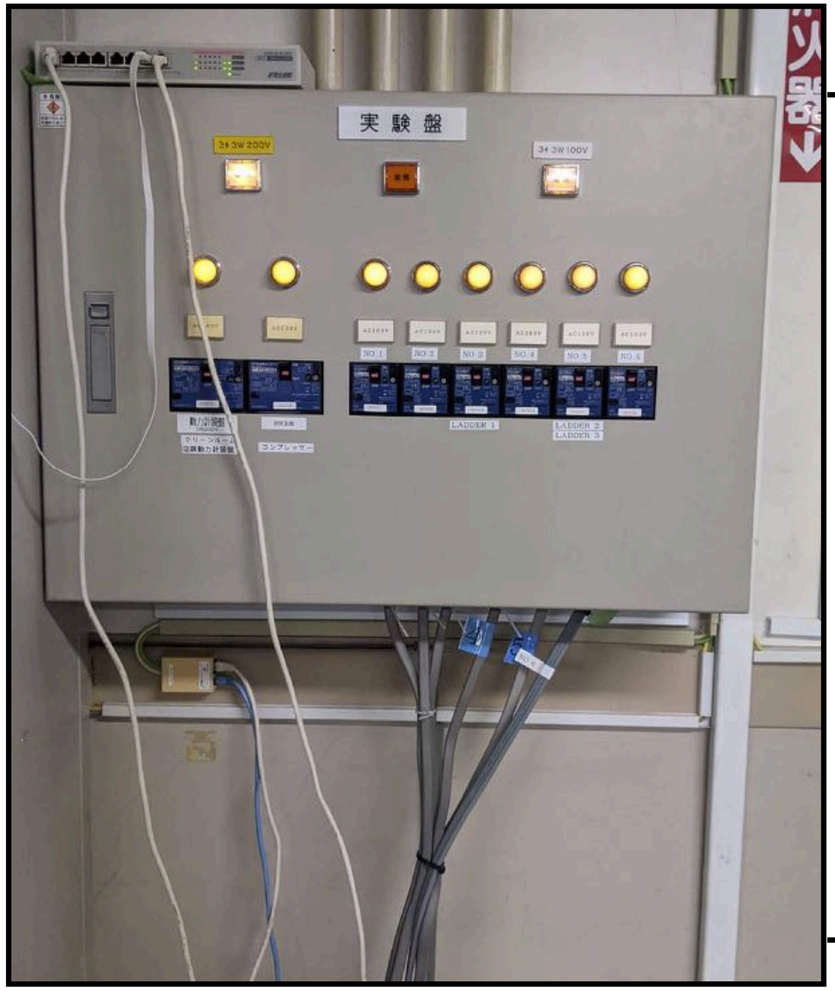


Ladder 1

4つ(ROC 3＋Ladder 1)

- ラダーへの電源が2系統に分かれている。

理研テストベンチの電源まわり

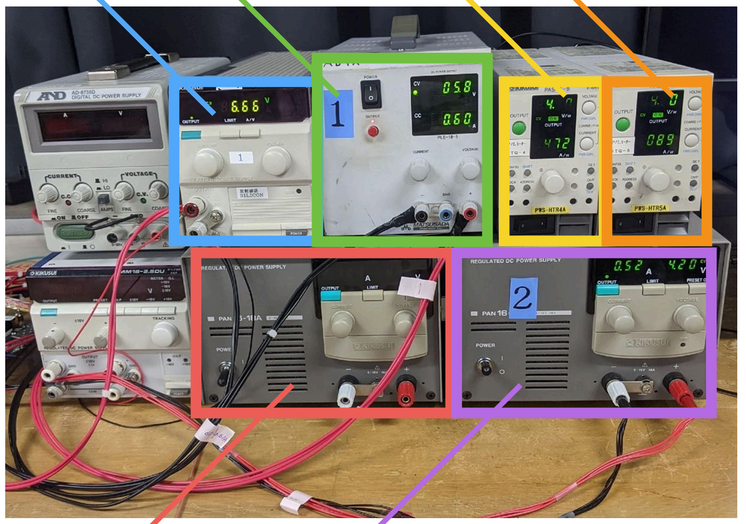


計 6 系統、各 20 A

#6

#2

NIM, VME クレート



冷却ファン

backup

data	lab	roc	roc_port	bus	type	quality	replace(comment, char(10), ",")
nwu_fphx_raw_20210405-1507_0.dat	NWU	9	N/A	new2	Calib	N/A	chip24, 26: half entry,
nwu_fphx_raw_20210405-1510_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	parameter scan: regulator, bas extender, LVDS, and number of init when started.,chip24, 26 have half data,
nwu_fphx_raw_20210405-1517_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26 half entry,
nwu_fphx_raw_20210405-1527_0.dat	NWU	9	N/A	new2	Calib	N/A	chip24, 26: half entry,
nwu_fphx_raw_20210405-1534_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip 24, 26: half entry,
nwu_fphx_raw_20210405-1541_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	LVDS=7mA,chip24, 26: half entry
nwu_fphx_raw_20210405-1543_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	
nwu_fphx_raw_20210405-1551_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1554_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1556_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1604_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	Init done twice at the beginning of run.,LVDS=8mA,chip24, 26: half entry,
nwu_fphx_raw_20210405-1607_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1611_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1613_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chi24, 26: half entry,
nwu_fphx_raw_20210405-1623_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1628_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	check what is executed in calibration test actually since I expected that Init command is done twice at the beginning of the run, but it's not true. Only one time as usual.,data taking itself is fine (I mean as usual),chip24, 26: half entry,
nwu_fphx_raw_20210405-1642_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	Absolutely the init command is done twice at the biginning of this run.,chip24, 26: half entry,
nwu_fphx_raw_20210405-1649_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1652_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1654_0.dat	NWU	9	N/A	new2	Calib	N/A	
nwu_fphx_raw_20210405-1657_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	Init is done 3 times at the biginning,chip24, 26: half entry,
nwu_fphx_raw_20210405-1701_0.dat	NWU	9	N/A	new2	Calib	N/A	
nwu_fphx_raw_20210405-1704_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	
nwu_fphx_raw_20210405-1720_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx2, Initx2,chip24, 26: half entry,
nwu_fphx_raw_20210405-1723_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx2, Initx2,chip24, 26: half entry,
nwu_fphx_raw_20210405-1725_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx2, Initx2,chip24, 26: half entry,
nwu_fphx_raw_20210405-1727_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx2, Initx2,chip24, 26: half entry,
nwu_fphx_raw_20210405-1730_0.dat	NWU	9	N/A	new2	Calib	N/A	FFRx1, Initx2,chip24, 26: half entry
nwu_fphx_raw_20210405-1801_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx2, Initx1,chip24, 26: half entry,
nwu_fphx_raw_20210405-1806_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx2, Initx1,chip24, 26: half entry,
nwu_fphx_raw_20210405-1811_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx2, Initx1,chip24, 26: half entry,
nwu_fphx_raw_20210405-1814_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	
nwu_fphx_raw_20210405-1825_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx3, Initx3,chip24, 26: half entry,
nwu_fphx_raw_20210405-1827_0.dat	NWU	9	N/A	new2	Calib	N/A	FFRx3, Initx3,chip24, 26: half entry,
nwu_fphx_raw_20210405-1830_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx3, Initx3,chip24, 26: half entry,
nwu_fphx_raw_20210405-1832_0.dat	NWU	9	N/A	new2	Calib	N/A	FFRx3, Initx3,chip24, 26: half entry,
nwu_fphx_raw_20210405-1835_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	FFRx3, Initx3,chip24, 26: half entry,
nwu_fphx_raw_20210405-1850_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	INTT PPL5-N, FFRx1, Initx1,chip24, 26: half entry,
nwu_fphx_raw_20210405-1858_0.dat	NWU	9	N/A	new2	Calib	N/A	
nwu_fphx_raw_20210405-1914_0.dat	NWU	9	N/A	new2	Calib	N/A	chip24, 26: half entry, bit noisy,
nwu_fphx_raw_20210405-1916_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1919_0.dat	NWU	9	N/A	new2	Calib	N/A	chip24, 26: half entry,
nwu_fphx_raw_20210405-1922_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	
nwu_fphx_raw_20210405-1927_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	
nwu_fphx_raw_20210405-1931_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1933_0.dat	NWU	9	N/A	new2	Calib	missing chips/channels	chip24, 26: half entry,
nwu_fphx_raw_20210405-1936_0.dat	NWU	9	A3	new2	Calib	missing chips/channels	chip24, 26: half entry
nwu_fphx_raw_20210406-1216_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=8mA,chip24, 26: half entry
nwu_fphx_raw_20210406-1221_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=8mA,chip24, 26: half entry,bit noisy
nwu_fphx_raw_20210406-1224_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=8mA,chip24, 26: half entry
nwu_fphx_raw_20210406-1228_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=8mA,chip24, 26: half entry
nwu_fphx_raw_20210406-1232_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=8mA,chip24, 26: half entry
nwu_fphx_raw_20210406-1236_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=7mA,chip24, 26: half entry,
nwu_fphx_raw_20210406-1240_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=7mA,chip24, 26: half entry
nwu_fphx_raw_20210406-1245_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=7mA,chip24, 26: half entry,
nwu_fphx_raw_20210406-1249_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=7mA,chip24, 26: half entry,bit noisy
nwu_fphx_raw_20210406-1253_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=7mA,chip24, 26: half entry
nwu_fphx_raw_20210406-1257_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	
nwu_fphx_raw_20210406-1302_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	LVDS=6mA,chip24, 26: half entry,noisy,
nwu_fphx_raw_20210406-1307_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	
nwu_fphx_raw_20210406-1312_0.dat	NWU	9	C3	new2	Calib	missing chips/channels	

奈良女で new4 を使ったときの結果

2021/4/6 - 2021/4/7 の間に 55 回測定した記録が手元のデータベースにあった

2021/4/7 17:00 以前のデータ

data	lab	roc	roc_port	bus	quality	replace(comment, char(10), ",")
nwu_fphx_raw_20210406-1817_0.dat	NWU	9	C3	new4	Perfect	LVDS=8mA,Dig-REG:5.0V - 0.556A->0.645A,Ana-REG:5.0V - 0.21A,,,,
nwu_fphx_raw_20210406-1824_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=8mA,chip12 half,,,,
nwu_fphx_raw_20210406-1829_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=8mA,chip24, 26 half,,,,,
nwu_fphx_raw_20210406-1833_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=8mA,chip12, 24 half,,,,,,
nwu_fphx_raw_20210406-1837_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=8mA,chip24 half,,,,,,,
nwu_fphx_raw_20210406-1842_0.dat	NWU	9	C3	new4	Perfect	LVDS=7mA,,,,,,,,
nwu_fphx_raw_20210406-1847_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=7mA,chip 12, 24, 26 half,,,,,,,,
nwu_fphx_raw_20210406-1851_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=7mA,chip 8, 10, 21, 24 half,chip 12 nothing,,,,,,,,
nwu_fphx_raw_20210406-1856_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=7mA,chip 12, 24, 26 half,,,,,,,,
nwu_fphx_raw_20210406-1900_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=7mA,chip 12, 24 half,,,,,,,,,
nwu_fphx_raw_20210407-1335_0.dat	NWU	9	C3	new4	Perfect	LVDS=8mA,bit noisy,
nwu_fphx_raw_20210407-1340_0.dat	NWU	9	C3	new4	Perfect	LVDS=8mA,bit noisy,,
nwu_fphx_raw_20210407-1344_0.dat	NWU	9	C3	new4	Perfect	LVDS=8mA,,
nwu_fphx_raw_20210407-1349_0.dat	NWU	9	C3	new4	Perfect	LVDS=7mA,noisy,
nwu_fphx_raw_20210407-1353_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=7mA,chip23, 24: half entry,,
nwu_fphx_raw_20210407-1357_0.dat	NWU	9	C3	new4	Perfect	LVDS=7mA,
nwu_fphx_raw_20210407-1405_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=6mA,chip12, 24: half entry,,,
nwu_fphx_raw_20210407-1410_0.dat	NWU	9	C3	new4	Perfect	LVDS=6mA,
nwu_fphx_raw_20210407-1414_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=6mA,chip22: half entry,
nwu_fphx_raw_20210407-1419_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=5mA,chip12, 24: half entry,
nwu_fphx_raw_20210407-1422_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=5mA,chip12, 24: half entry,chip14, <ch65: no data,
nwu_fphx_raw_20210407-1427_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=5mA,chip12, 24: half entry,
nwu_fphx_raw_20210407-1647_0.dat	NWU	9	C3	new4	Perfect	LVDS=8mA,bit noisy,,
nwu_fphx_raw_20210407-1432_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=4mA,chip12, 24, 26: half entry,,
nwu_fphx_raw_20210407-1652_0.dat	NWU	9	C3	new4	Perfect	LVDS=8mA,bit noisy,,,
nwu_fphx_raw_20210407-1656_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=8mA,chip22: half entry,

奈良女で new4 を使ったときの結果

2021/4/6 - 2021/4/7 の間に 55 回測定した記録が手元のデータベースにあった

2021/4/7 17:00 以降のデータ

data	lab	roc	roc_port	bus	quality	replace(comment, char(10), ",")
nwu_fphx_raw_20210407-1700_0.dat	NWU	9	C3	new4	Perfect	LVDS=8mA,
nwu_fphx_raw_20210407-1703_0.dat	NWU	9	C3	new4	Perfect	LVDS=7mA,
nwu_fphx_raw_20210407-1707_0.dat	NWU	9	C3	new4	Perfect	LVDS=7mA,,
nwu_fphx_raw_20210407-1710_0.dat	NWU	9	C3	new4	Perfect	LVDS=7mA,noisy,
nwu_fphx_raw_20210407-1714_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=6mA,chip12, 19, 20, 21, 22, 23, 24,26: half entry,,
nwu_fphx_raw_20210407-1718_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=6mA,chip12, 23, 24,26: half entry,
nwu_fphx_raw_20210407-1721_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=6mA,chip12, 24,26: half entry,,
nwu_fphx_raw_20210407-1726_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=5mA,chip22: no data,,,
nwu_fphx_raw_20210407-1730_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=5mA,chip12, 24: half entry,chip22: no data,,,,
nwu_fphx_raw_20210407-1801_0.dat	NWU	9	C3	new4	No data	LVDS=8mA,,
nwu_fphx_raw_20210407-1811_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=8mA,chip12, 24,26,
nwu_fphx_raw_20210407-1815_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=8mA,chip24: half entry,,
nwu_fphx_raw_20210407-1819_0.dat	NWU	9	C3	new4	Perfect	LVDS=8mA,bit noisy,
nwu_fphx_raw_20210407-1824_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=7mA,chip24: half,bit noisy,,
nwu_fphx_raw_20210407-1828_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=7mA,chip24: half,bit noisy,,,
nwu_fphx_raw_20210407-1831_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=7mA,chip12, 26: half,bit noisy,,,,
nwu_fphx_raw_20210407-1836_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=6mA,chip21, 26: half,chip12: no data,bit noisy,,,,,
nwu_fphx_raw_20210407-1841_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=6mA,chip12, 26: half,noisy,,,,,,
nwu_fphx_raw_20210407-1845_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=6mA,chip24: half,,,
nwu_fphx_raw_20210407-1855_0.dat	NWU	9	C3	new4	Perfect	LVDS=8mA,,
nwu_fphx_raw_20210407-1858_0.dat	NWU	9	C3	new4	Fine	LVDS=8mA,only chi19, ch119 is lost,,
nwu_fphx_raw_20210407-1902_0.dat	NWU	9	C3	new4	Perfect	LVDS=8mA,,,
nwu_fphx_raw_20210407-1906_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=7mA,chip24: half entry,chip22: no data,noisy,
nwu_fphx_raw_20210407-1910_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=7mA,chip22, 24: half entry,noisy,,
nwu_fphx_raw_20210407-1914_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=7mA,chip22, 24: half entry,
nwu_fphx_raw_20210407-1923_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=6mA,chip22: no data,
nwu_fphx_raw_20210407-1927_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=6mA,chip24: half data,chip22: no data,
nwu_fphx_raw_20210407-1931_0.dat	NWU	9	C3	new4	No data	LVDS=6mA,,
nwu_fphx_raw_20210407-1936_0.dat	NWU	9	C3	new4	missing chips/channels	LVDS=6mA,chip24: half data,chip22: no data,,

奈良女で new4 を使ったときの結果

2021/4/6 - 2021/4/7 の間に 55 回測定した記録が手元のデータベースにあった

結果

Perfect: 17
Fine: 1
missing chips/channels: 35
- chip24 and/or 26 のみ half entry: 6
- chip24, 26 以外のチップも half entry: 29

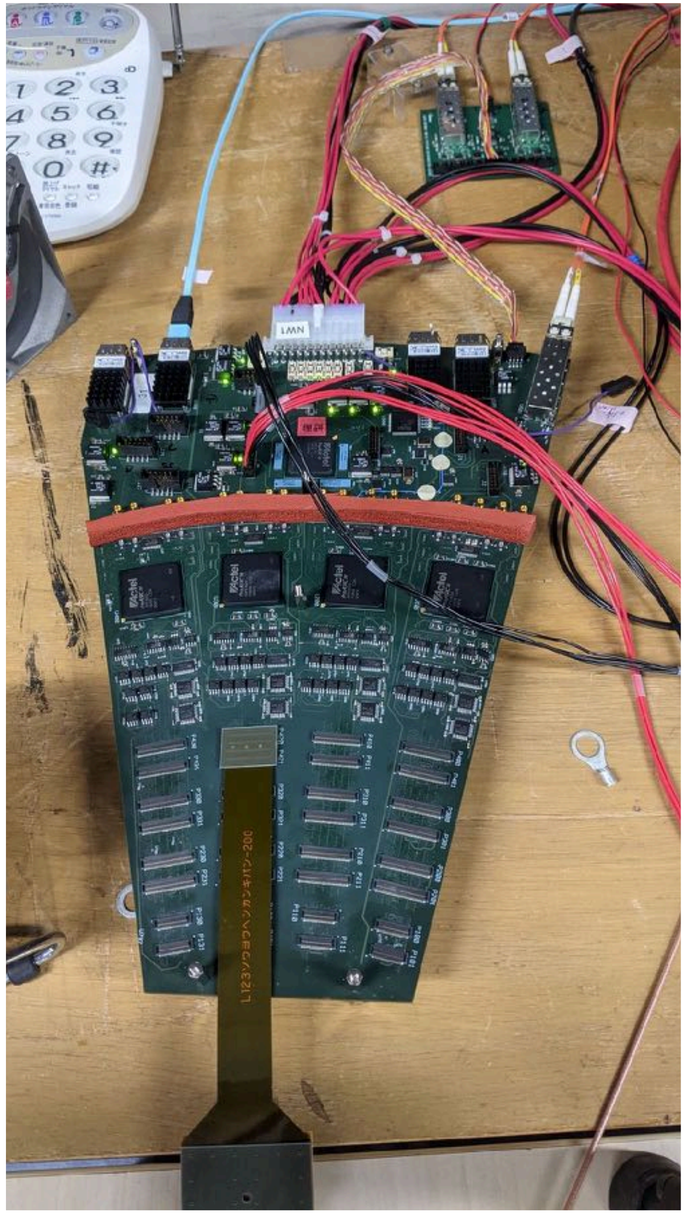
No data: 2

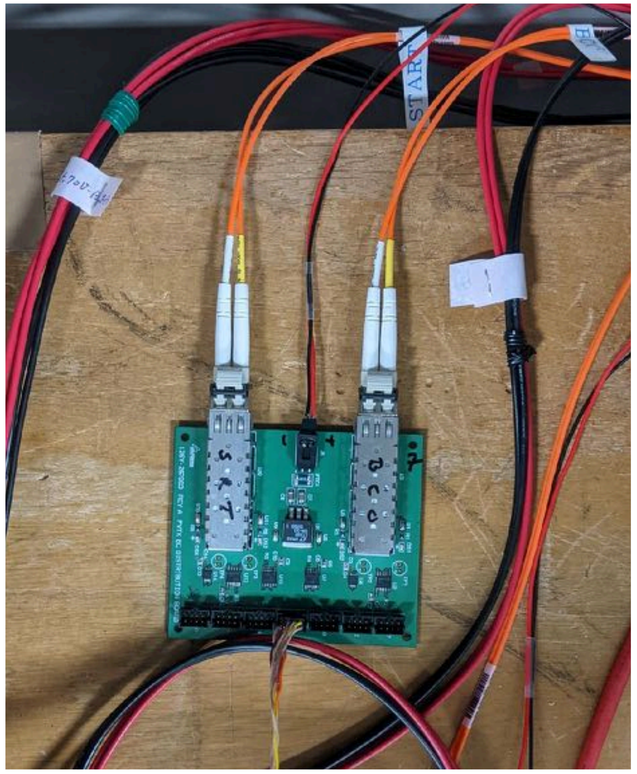
奈良女は { Perfect(17) + Fine(1) + chip24 and/or 26 missed(6) } / total(55) = 24 / 55 回が成功

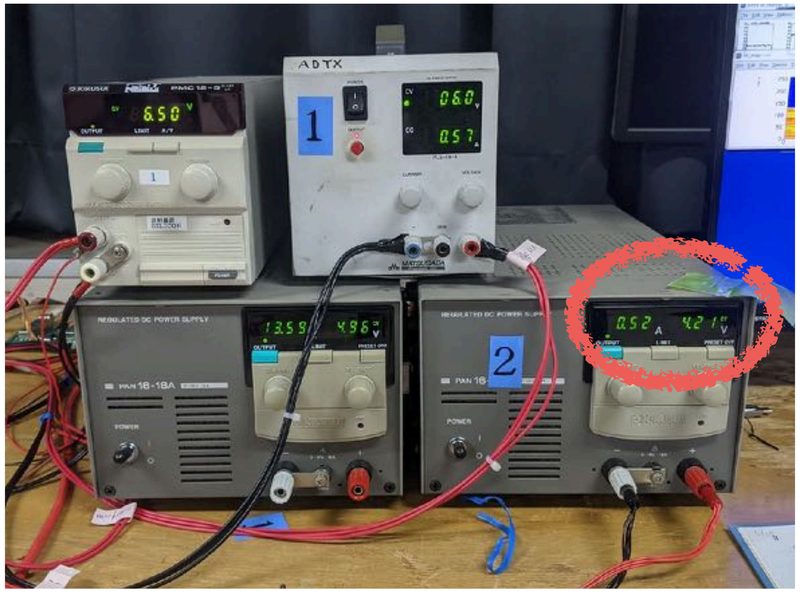
理研の成功率 60 / 61 は明らかに状況が異なる

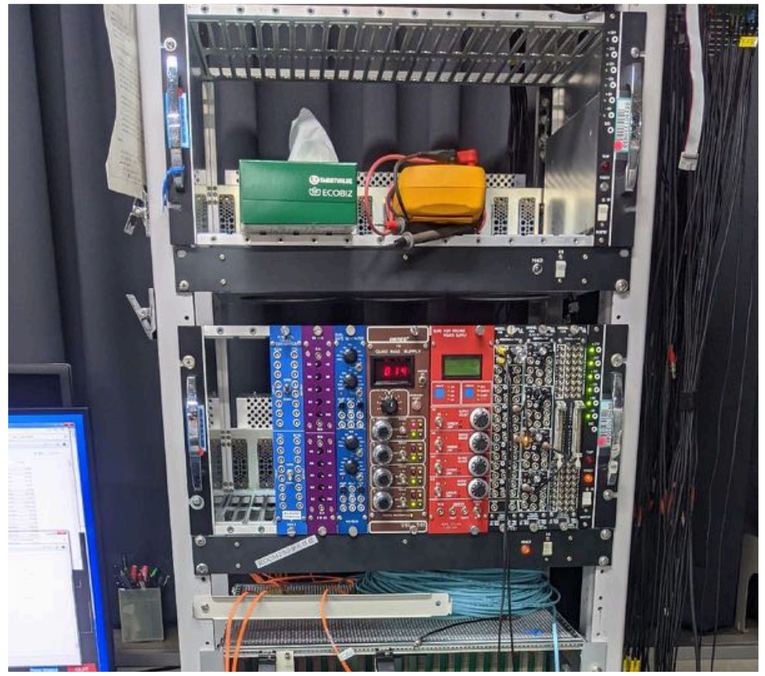
セットアップ構築

セットアップ構築




START

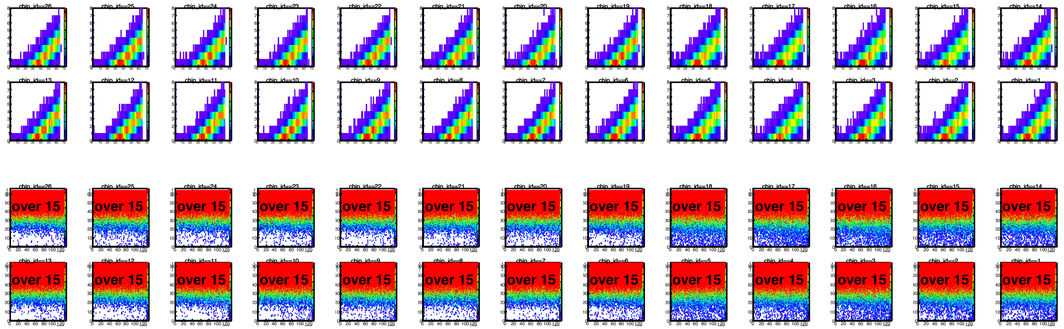

ADTX
1
2




FEMIB 3
FPGA ADDR
ETH
USB
BCO
START
ROC ADDR
JTAG
RESET
G-LINK
FVTX FEM INTERFACE
FVTX FEM
DATA CH 1
FIO STATUS
SC
DATA

キャリブレーション

nwu_fphx_raw_20210615-1326_0.dat

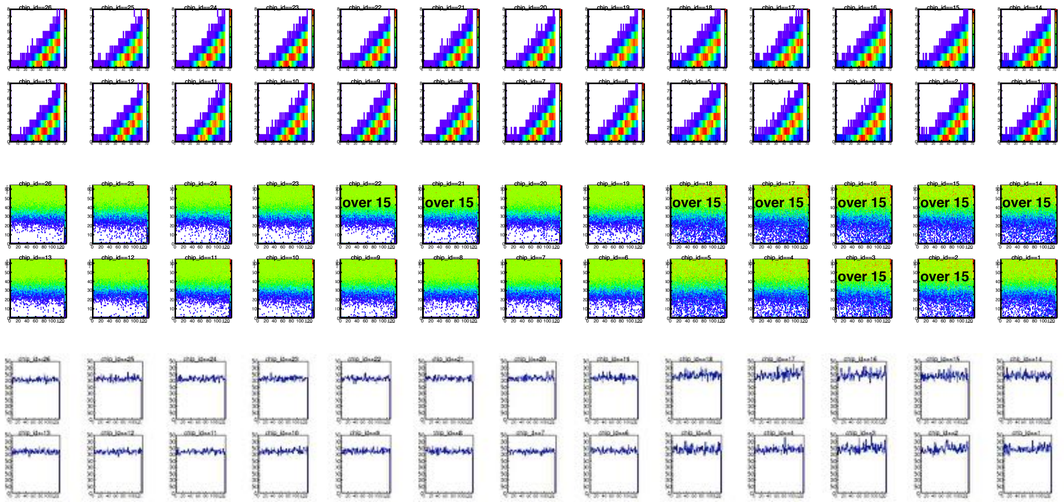


→作業開始 1.5 日でデータが取れるようになった

最適な delay を使っていない (3 を使用)ので、

データ量がおかしくなっている

nwu_fphx_raw_20210615-1514_0.dat



delay 1, 2, 3, 4, 5 でデータを取ってみた

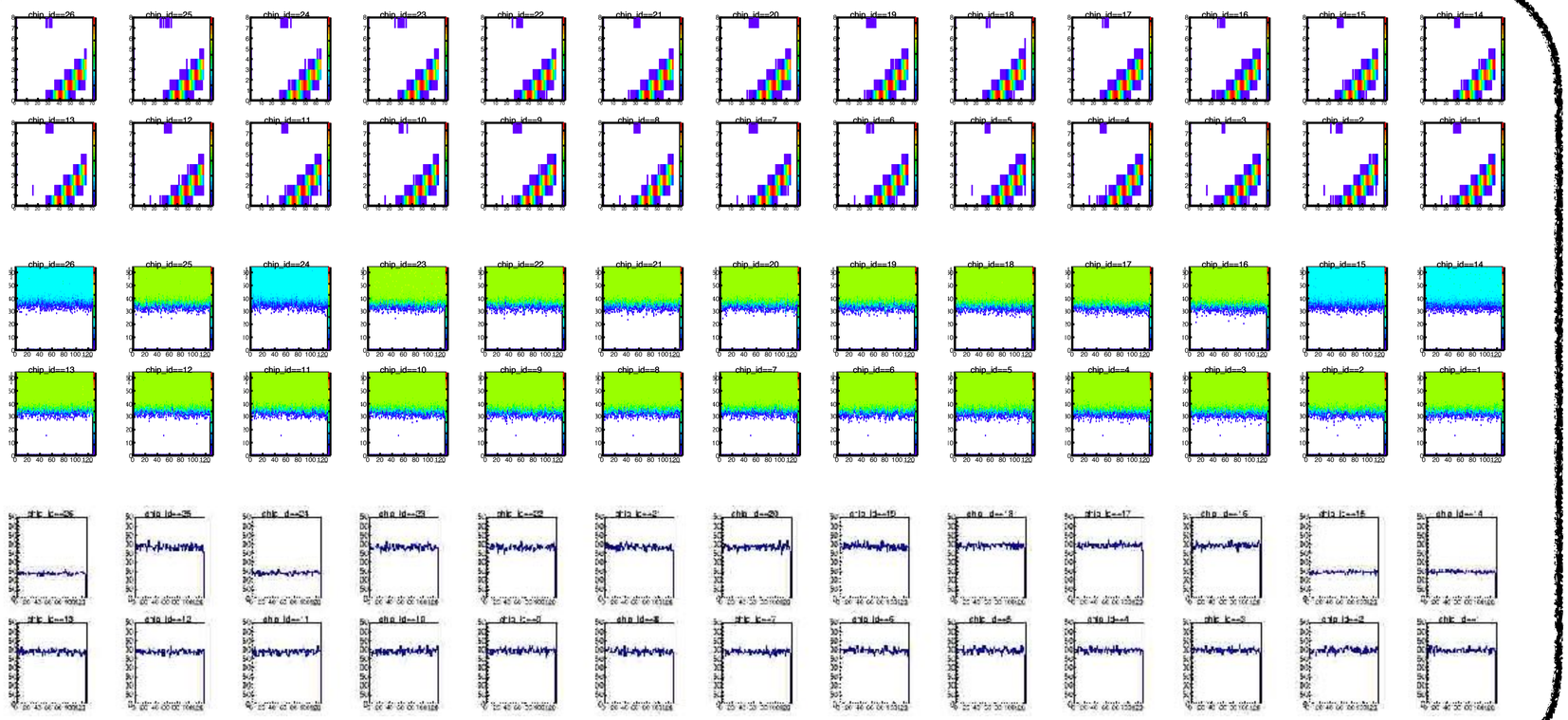
→delay 5 で正常な結果が得られる

※ この測定でバイアスはかけていない

バスエクステンダーありでキャリブレーション

new2 (chip24, 26 のラインに問題あり) を奈良女から持ってきた

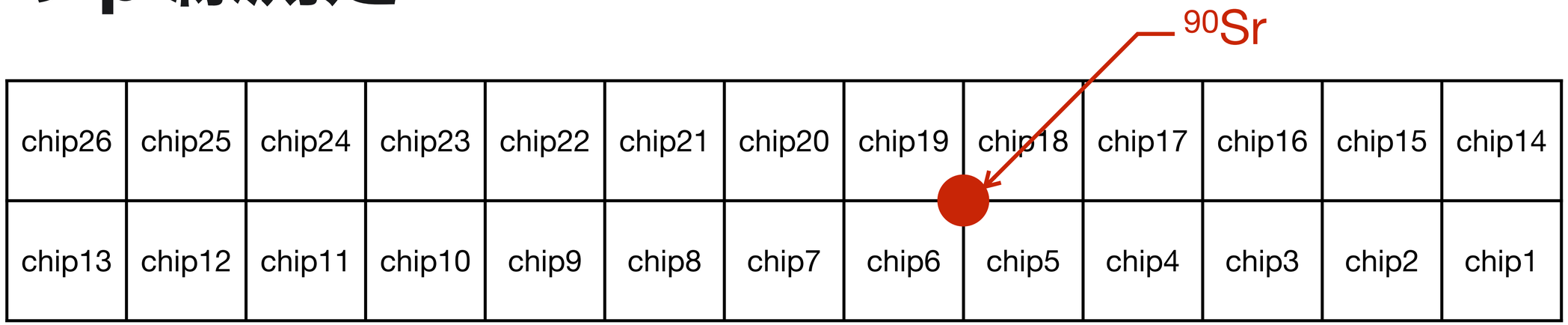
nwu_fphx_raw_20210615-1858_0.dat

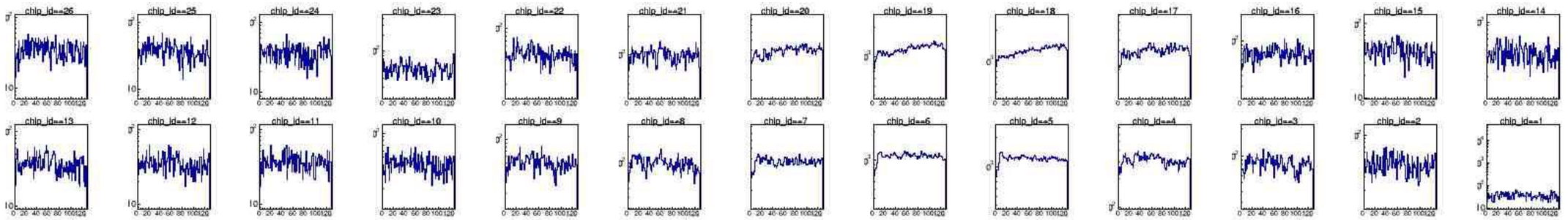


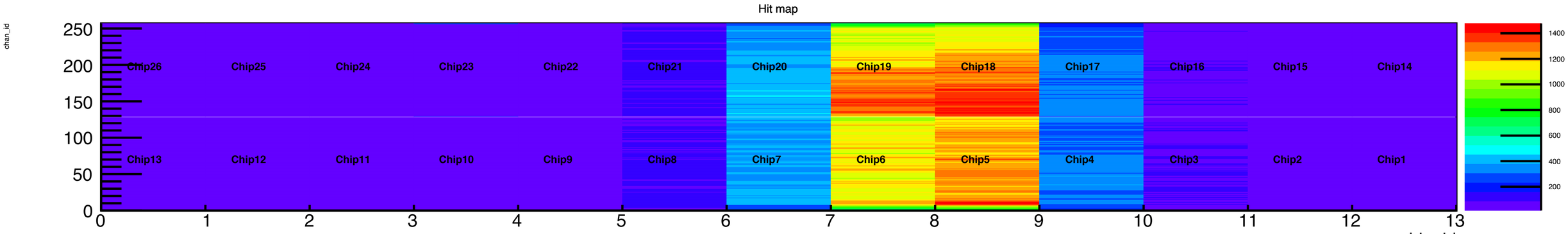
→ データが取れた！

^{90}Sr の β 線測定

奈良女で使用している BNL_original_FPGA_20201005_3 の外部トリガー用 FPGA コードを使用



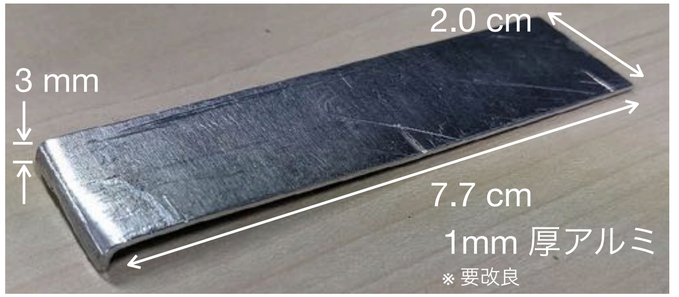




→データが取れた！

その後

- **環境整備**
  - ソフトウェア（SQLite3 導入、テキストエディタ導入、糠塚製 data_manager 導入）
  - バイアス用 BNC-SHV ケーブルの修理
  - 外部トリガー用 シンチレーターと PMT の接着
  - 冷却ファンにスイッチ接続
  - ケーブル剥がし試作
- **Bus extender なしでキャリブレーション（ROC NW1 の全ポート）**
- **Bus extender ありでキャリブレーション（LDVS=2mA, 8mA で大量にデータ取得）**

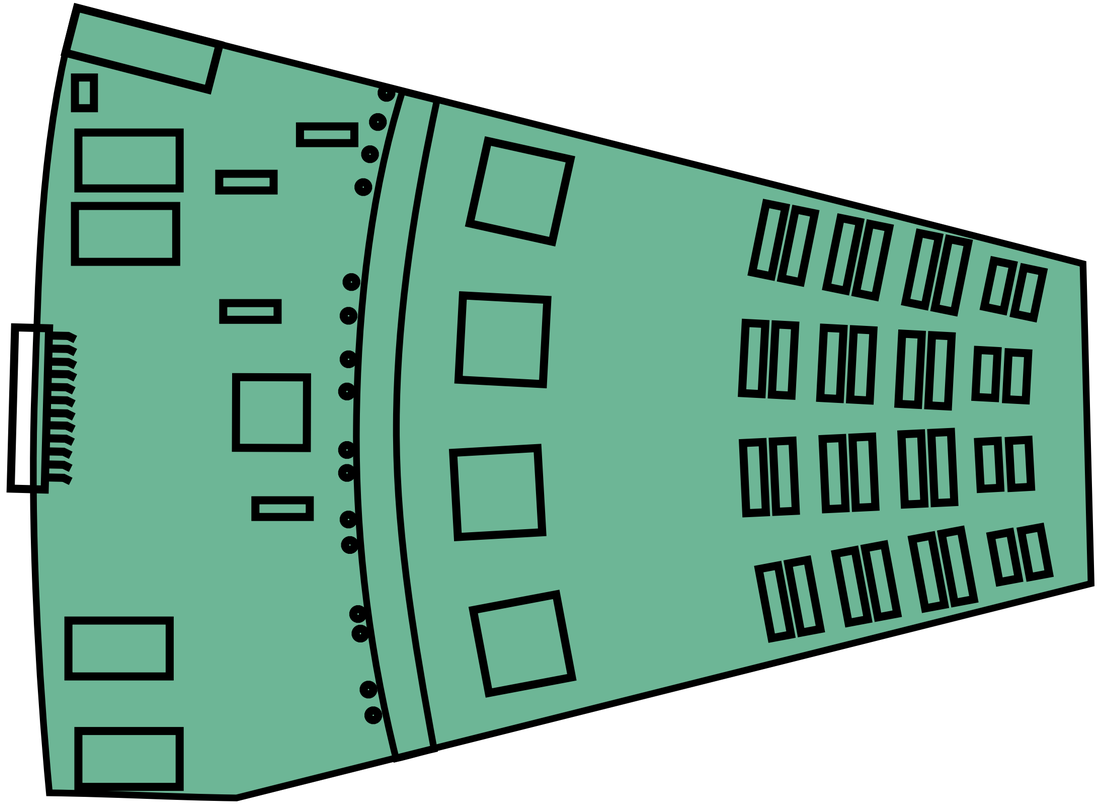


その後、ROC 全ポートでキャリブレーション

C1, C2, C3: 問題なし

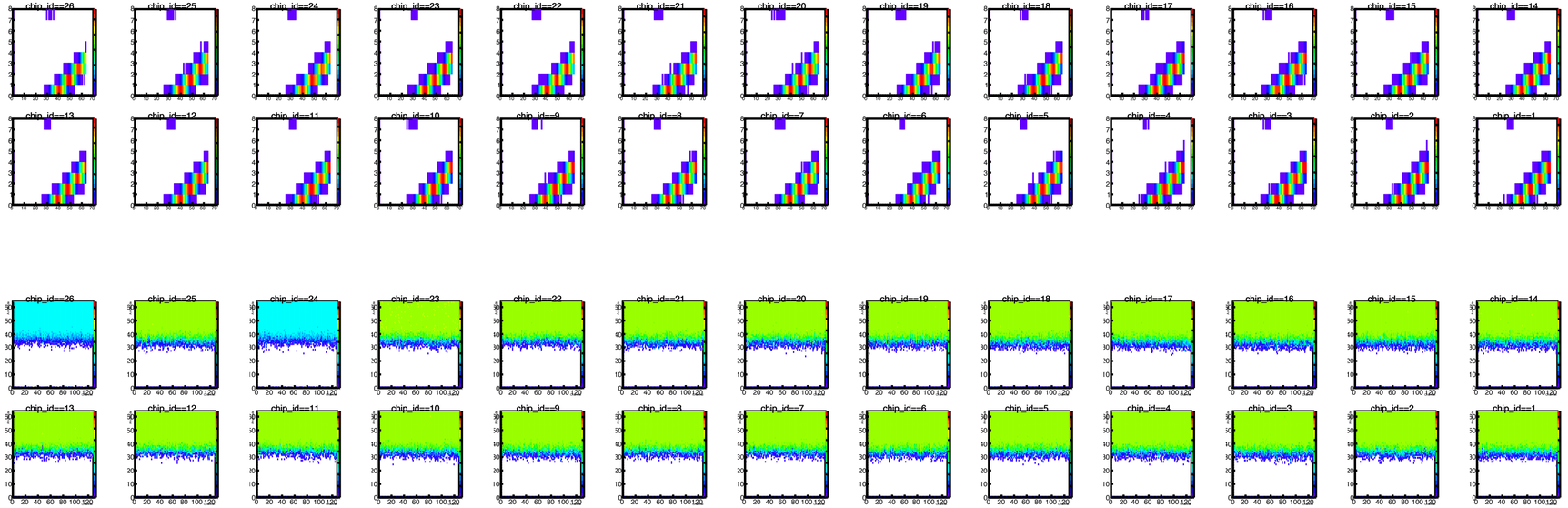
A1, A3: 全くデータが得られない（おそらく A2 もだめ）

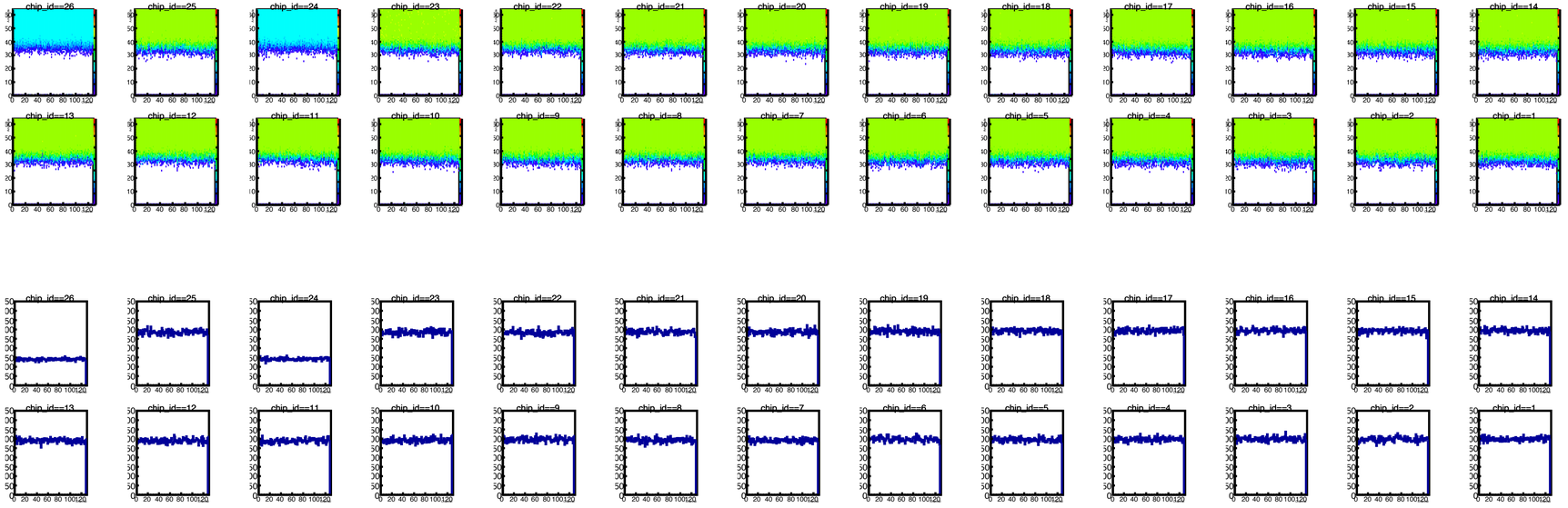
なぜ？



その後、バスエクステンダーありでキャリブレーション

riken_fphx_raw_20210621-2331_0.dat





LVDS = 2 mA (デフォルト)

INTT：Pre2

ROC：NW1

ROC ポート：C3

conv. cable：small8

chip24, 26 がうまくいか

ないのは既知

ほかは OK

その後、バスエクステンダーありでキャリブレーション

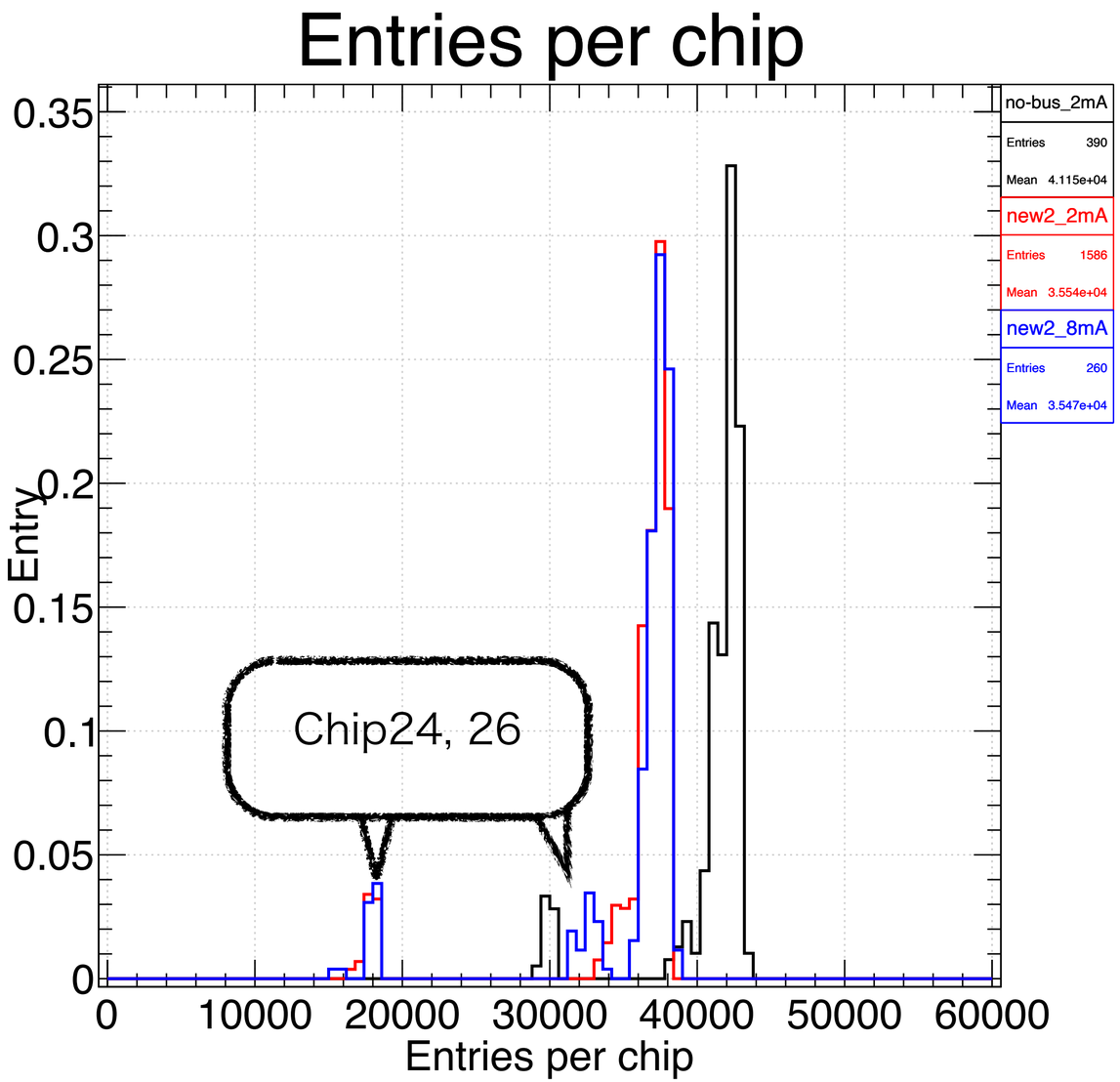
data	ladder	roc	roc_port	LVDS	quality	
riken_fphx_raw_20210621-2331_0.dat	pre2	NW1	C3	3	Fine	chip24, 26: half
riken_fphx_raw_20210621-2338_0.dat	pre2	NW1	C3	3	Fine	chip24, 26: half
riken_fphx_raw_20210621-2342_0.dat	pre2	NW1	C3	3	Fine	chip24, 26: half
riken_fphx_raw_20210621-2347_0.dat	pre2	NW1	C3	3	Fine	chip24, 26: half
riken_fphx_raw_20210621-2351_0.dat	pre2	NW1	C3	3	Fine	chip24, 26: half
riken_fphx_raw_20210621-2355_0.dat	pre2	NW1	C3	3	Fine	chip24, 26: half
riken_fphx_raw_20210621-2358_0.dat	pre2	NW1	C3	3	Fine	chip24, 26: half
riken_fphx_raw_20210622-0002_0.dat	pre2	NW1	C3	3	Fine	chip24, 26: half
riken_fphx_raw_20210622-0006_0.dat	pre2	NW1	C3	3	Fine	chip24, 26: half
riken_fphx_raw_20210622-0010_0.dat	pre2	NW1	C3	3	Fine	chip24, 26: half
riken_fphx_raw_20210622-0014_0.dat	pre2	NW1	C3	3	Fine	chip24, 26: half
riken_fphx_raw_20210622-0027_0.dat	pre2	NW1	C3	255	Fine	chip24, 26: half
riken_fphx_raw_20210622-0031_0.dat	pre2	NW1	C3	255	Fine	chip24, 26: half
riken_fphx_raw_20210622-0035_0.dat	pre2	NW1	C3	255	Fine	chip24, 26: half
riken_fphx_raw_20210622-0038_0.dat	pre2	NW1	C3	255	Fine	chip24, 26: half
riken_fphx_raw_20210622-0042_0.dat	pre2	NW1	C3	255	Fine	chip24, 26: half
riken_fphx_raw_20210622-0046_0.dat	pre2	NW1	C3	255	Fine	chip24, 26: half
riken_fphx_raw_20210622-0050_0.dat	pre2	NW1	C3	255	Fine	chip24, 26: half
riken_fphx_raw_20210622-0054_0.dat	pre2	NW1	C3	255	Fine	chip24, 26: half
riken_fphx_raw_20210622-0058_0.dat	pre2	NW1	C3	255	Fine	chip24, 26: half
riken_fphx_raw_20210622-0101_0.dat	pre2	NW1	C3	255	Fine	chip24, 26: half

LVDS = 2 mA
11 回測定した

LVDS = 8 mA
10 回測定した

全部うまくいった

その後、バスエクステンダーありでキャリブレーション



※ヒストグラムは面積で規格化している

- バスエクステンダーなし、2 mA
- バスエクステンダーあり、2 mA
- バスエクステンダーあり、8 mA

UPDATED

チップごとのデータ数のヒストグラム

- 良好なキャリブレーションは
  - バスエクステンダーなし：4×10^4
  - バスエクステンダーあり：3.5×10^4

  程度のデータ数が得られる
- ピークの広がりはチップの違い
- バスエクステンダーありの 2mA, 8mA はデータ数にほとんど違いがない

  → LDVS 設定に関係なく良好なキャリブレーションができている