SlowControlなど

蜂谷　崇

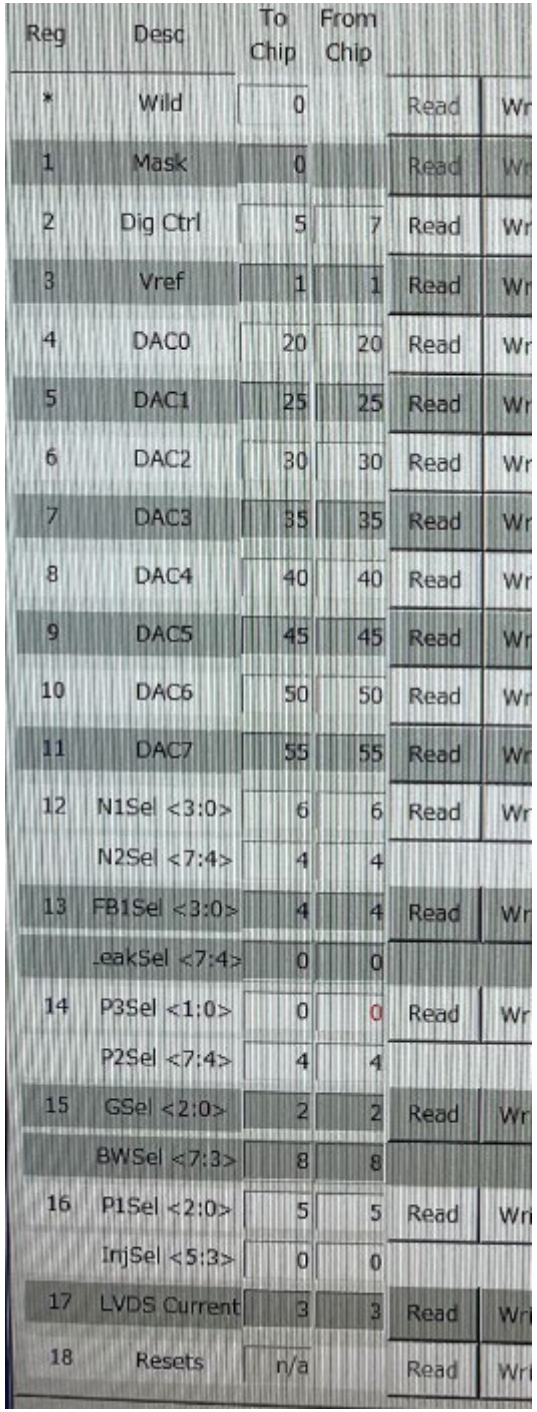
ReadBackerの問題

- Readbackerでデータがおかしい@理研
  - ビットずれや化けのような症状
  - BE使用時、同様な症状が見つかった@奈良女
    - FFR後のLVDS値：　0xF (初期値)　→　0x1F

- BE有り無しでの再現実験
  - BEなし：　読み出しできた
  - BEあり：　まだ再テストしていない

- 原因
  - もしBEのせいだとすると、ROCでReadback波形をLatchするタイミングが問題。

- 今後
  - ReadBack波形をInterception, FEMで確認する

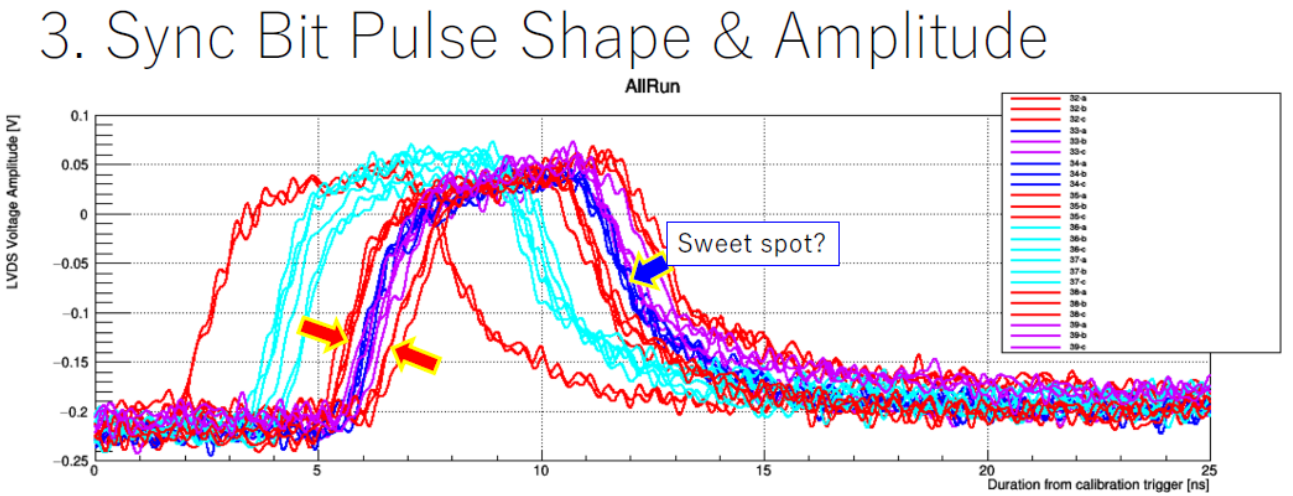


Reg	Desc	To Chip	From Chip		
*	Wild	0		Read	Wr
1	Mask	0		Read	Wr
2	Dig Ctrl	5	7	Read	Wr
3	Vref	1	1	Read	Wr
4	DAC0	20	20	Read	Wr
5	DAC1	25	25	Read	Wr
6	DAC2	30	30	Read	Wr
7	DAC3	35	35	Read	Wr
8	DAC4	40	40	Read	Wr
9	DAC5	45	45	Read	Wr
10	DAC6	50	50	Read	Wr
11	DAC7	55	55	Read	Wr
12	N1Sel <3:0>	6	6	Read	Wr
	N2Sel <7:4>	4	4		
13	FB1Sel <3:0>	4	4	Read	Wr
	eakSel <7:4>	0	0		
14	P3Sel <1:0>	0	0	Read	Wr
	P2Sel <7:4>	4	4		
15	GSel <2:0>	2	2	Read	Wr
	BWSel <7:3>	8	8		
16	P1Sel <2:0>	5	5	Read	Wr
	InjSel <5:3>	0	0		
17	LVDS Current	3	3	Read	Wr
18	Resets	n/a		Read	Wr

データ伝送の問題

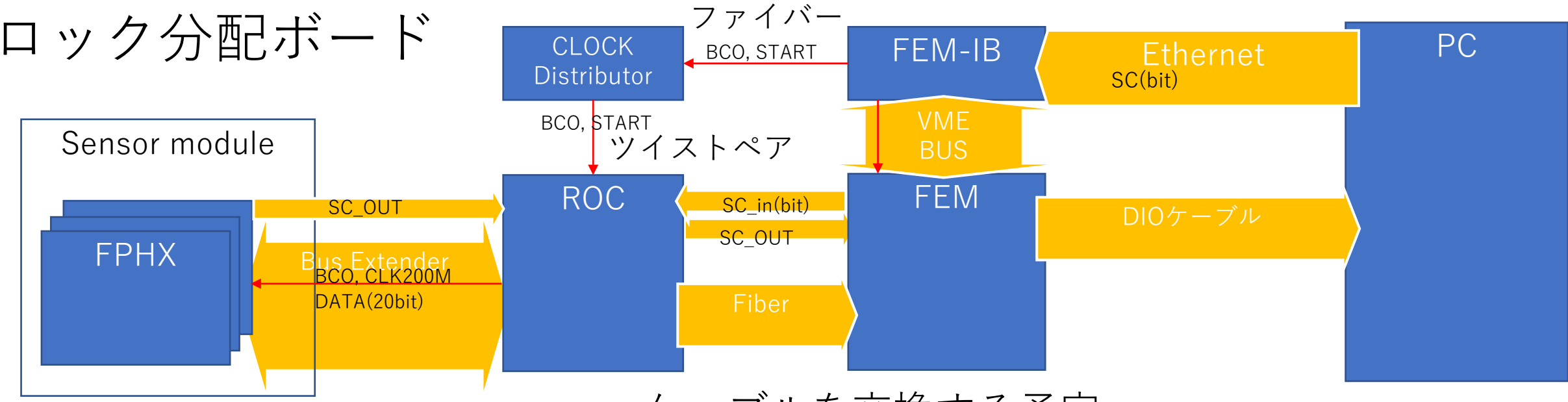
- データ数が半分になる問題
  - 比較調査のため理研にテストベンチをもう一台設置。　奈良女ベンチと比較
  - 理研ベンチでは、問題発生率が低い：　理研 = ~2%, 奈良女 = ~23%　なぜ？
  - 違いを比較　：　あまり違いはないが、電源の種類や電圧値を理研にそろえる。

	NWU	RIKEN
Power supply	1 switching, all other series	all series
Supply voltage	6.3V for optics	6.6V
ROC type	Test bench	1008 ver. (FPGA code might be different)
Ladder	Full from BNL	Full from BNL

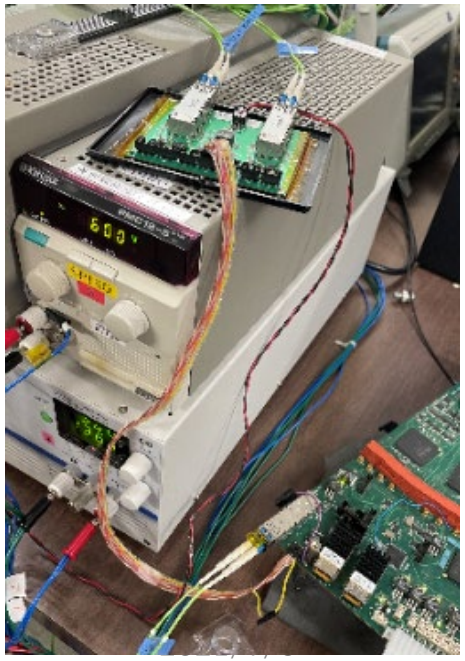


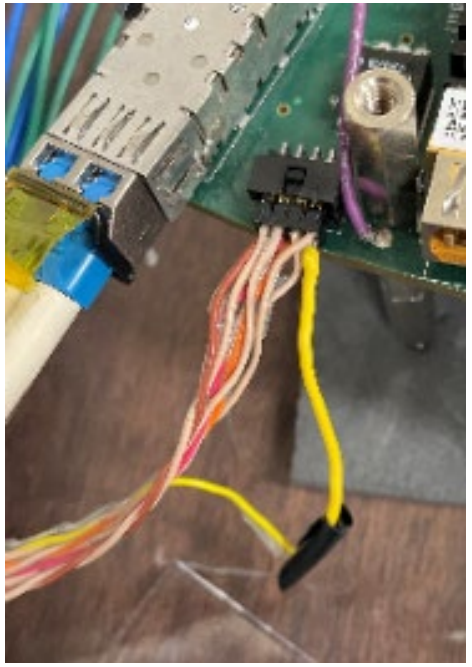
- さらなる情報：
  - CLK分配ボードの接触不良で問題発生率が変わる@理研
  - →　接触によってCLKのスキューが変わるとすると説明できる？！

クロック分配ボード

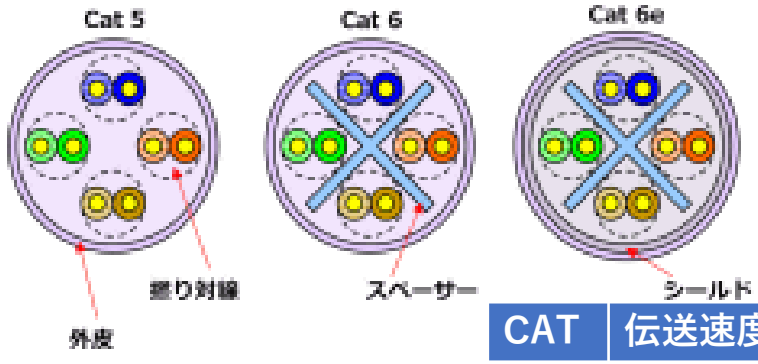


クロック分配ボード





- ケーブルを交換する予定
  - 配線が細い　AWG28　→　24
  - 8ピンコネクタ：　LANケーブルで置き換えてみる



本来はどのような
ケーブルの仕様か？

CAT	伝送速度	規格	
5	100MHz	100Base-TX	ツイストペア
6	250MHz	1000Base-TX	仕切りあり
6A	500MHz	10GBase-T	シールドあり

Reviewに向けて

- Electronics Readout Performance
  - **BE単体性能　：　減衰、反射の周波数特性、Eyeダイアグラム**
  - **テストパルスによるデータ収集効率**

  - ADC vs AmplitudeによるGainとOffsetの理解
    - Ch毎のばらつき

  - LVDS波高に対する収集率の変化
    - LVDS波高についてのEyeダイアグラム(森田さんのStudy)

  - HalfEntry問題

  - SlowControlについて
    - コマンドを送る方法と制御
      - Ladder, Chipごとにコマンドを送れる。
    - Readbackの方法と結果

USBからのSlowControlCommand

- 12ByteのUSBコマンド

11	10	9	8	7	6	5	4	3	2	1	0
Header	Size (2Byte)		Test Bench Command	Wedge Address	FEM Address	FPHX SC command (4Byte)				Check Sum	Trailer
0xFF			0x83	[7:4]= Side [3:0]= Wedge							0xFF

FPHX SlowControl Command 32bit (4byte)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Header							Chip					Register-ID					Instr			Data									Trailer			
0b_1101_111							10101 (wild *)										Write(1) Set(2), Reset(5), Default(6)											0b_0000			

読み出しデータは8ビット(に見える)

TestBench Command (1byte)

7	6	5	4	3	2	1	0
Destination			Command				
ROC/FPHX	FEM	FEM-IB					

some symbols for the available teststand ops	WORD	Dist	Com	# PLEASE DO NOT CHANGE THESE. ADD TO THEM, DO NOT CHANGE.
TESTBENCH_FPHX	0x83	100	0x03	# FPHX op (Send packet payload to FPHX)
TESTBENCH_RESET	0x8B	100	0x0B	# FFR (firefighter reset) for FPHX chip
TESTBENCH_CALIB	0x85	100	0x05	# Start calibration sequence
TESTBENCH_PULSEAMP	0x86	100	0x06	# Set the pulser amplitude
TESTBENCH_PULSE	0x87	100	0x07	# Generate a pulse
TESTBENCH_PULSER	0x88	100	0x08	# Configure the pulse train
TESTBENCH_LATCHFPGA	0x89	100	0x09	# Send the latch command to the FPGA(s)
TESTBENCH_PULSE_MODULE	0x8A	100	0x0A	# Send the module that should be pulsed (bits 0-2 - side, bits 4-7 = wedge location)
TESTBENCH_EEPROM_READ_WRITE	0x50	010	0x10	# Read or Write from the EEPROM on the FEM
TESTBENCH_EEPROM_BATCH_DOWNLOAD	0xD1	110	0x11	# Batch download of EEPROM from FEM to ROC (change from 7 to 11 8/2/11)
TESTBENCH_FOSYNC	0x41	010	0x01	# Send the FEM fiber opticy synch command (upper 4 bit means FEM command)
TESTBENCH_FEMLVL1DELAY	0x45	010	0x05	# Send the FEM fiber opticy synch command (upper 4 bit means FEM command)
TESTBENCH_BCOSTART	0x62	011	0x12	# Send BCO start command to the FEM_IB and the FEM
TESTBENCH_FPGARESET	0xE4	111	0x04	# Reset for FEM, FEMIB + ROC = 0xE4, both FEM and ROC = 0xC4. For just ROC = 0x84. For just FEM = 0x44
TESTBENCH_CHECKGLINK	0x56	010	0x16	# Check the status of the GLINK lock signal in the FEM IB
TESTBENCH_JTAGSYNC	0x54	010	0x14	# Send the JTAG fiber opticy synch command
TESTBENCH_CHECKFEMADDR	0x46	010	0x06	# Check the FEM with FEM_ADDR is present and responding
TESTBENCH_USENI	0x43	010	0x03	# Set data acquisition for National Instruments rather than DCM (default)
TESTBENCH_SELFTRIG	0x48	010	0x08	# Set the FEM to self-trigger on input data lines

Destination	Destination	Function	Destination Bits (top 3)	Command Bits (Bottom 5)	Comment	Data	Response
ROC	UNUSED	UNUSED	000	1			
	UNUSED	UNUSED	000	2			
	FPHX	FPHX Command	100	3	Send 32 bit command to FPHX	32 bit command	FPHX return word - should be value set to register
	FPGAs	RESET FPGA	100	4			COMMAND
	SC FPGA	Calibrate	100	5	Initiate calibration sequence	One byte containing pulse	COMMAND until Calib done, then "00000000"
	Pulser	Set Pulser Amplitude	100	6		Pulser amplitude	
	Pulser	Send Pulse	100	7			
	Pulser	Send N pulses with M Spacing	100	8		Number of pulses and spacing	
	Data FPGA	LATCH	100	9		One byte containing pulse	# Fibers latched (0-16)
	Calib Circuitry	Set module to pulse (ROCII)	100	0xa		0-7 selects side 0-7 of 4 wedges	
	FPHX	FPHX Reset	100	0xb			COMMAND
	SC FPGA	Set Calibration parameters	100	0xc		AMPL_STEP, N_AMPL_STEPS, N_PULSES, SPACING	COMMAND
	Data FPGA	FPHX data lines to mask off	100	0xd		AMPL_STEP, N_AMPL_STEPS, N_PULSES, SPACING	COMMAND
FEM	SC FPGA	SC FO sync command	010	1			"11111111" if synced, else "00000000"
	SC FPGA	Start BCO	010	2		One byte containing pulse	COMMAND
	SC and Data FPGAs	Set DAQ for NI	010	3			
	SC and Data FPGAs	RESET FPGA	010	4		One byte containing pulse	COMMAND
	SC FPGA	Set LVL-1 delay	010	5		One byte of lvl-1 delay value	LVL-1 delay value
	SC FPGA	Is FEM N Present?	010	6			Returns FEM Address if present
	SC FPGA	Is Calib Done?	010	7			"11111111" if calibrating, else "00000000"
	SC FPGA	USE_COSMIC_TRIGGER	010	8	USE_COSMIC_TRIGGER set to '1' and internal triggering used if this command is called		
	EEPROM	EEPROM Write	010	0x10	Writes FPHX data to EEPROM		
	SC FPGA	BATCH DOWNLOAD	010	0x11	Read all chip data and download		
	SC FPGA	READ PAGE	010	0x12	Read 1 chip's data, download		
	SCFPGA	Send JTAG Sync	010	0x14	Tell ROC to use JTAG FPGA for programming		
	SC FPGA	Is SC FO synched?	010	0x15			"11111111" if synced, else "00000000"
	SC FPGA	Check LATCH	010	0x16			# Fibers latched (0-16)
	SCFPGA	Set Data FPGA MODE=1	010	0x18	Collect data from 2 BCO clocks (mode=1)	none	
	SC and Data FPGAs	Set Data FPGA MODE=0	010	0x19	Collect data from 1 BCO clock (mode=0)	none	
FEM_IB	FEM_IB	Is GLINK locked?	001	1			"1" if locked, "0" if not
	Start Fiber	Start BCO	001	2	Issue a Start BCO on Start Fiber	One byte containing pulse	COMMAND
	FPGA	RESET FPGA	001	4			COMMAND
		JTAG Programming On	001	?			
		JTAG Programming Off	001	?			
ROC + FEM	FPGAs	Reset	110	4		One byte containing pulse	COMMAND
	EEPROM	EEPROM Batch Read	110	0x11	Read all chip data and download		COMMAND
	EEPROM	EEPROM Page Read	110	0x12	Read 1 chip's data, download	Page Address (3 bytes)	COMMAND
FEM + FEMIB	FPGAS	Start BCO	011	2			

Command Packet = FF LL LL CC WW EE DD DD …. CS FF
LL LL = command length (count starts with command and ends with last data byte)
CC = command (see above)
EE = FEM address (0xf = wild card)
WW = Wedge address (0xFF = wild card)

DD = data
CS = check sum (xor of all the DD)