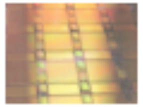
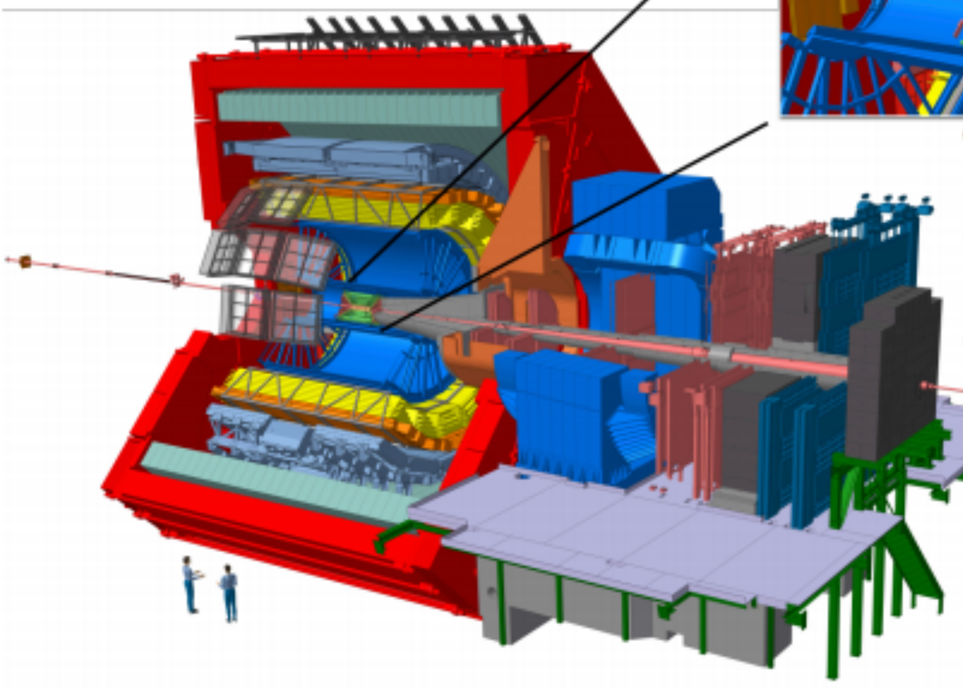
ALPIDE for MVTX and the next steps

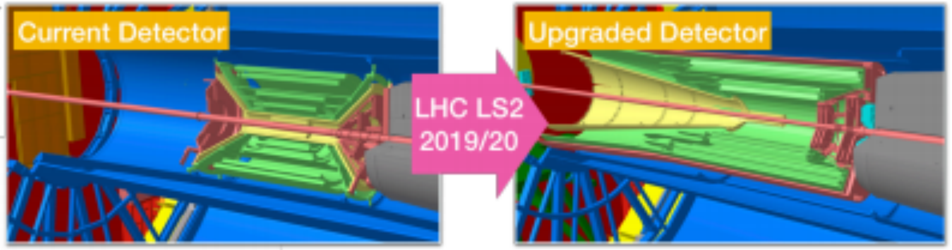
Y. Kwon
(Yonsei Univ.)

ALPIDE(ALice PIxel DEtector)

ALICE Inner Tracking System







6 layers:
- 2 hybrid silicon pixel
- 2 silicon drift
- 2 silicon strip

Inner-most layer:
- radial distance: 39 mm
- material: $X/X_0 = 1.14\%$
- pitch: $50 \times 425\ \mu m^2$

rate capability: 1 kHz

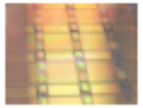
7 layers:
- all Monolithic Active Pixel Sensors

Inner-most layer:
- radial distance: 23 mm
- material: $X/X_0 = 0.3\%$
- pitch: $O(30 \times 30\ \mu m^2)$

rate capability: 100 kHz (Pb-Pb)

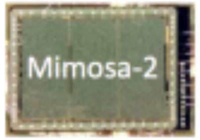
LoI: 2012
ITS CDR: 2012
ITS TDR: 2013

MAPS Evolution



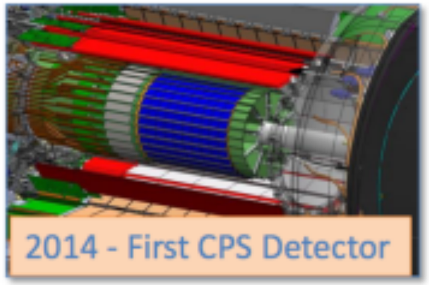
L. Musa, 30 years HI Forum
November 2016

Owing to the industrial development of CMOS imaging sensors and the intensive R&D work (IPHC, RAL, CERN)

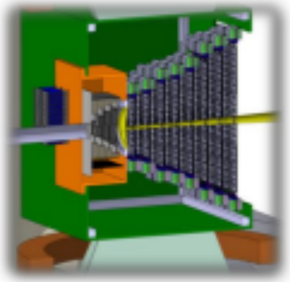


...

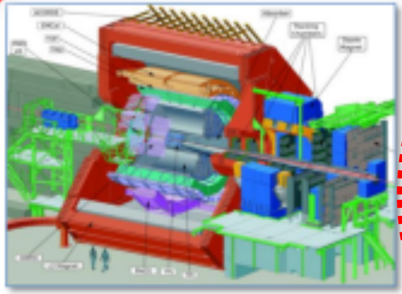
... several HI experiments have selected CMOS pixel sensors for their inner trackers



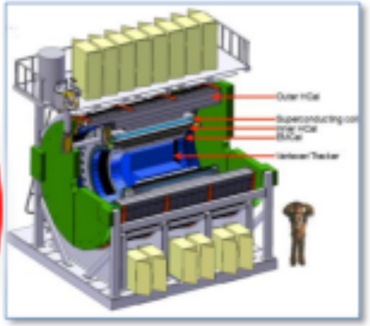
STAR HFT
0.16 m^2 – 356 M pixels



CBM MVD
0.08 m^2 – 146 M pixel



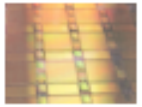
ALICE ITS Upgrade (and MFT)
10 m^2 – 12 G pixel



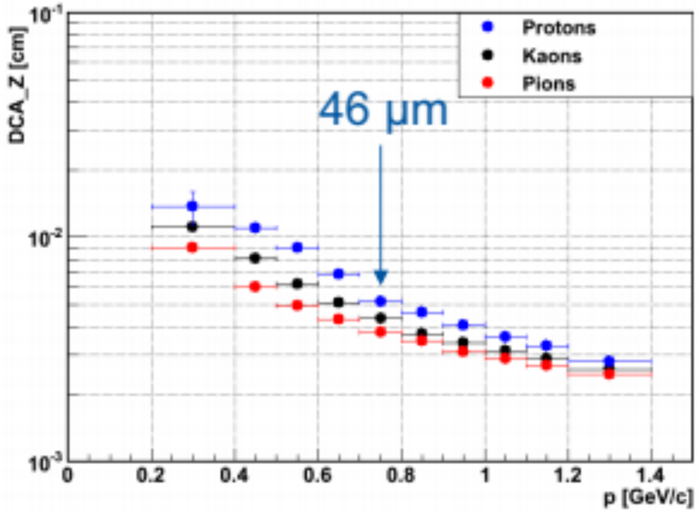
sPHENIX
0.2 m^2 – 251 M pixel

30

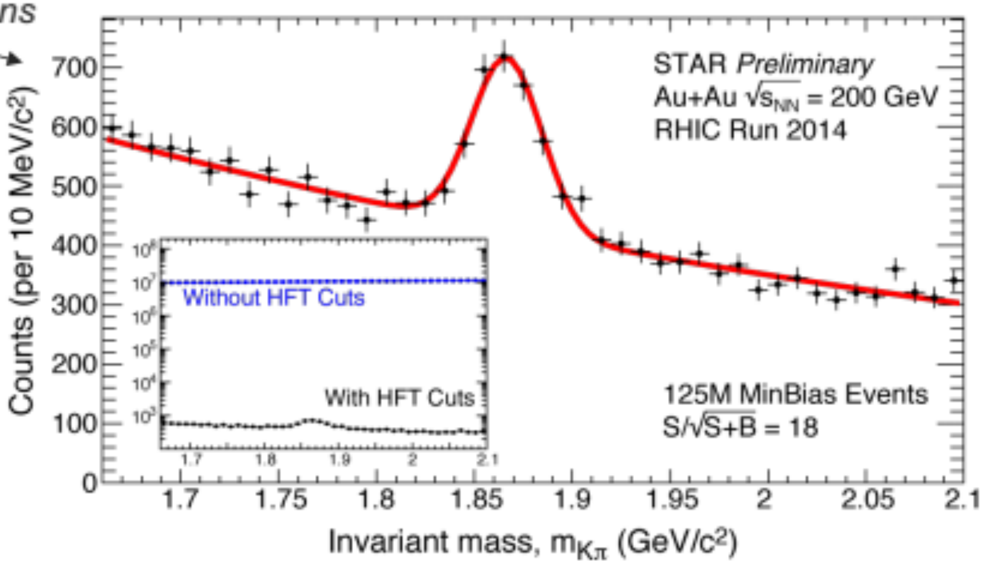
STAR HFT



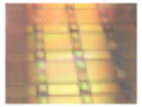
- DCA pointing resolution
  - Design requirement exceeded: 46 µm for 750 MeV/c Kaons for the **2 sectors** equipped **with aluminum cables on inner layer**
  - ~ 30 µm for p > 1 GeV/c
  - From 2015: all sectors equipped with aluminum cables on the inner layer



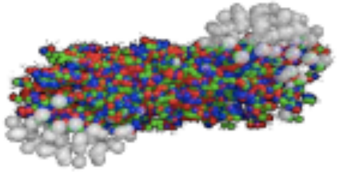
***$D^0 \rightarrow K\,\pi$ production** in $\sqrt{s_{NN}}$ = 200GeV Au+Au collisions (partial event sample)*



- Physics of D-meson productions
  - High significance signal
  - Nuclear modification factor R_{AA}
  - Collective flow v_2
- First Λ_c^+ signal observed in HI collisions (QM 2017)!



ALICE Upgrade



Motivation: QGP precision study

- High precision measurement of heavy flavour hadrons over a large range in p_T and rapidity and multi-differentially in centrality and reaction plane.

Requirements:

- Excellent tracking efficiency and resolution at low p_T
- Large statistics with minimum bias trigger to gain a factor 100 over present program
  - Pb-Pb recorded luminosity $\geq 10\ nb^{-1}$ plus p-p and p-A data
- Preserve PID capability at high rate

Strategy:

- **Readout all Pb-Pb interactions** at max. rate (50 kHz) with minimum bias trigger
  - Upgrade of the detector readout and online and offline systems
- Large improvement of **vertexing and tracking capability**
  - **New Inner Tracking System (ITS)** and Muon Forward Tracker (MFT)

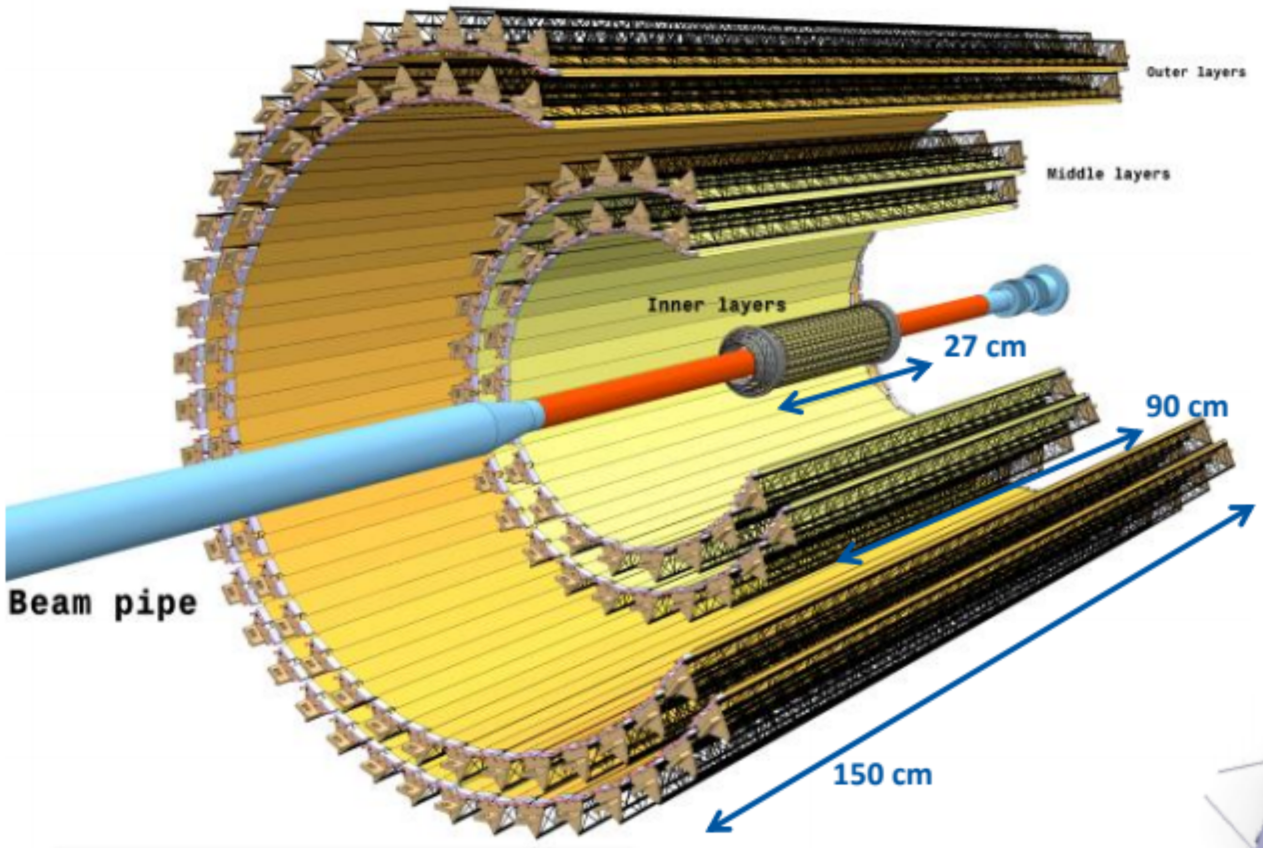
ITS Chip General Requirements

Parameter	Inner Barrel	Outer Barrel
Chip size (mm x mm)	15 x 30	
Chip thickness (μm)	50	100
Spatial resolution (μm)	5	10 (5)
Detection efficiency	> 99%	
Fake hit rate	$< 10^{-5}$ evt^{-1} $pixel^{-1}$ (ALPIDE $<< 10^{-5}$)	
Integration time (μs)	< 30 (< 10)	
Power density (mW/cm^2)	< 300 (~35)	< 100 (~20)
TID radiation hardness (krad) (**)	2700	100
NIEL radiation hardness (1 MeV n_{eq}/cm^2) (**)	1.7×10^{13}	1.7×10^{12}
Readout rate, Pb-Pb interactions (kHz)	100	
Hit Density, Pb-Pb interactions (cm^{-2})	18.6	2.8

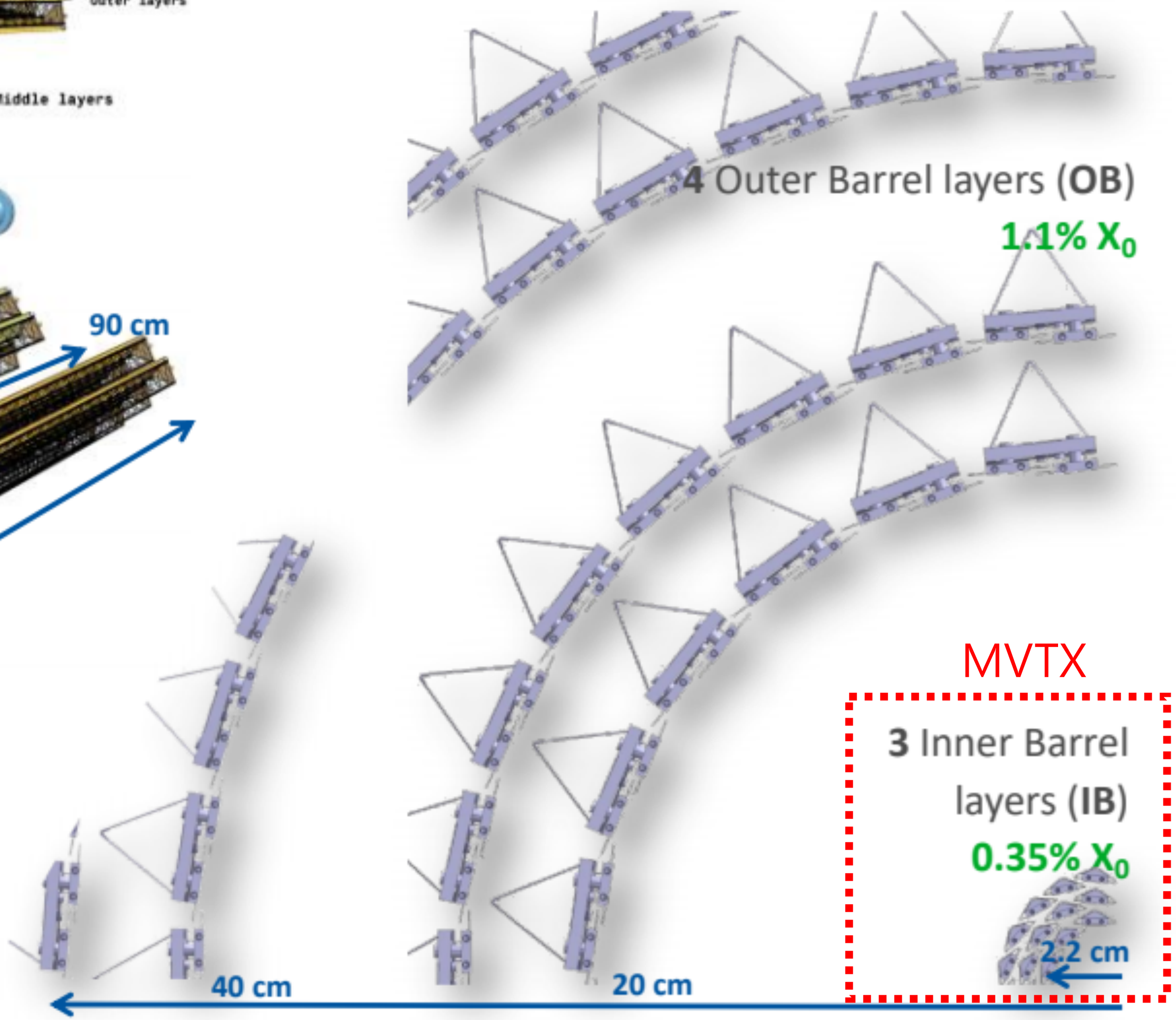
(*) In color: ALPIDE performance figure where above requirements

(**) 10x radiation load integrated over approved program (~ 6 years of operation)

ALICE ITS Upgrade Layout

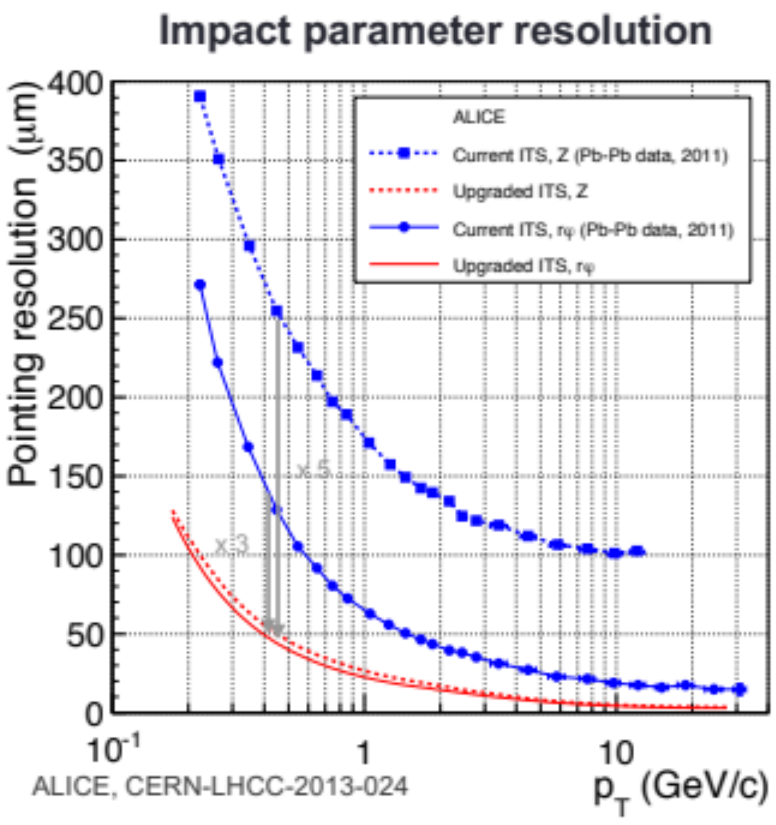


10 m² sensitive area
24120 CMOS Pixel Sensors
~**12.5** Gpixels

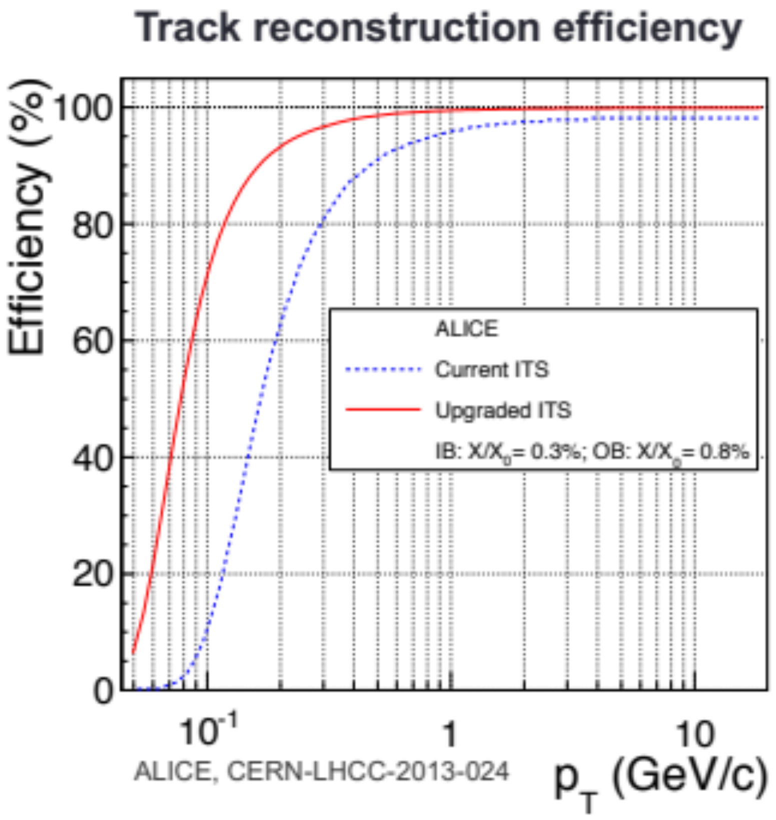


# STAVES:	48	42	30	24	20	16	12
# CHIPS:	9408	8232	3360	2688	432		

ALICE ITS Upgrade Performance Studies



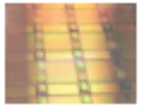
Improved impact parameter resolution

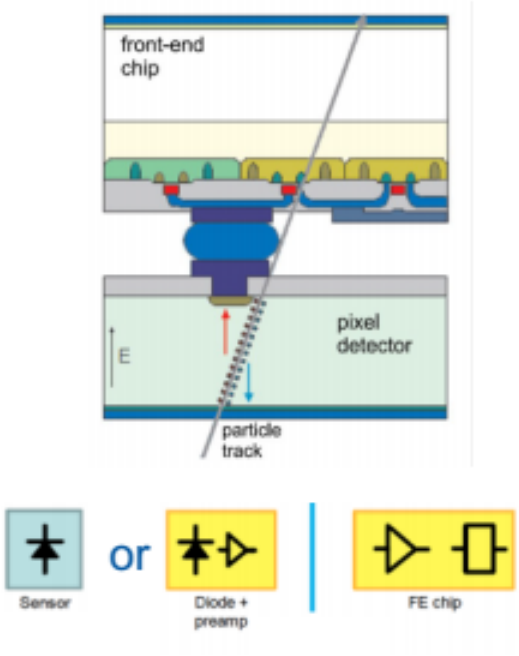


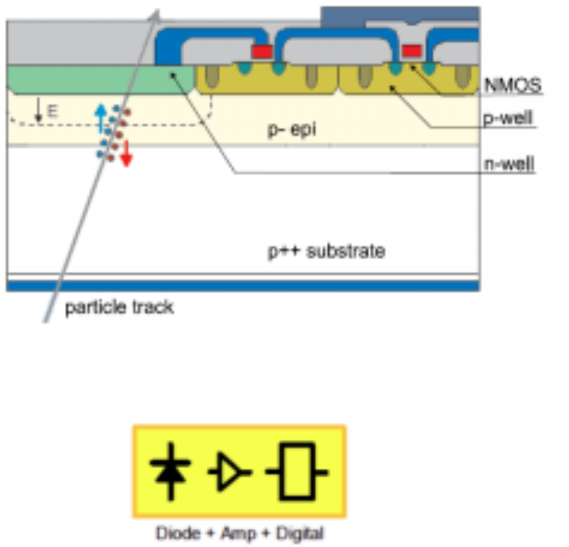
High standalone tracking efficiency

ALPIDE, Technology

Hybrid and Monolithic Pixels





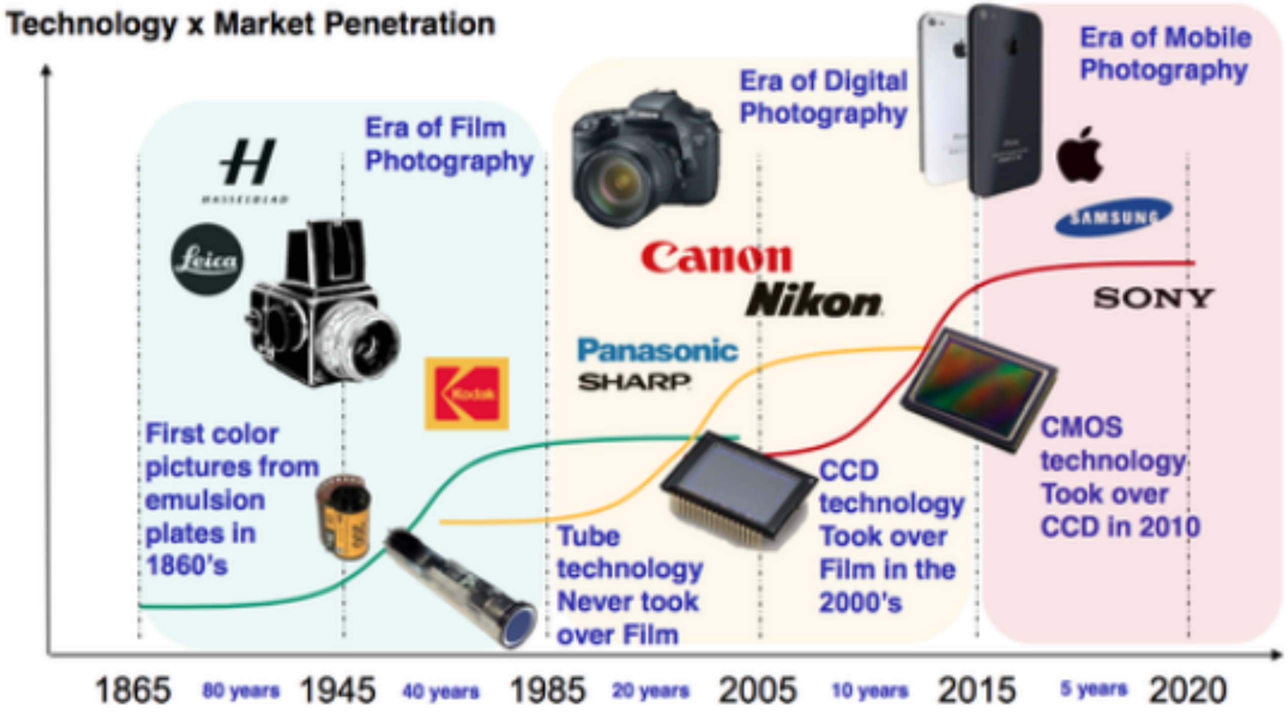


- Separately optimize sensor and FE-chip
- Fine pitch bump bonding to connect sensor and readout chip

- Charge generation volume integrated into the ASIC, but many different variants!
- Thin monolithic CMOS sensor, on-chip digital readout architecture

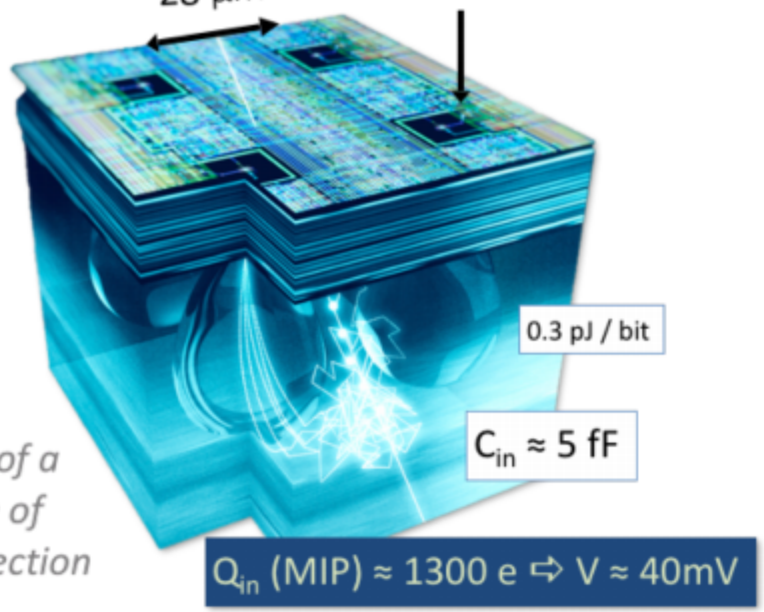
CMOS Image Pixel Sensors

- While 1980s were dominated by CCDs (camcorder market)
- The 1990s/2000s have shown an increasing demand for CMOS imaging sensors due to the camera phone market

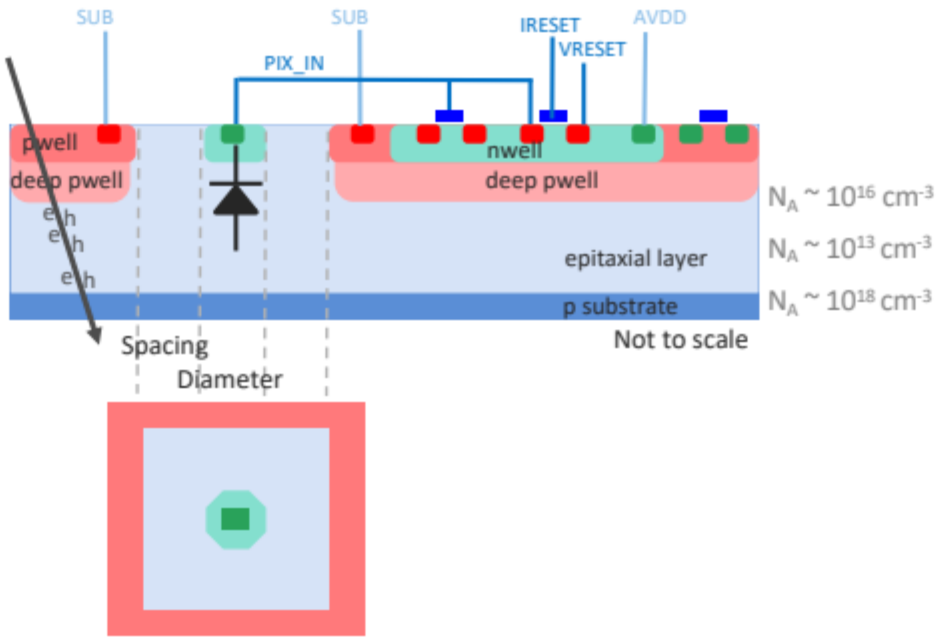


http://www.eetimes.com/document.asp?doc_id=1325655&image_number=1

ALPIDE Technology



Pixel Sensor CMOS 180 nm Imaging Process (TowerJazz)



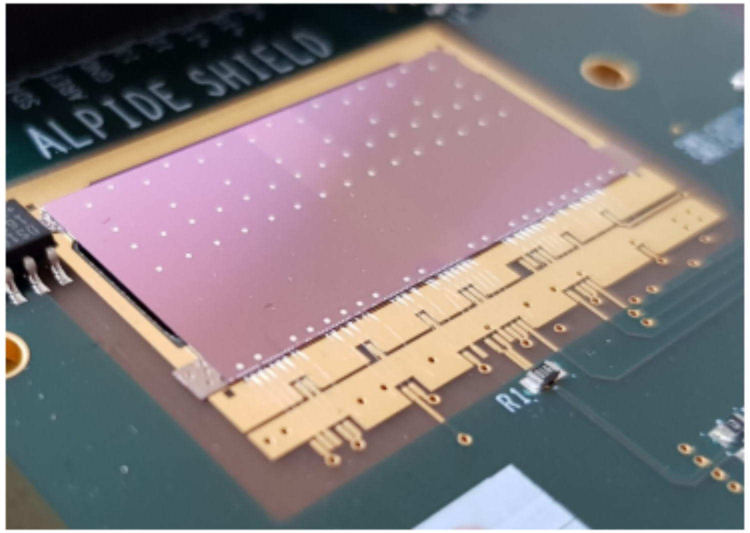
High-resistivity (> 1kΩ cm) p-type epitaxial layer (~25 µm) on p-type substrate

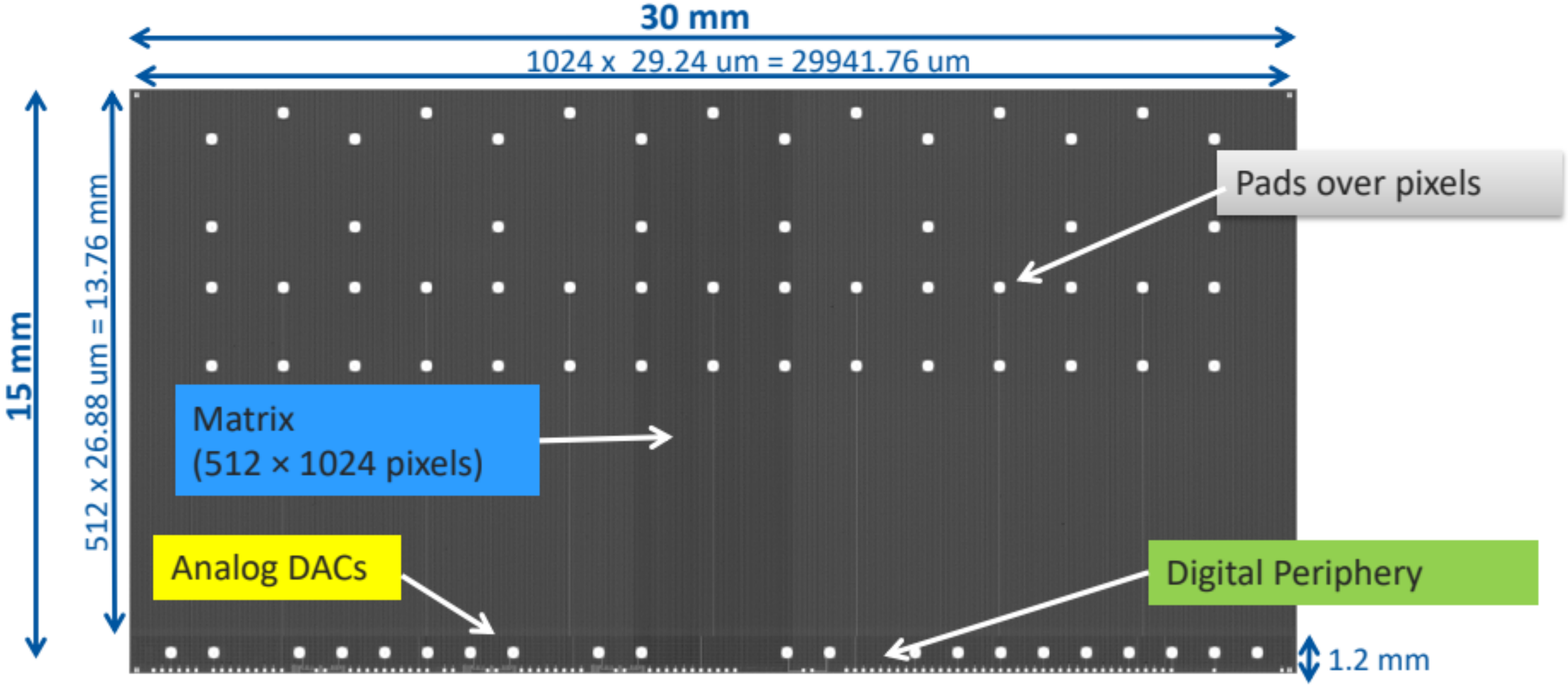
Deep PWELL shielding NWELL allowing PMOS transistors (full CMOS within active area)

Small n-well diode (2 µm diameter), ~100 times smaller than pixel => low capacitance => large S/N

Reverse bias can be applied to the substrate to increase the depletion volume around the NWELL collection diode

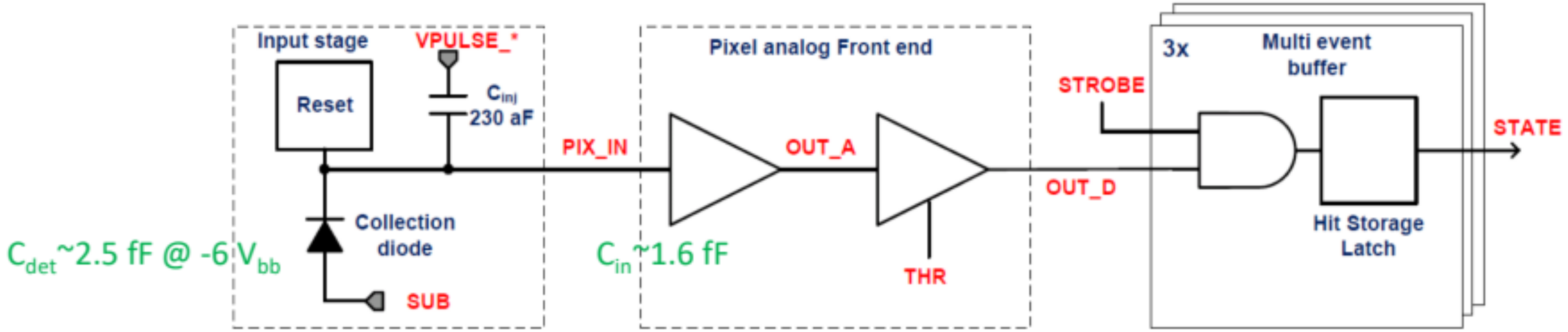
ALPIDE Chip

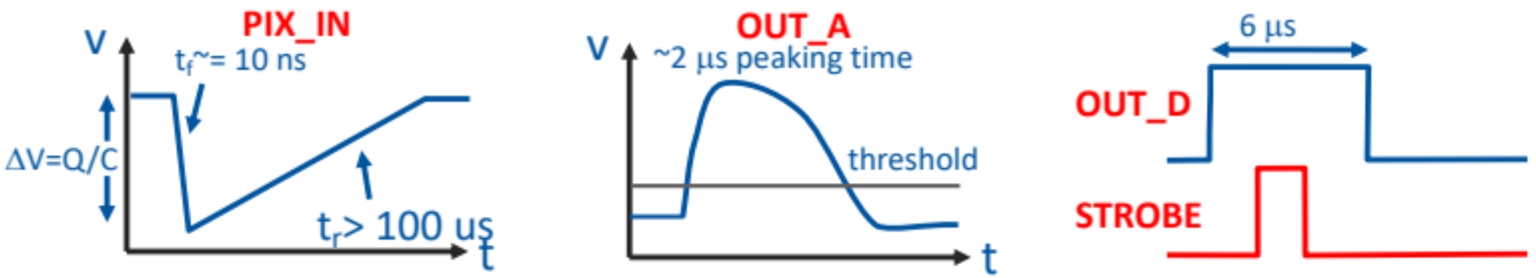




CNU,
ERN,
NFN (Torino, Cagliari),
PHC,
RFU,
IKHEF,
ONSEI

Pixel





Analog front-end and discriminator continuously active

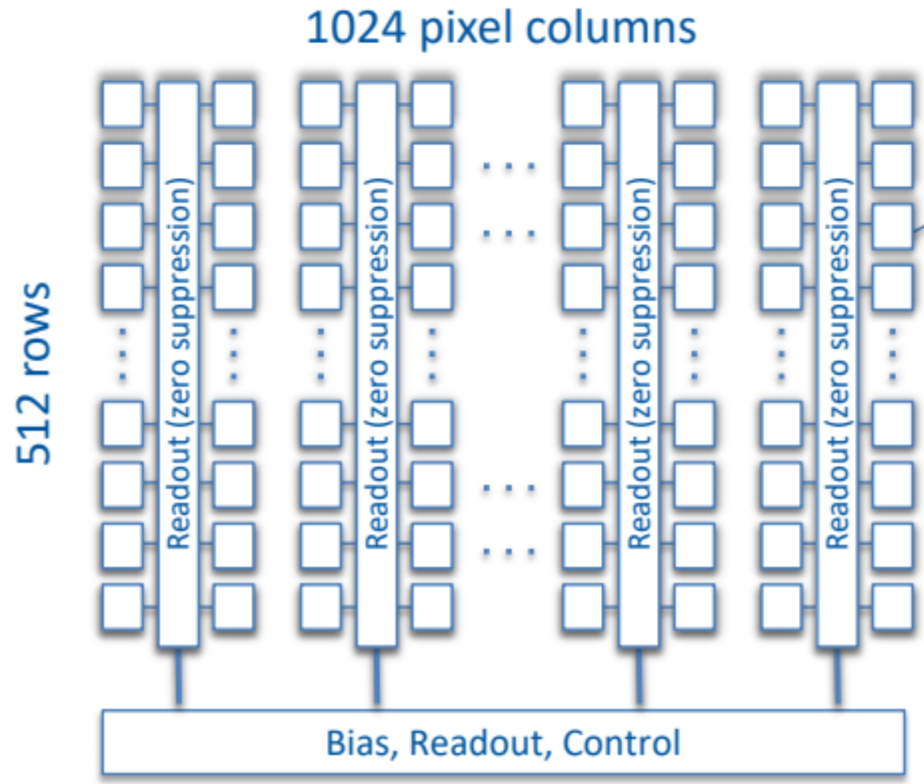
- Non-linear and operating in weak inversion. Ultra-low power: 40 nW/pixel
- The front-end acts as analogue delay line
- Test pulse charge injection circuitry
- Global threshold for discrimination -> binary pulse OUT_D

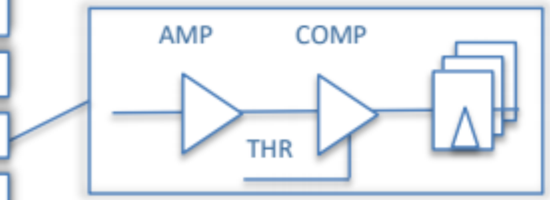
Digital pixel circuitry with three hit storage registers (multi event buffer)

- Global shutter (STROBE) latches the discriminated hits in next available register
- In-Pixel *masking* logic

Front End Characteristics (simulated)	
Gain (small signal) [mV/e]	4
ENC [e]	3.9
Threshold [e]	92 ± 2

ALPIDE Architecture





In pixel:

Amplification
Discrimination
3 hit storage registers (MEB)
Test charge injection
Masking

29 µm x 27 µm pixel pitch

Continuously active front-end

Global shutter (*STROBE signal*)

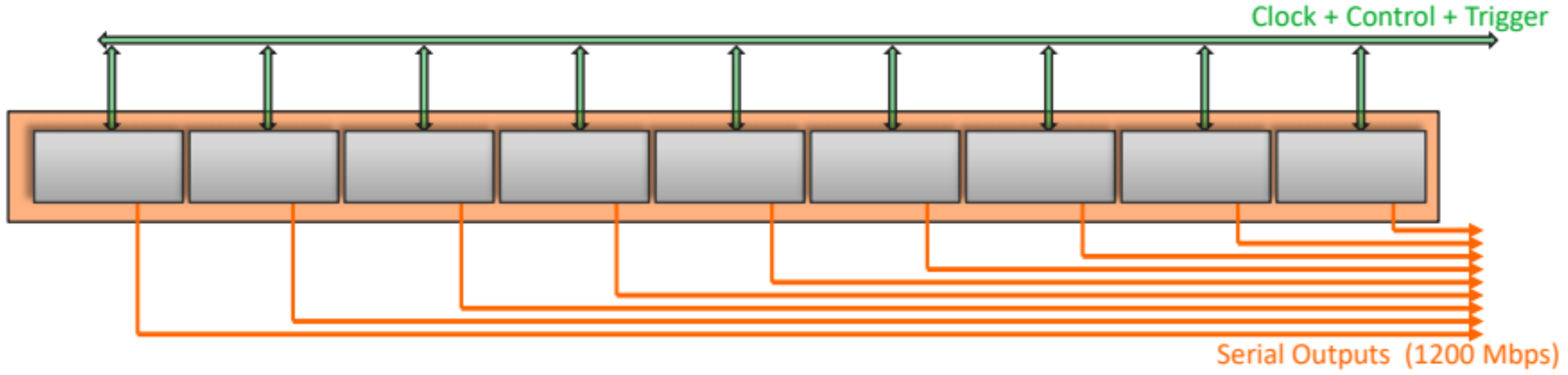
Zero-suppressed matrix readout

Triggered or continuous readout modes

ALPIDE, Performance

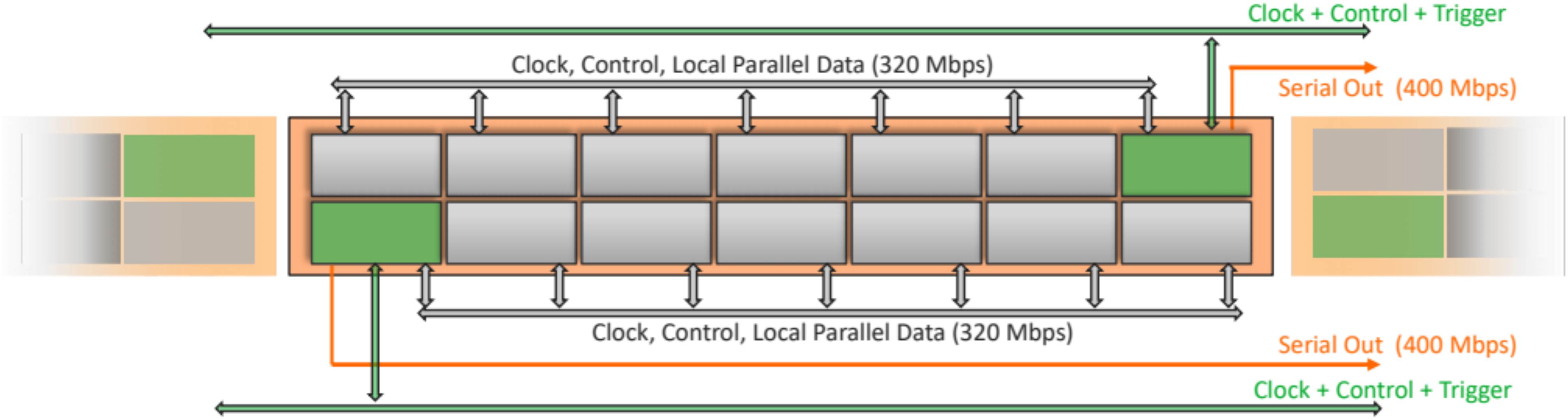
Detector Modules with ALPIDE Chips

ITS Inner Barrel Module – 9 chips, *shared* clock (40 MHz) and control (40 Mbps), individual data readout lines

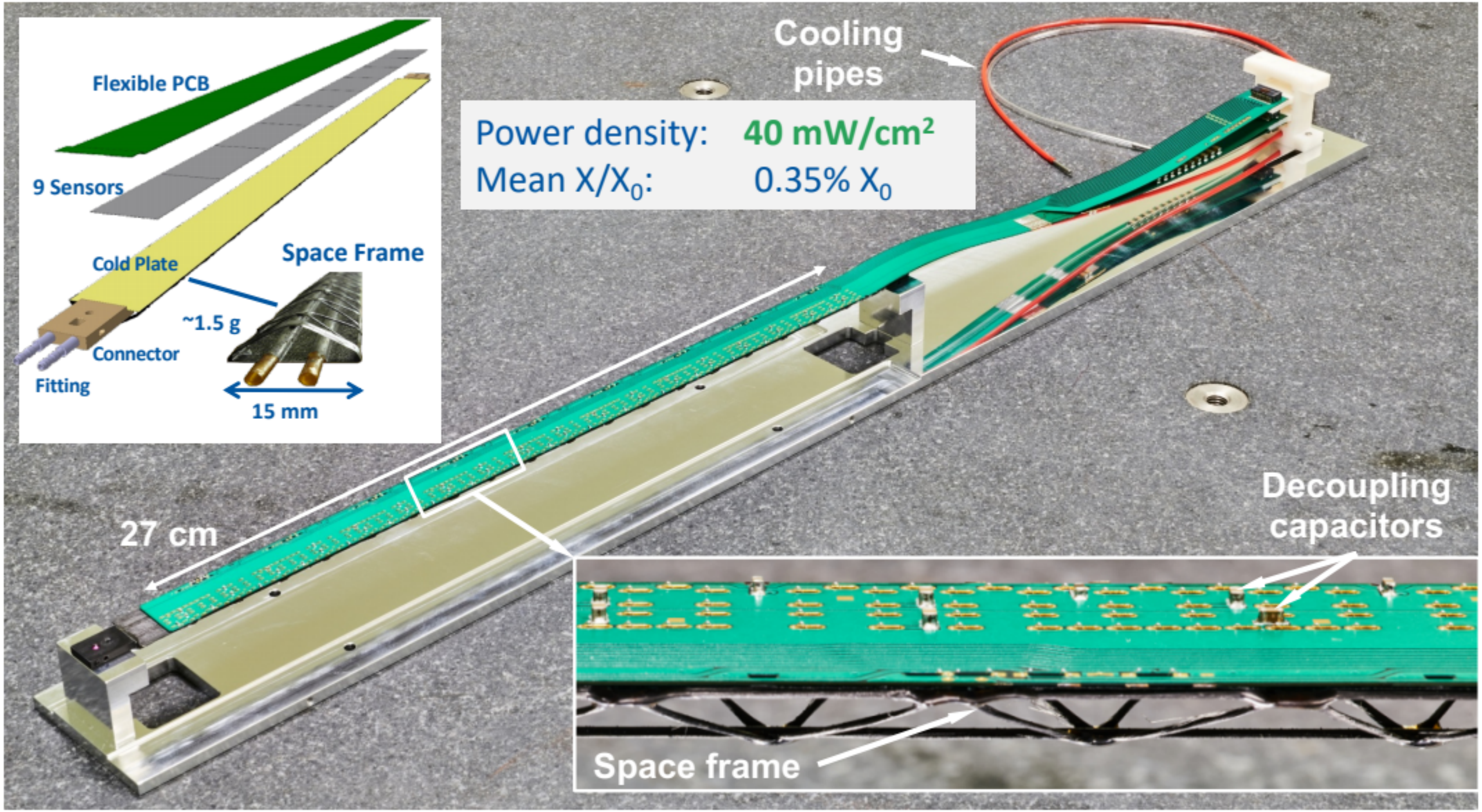


ITS Outer Barrel Module – 2 groups of chips, Master + 6 Slaves

Only the Master interfaces to the external world and bridges control and data transfer



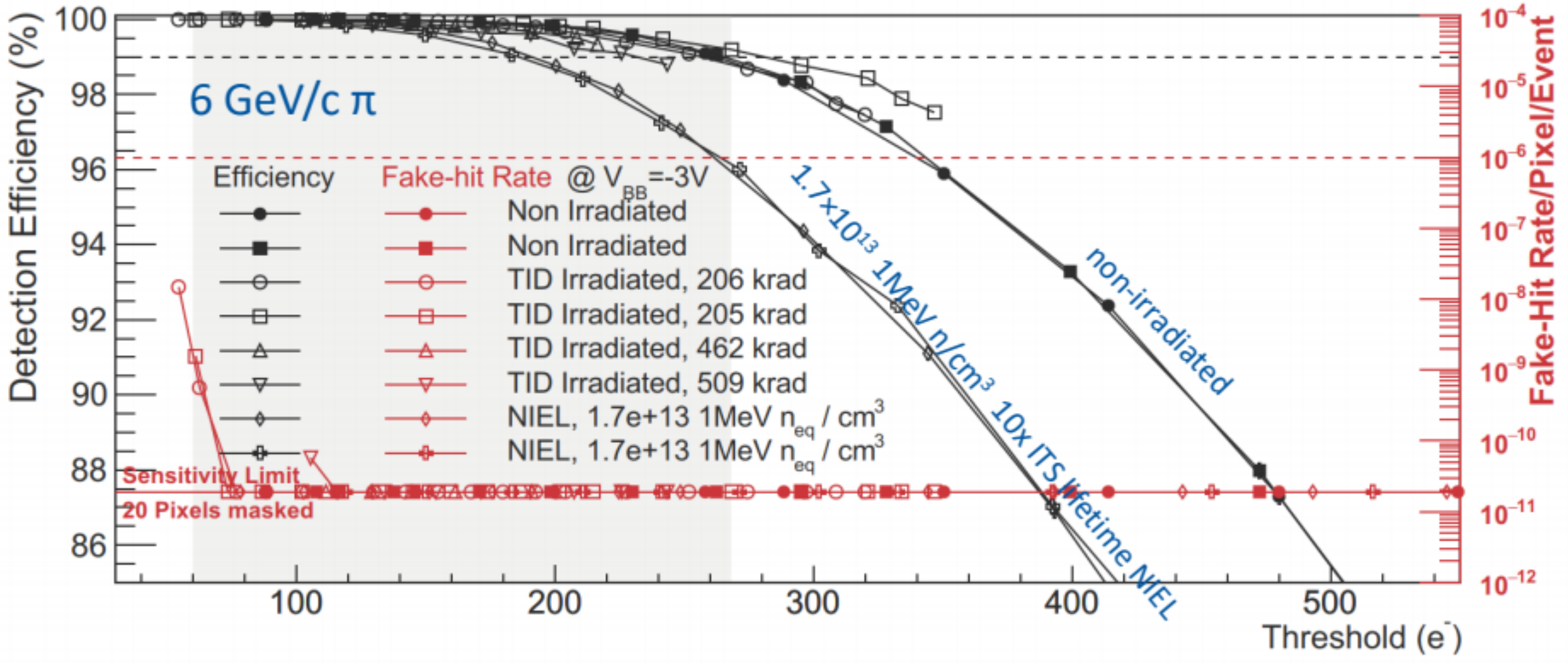
Inner Barrel Stave



Power density: 40 mW/cm²
Mean X/X_0: 0.35% X_0

Detection Efficiency and Fake Hit Rate

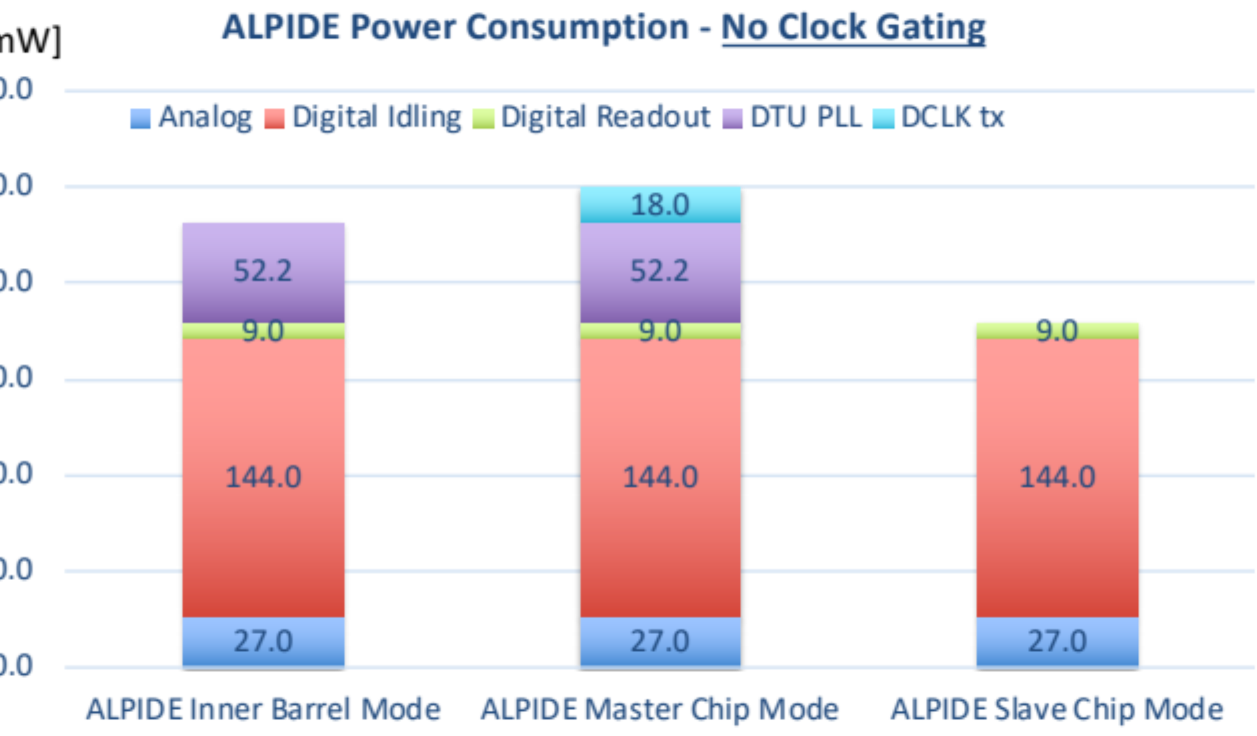
Test Beam Measurements

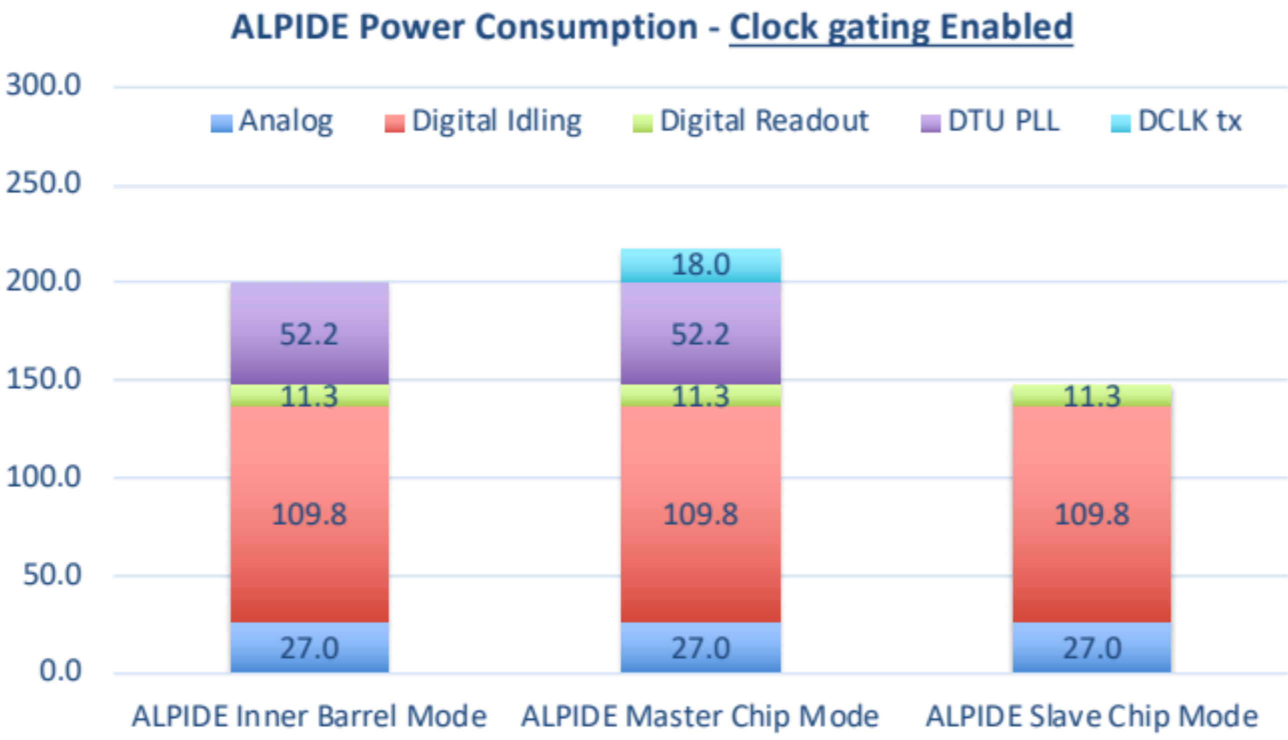


Large operational margin with O(10) masked pixels (0.002%)

Fake hit rate < $2*10^{-11}$ pixel hits/event

Typical Power Consumption Figures





Clock Gating OFF

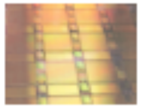
Inner Barrel Mode: 51 mW/cm^2
Outer Barrel Average: 42 mW/cm2

Clock Gating ON

Inner Barrel Mode: 44 mW/cm^2
Outer Barrel Average: 35 mW/cm2

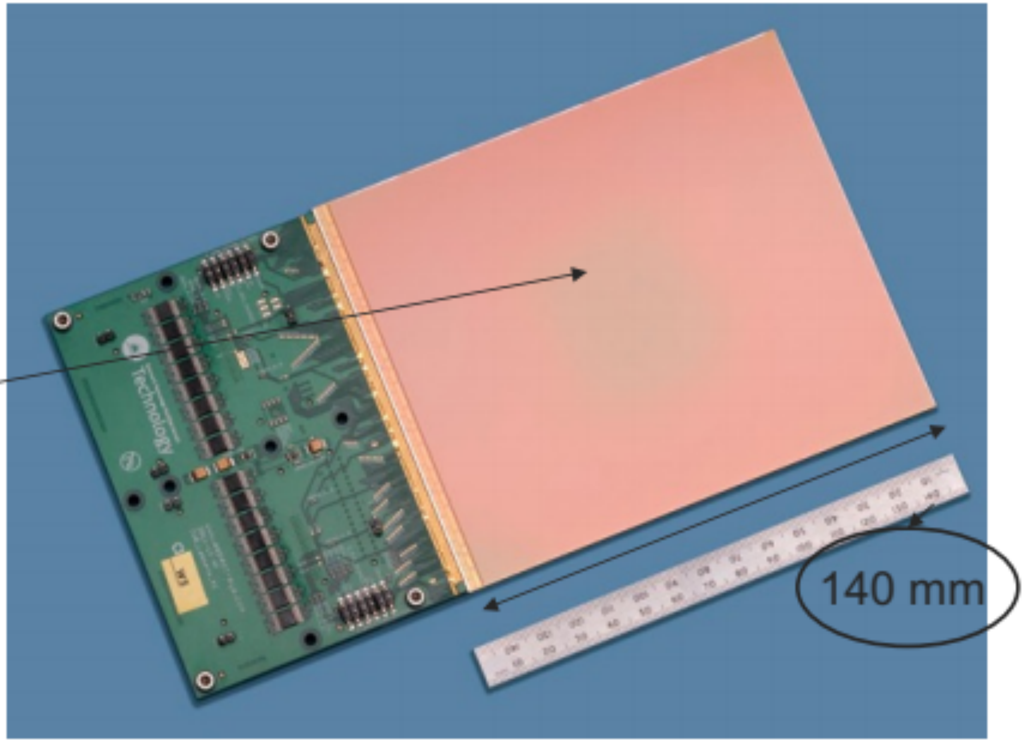
ITS3 & The next steps

MAPS (Monolithic Active Pixel Sensors) for Imaging and More



Many developments in the field of CMOS imaging sensors and MAPS in general within the community!

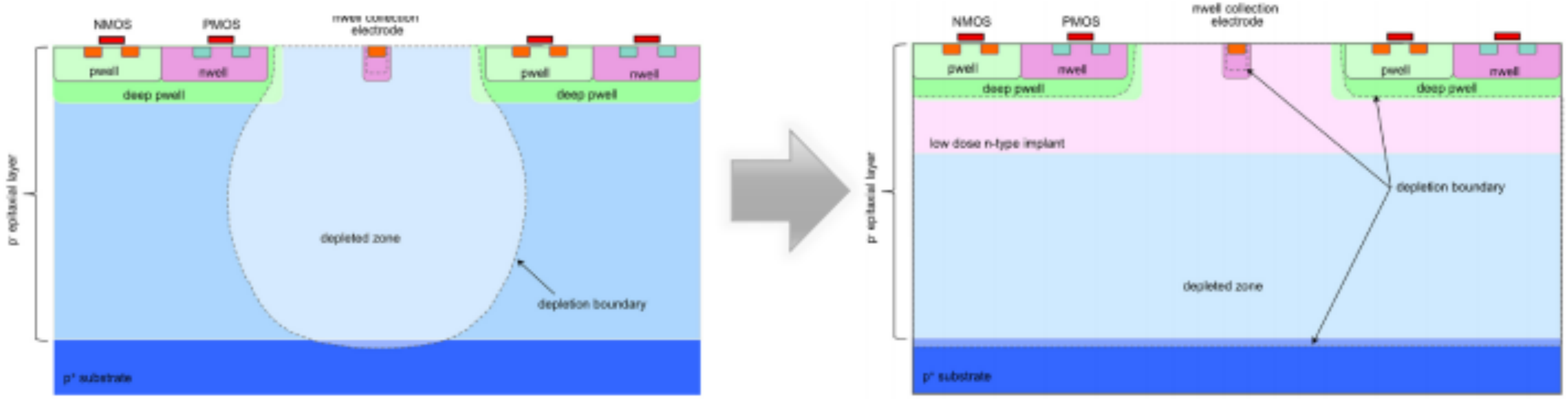
Example:
Wafers scale (8”) imaging sensor developed by the RAL team (stitched)



N. Guerrini, RAL, 5th school on detectors, Legnaro, April 2013

TJ 180 nm modified process

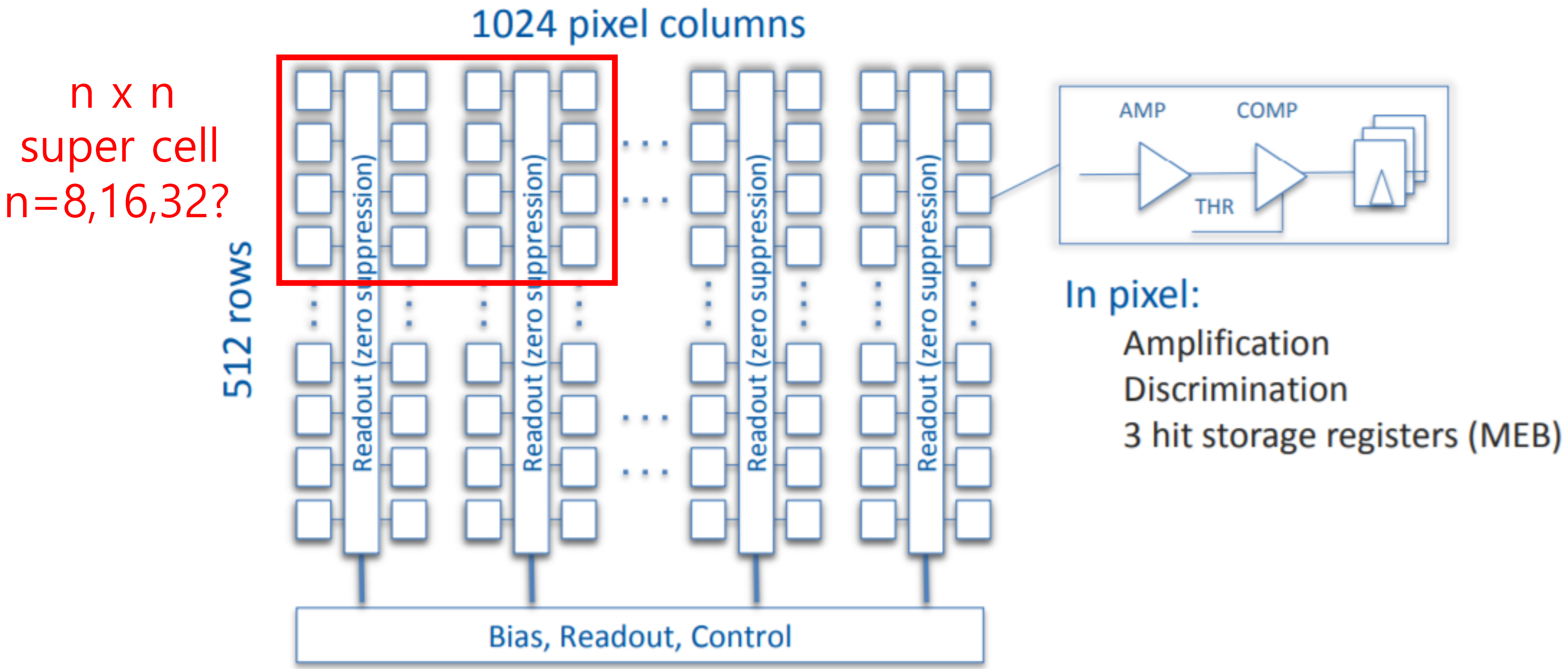
- Novel modified process developed in collaboration of CERN with TJ foundry in context of ALICE ITS.
- Combined with a small collection diode.



- Adding **a planar n-type layer** significantly improves depletion under deep PWELL
- Increased depletion volume → **fast charge collection by drift**
- better time resolution reduced probability of charge trapping (**radiation hardness**)
- Possibility to fully deplete sensing volume with no significant circuit or layout changes

W. Snoeys et al., NIM A871 (2017) 90 – 96.

ALPIDE-REBIN



What we deal with is the digital storage, and all modification is in periphery.

Towards timing device: 50 (μ)-thick Si sensor under usual condition

Assuming Si sensor thickness 50μ and $\vec{E} = \frac{20\ V}{50\ \mu}$, carrier drift time will be

$$v_e \sim 5.6 \cdot 10^6 \left(\frac{cm}{s}\right)$$

$$\Delta t_{50\ \mu} \sim 0.9 \cdot 10^{-9}\ (s)$$

Generic time resolution for sensor will be good!

Contents lists available at ScienceDirect

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journal homepage: www.elsevier.com/locate/nima

ELSEVIER

A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance

W. Snoeys [a,*], G. Aglieri Rinella [a], H. Hillemanns [a], T. Kugathasan [a], M. Mager [a], L. Musa [a], P. Riedler [a], F. Reidt [a], J. Van Hoorne [a], A. Fenigstein [b], T. Leitner [b]

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