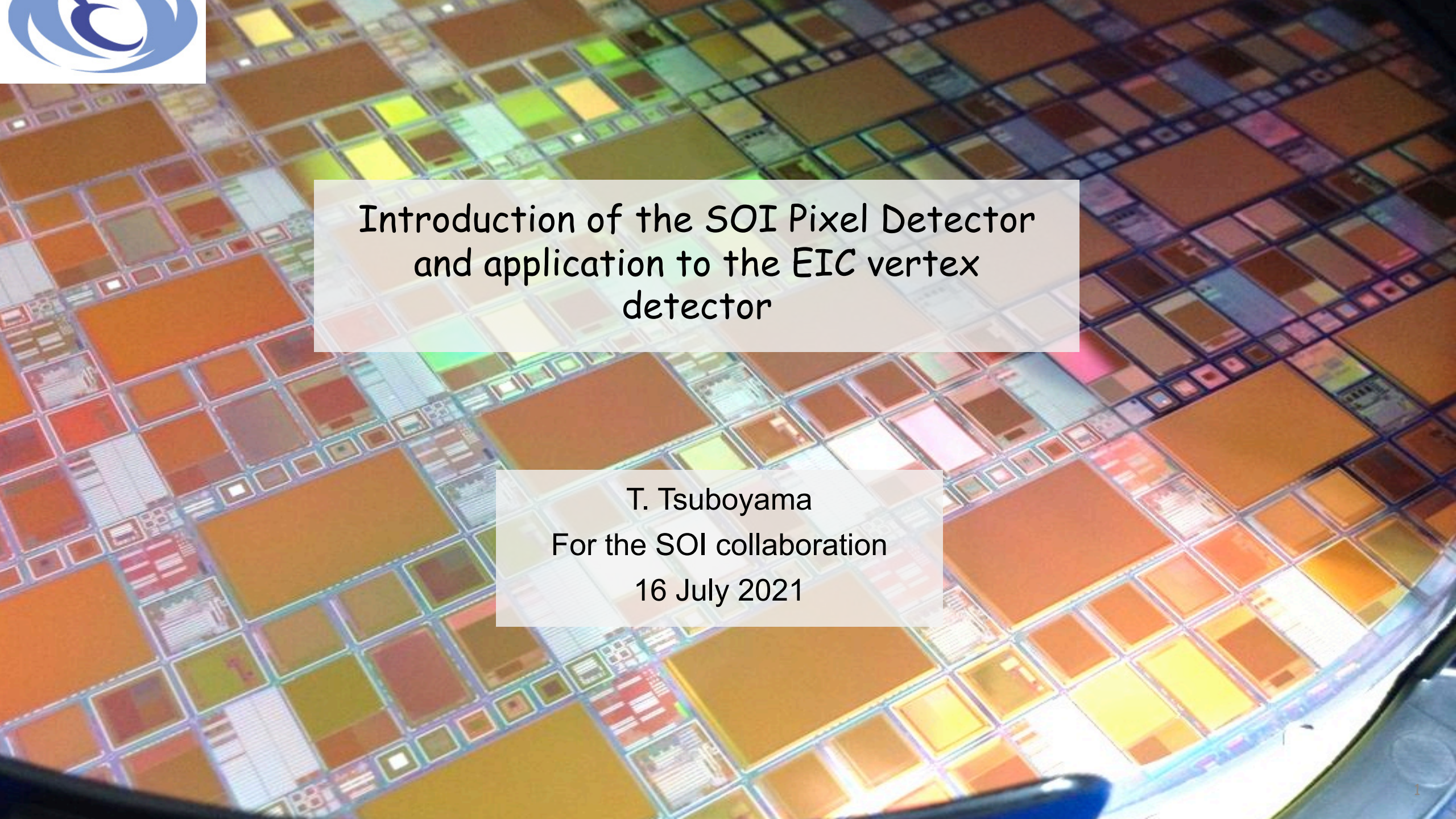


Introduction of the SOI Pixel Detector and application to the EIC vertex detector

T. Tsuboyama

For the SOI collaboration

16 July 2021

WHAT is Silicon-On-Insulator Pixel (SOIPIX)?

SOI is an advanced CMOS LSI technology:

CMOS circuit is produced on silicon wafer separated by an oxide layer

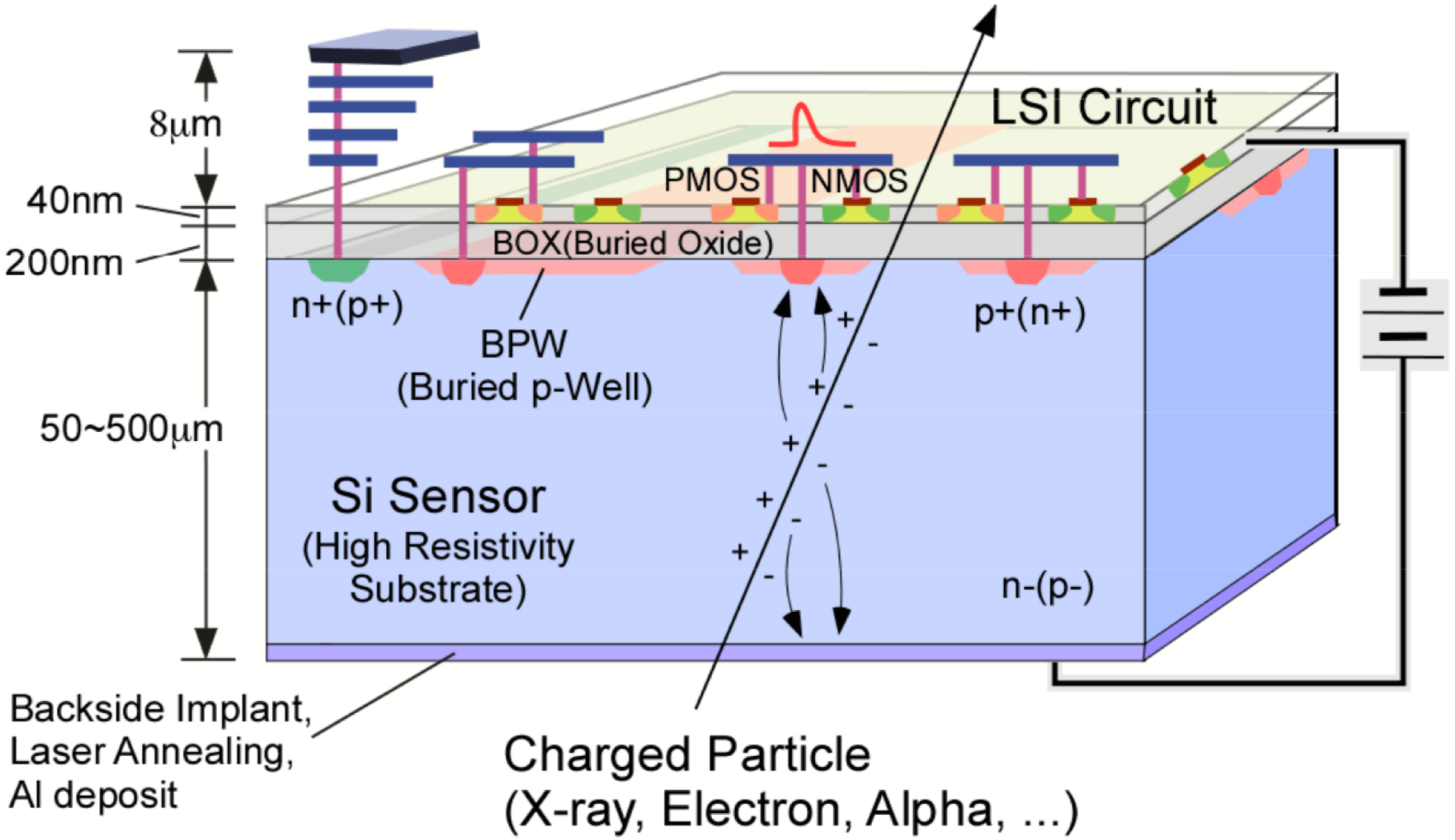
Transistors are isolated from each other and from the Si bulk

→ High performance CMOS circuit can be obtained

CMOS radiation sensor

The charge induced in the Si wafer is processed by the CMOS circuit above

Various wafer (sensor) and implantation features can be chosen depending on the radiation (MIP/X ray/Gamma/Neutron…)



Close up of the SOI structure

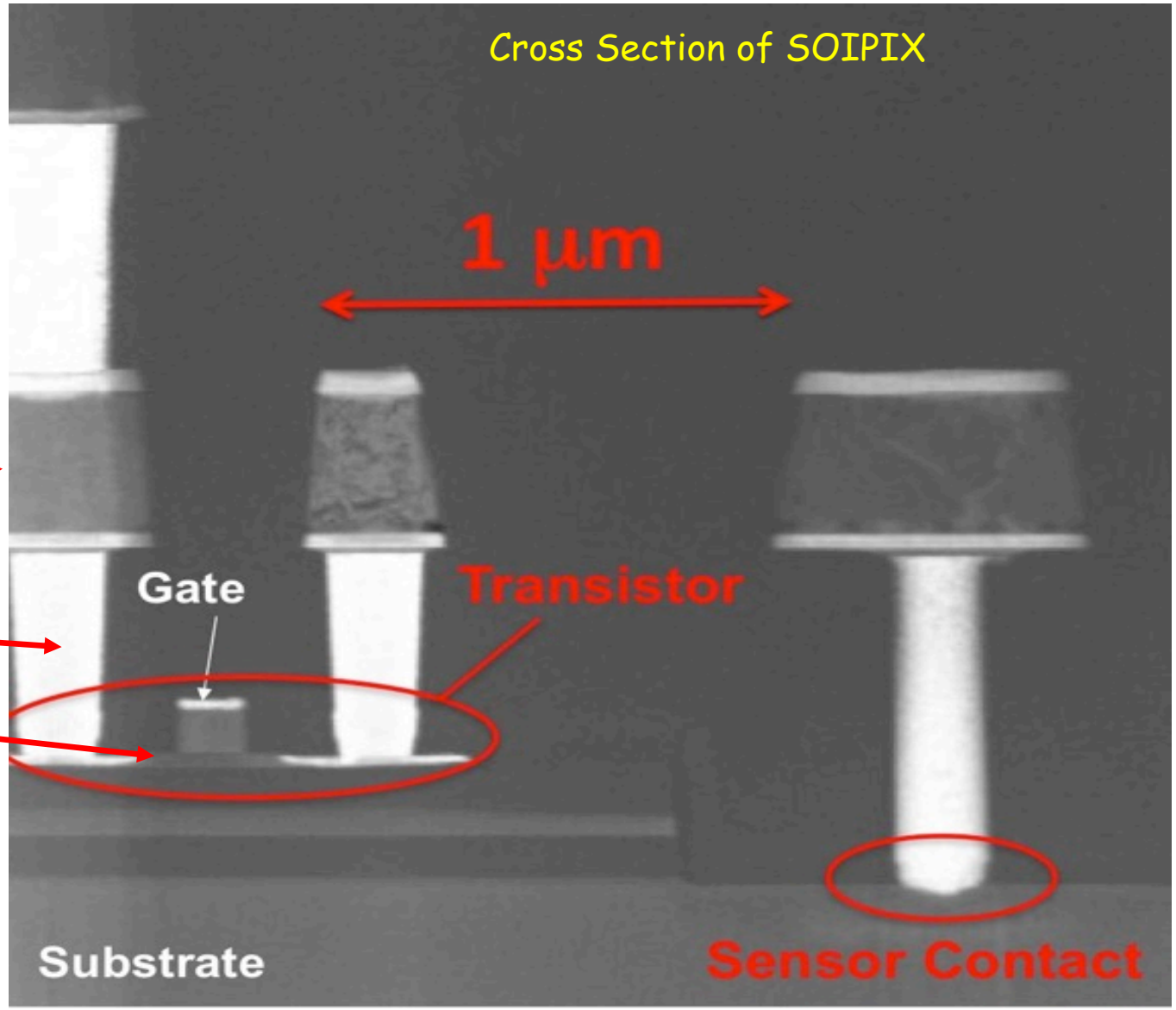
Aluminum metal layer

Tungsten Plugs

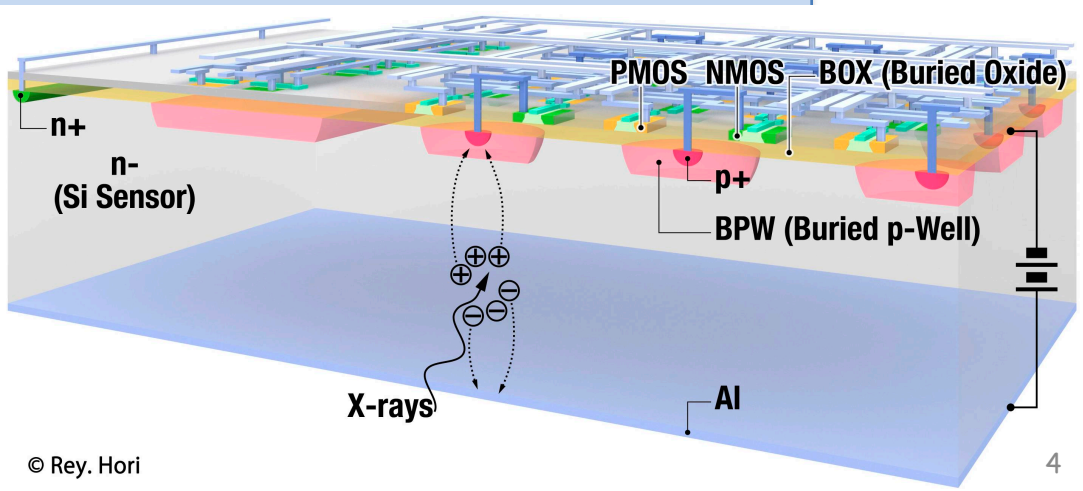
Transistor (40 nm thick Silicon)

SiO_2 layer (140-200 nm)

Substrate (Sensor Silicon)



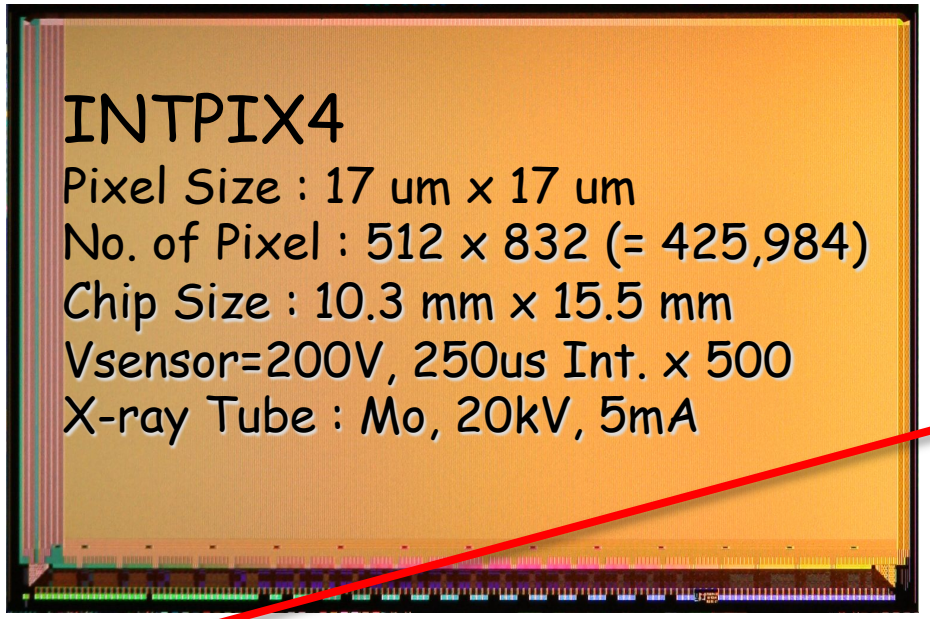
- Working with LAPIS semiconductor, Japan.
- The production is done in the industry semiconductor factory → Reliability, Quality control…
- Standard CMOS technology → Complex circuit can be implemented in the pixel die with the standard CAD tools.
- Sensor thickness from 500 μm to 50 μm (thinning)
- The sensor characteristics can be controlled by impurity implantation design.

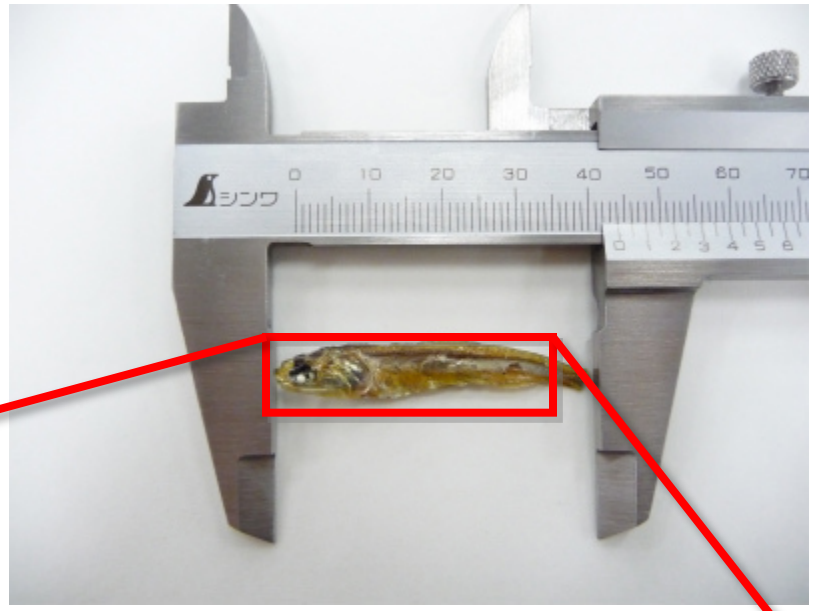


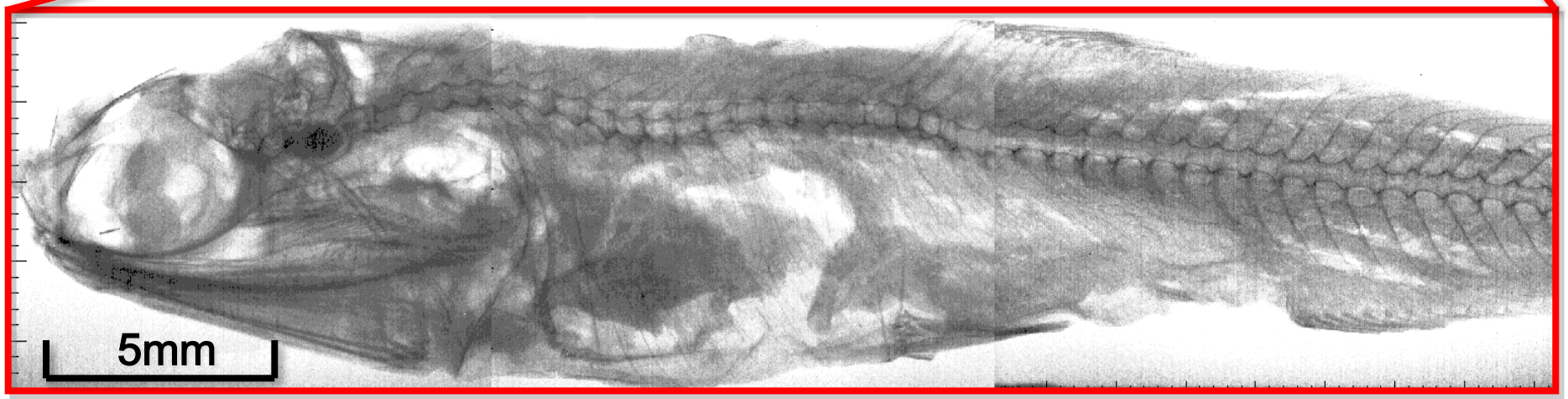
Activities of the SOI pixel sensor group

- 2005 SOI activity started in KEK

First X ray image of a small fish (2010.12)





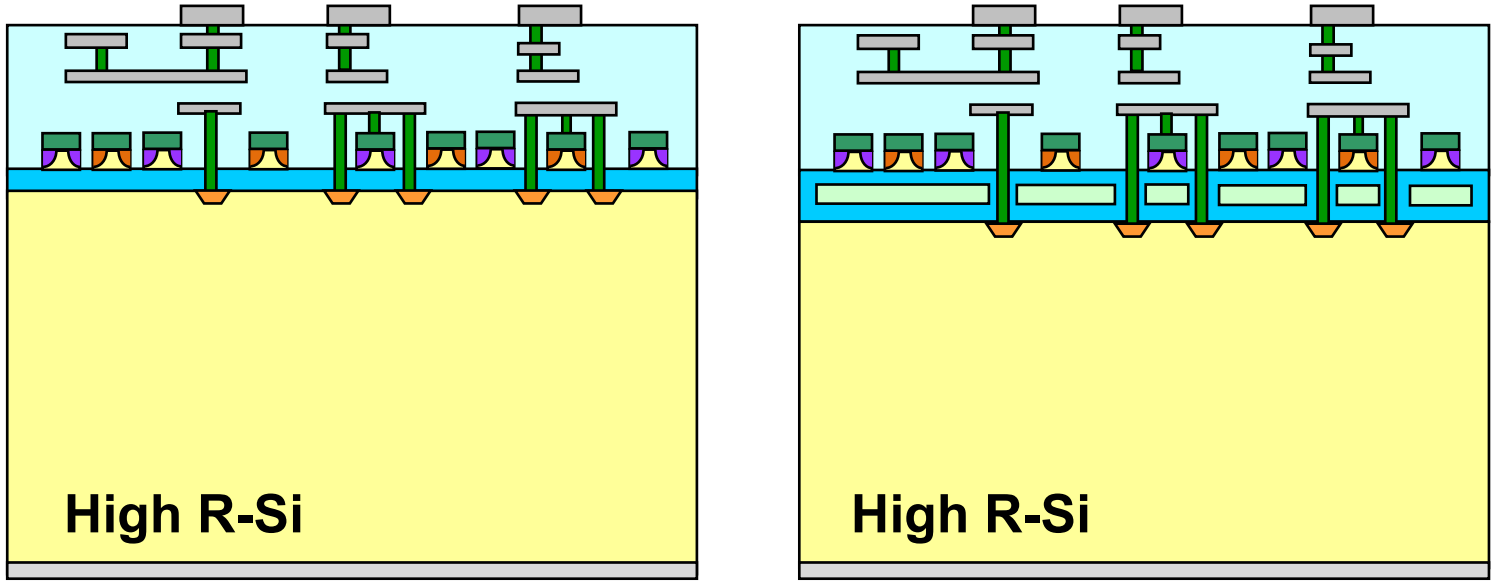


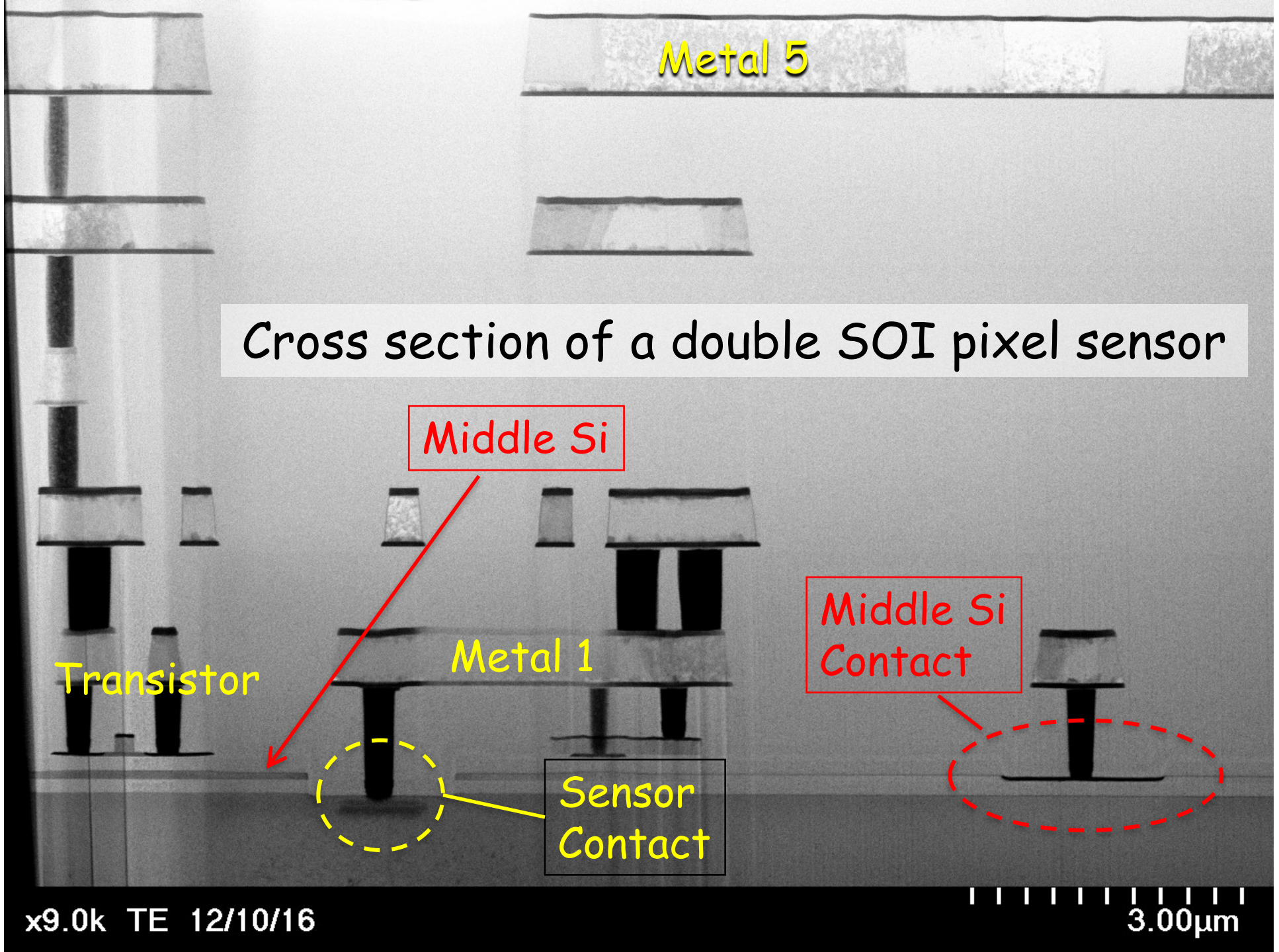
X-ray Image of a small dried sardine taken by a INTPIX4 sensor (3 images are combined).

(A. Takeda)

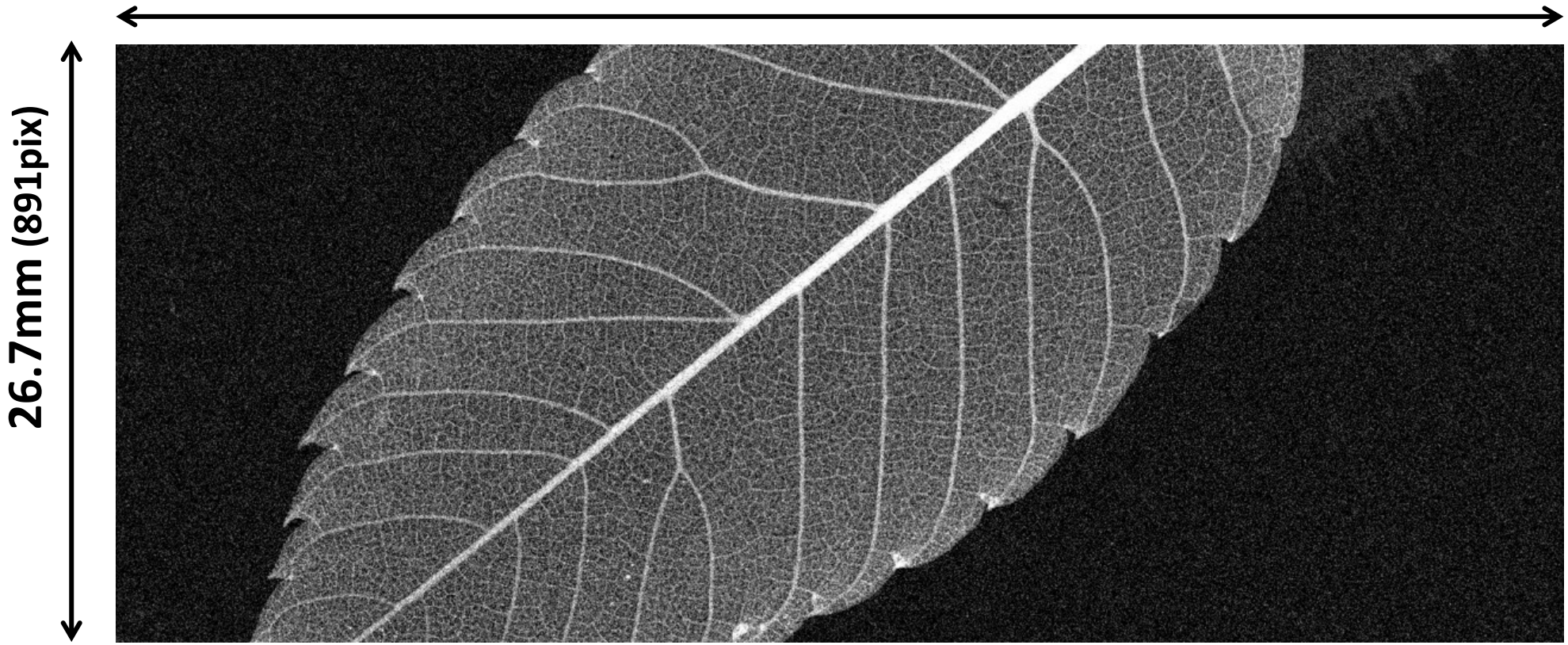
Double SOI (2012-)

- Another SOI structure is added to a SOI sensor.
- The new SOI layer works as shield between the CMOS circuit and the sensor.
- Improve the performance of the SOI pixel sensor.
  - Effect of back bias voltage
  - Digital-Analog interferences
  - Radiation hardness




Metal 5
Cross section of a double SOI pixel sensor
Middle Si
Transistor
Metal 1
Middle Si Contact
Sensor Contact
x9.0k TE 12/10/16
3.00µm

SOPHIAS
for the Free Electron Laser Imaging device

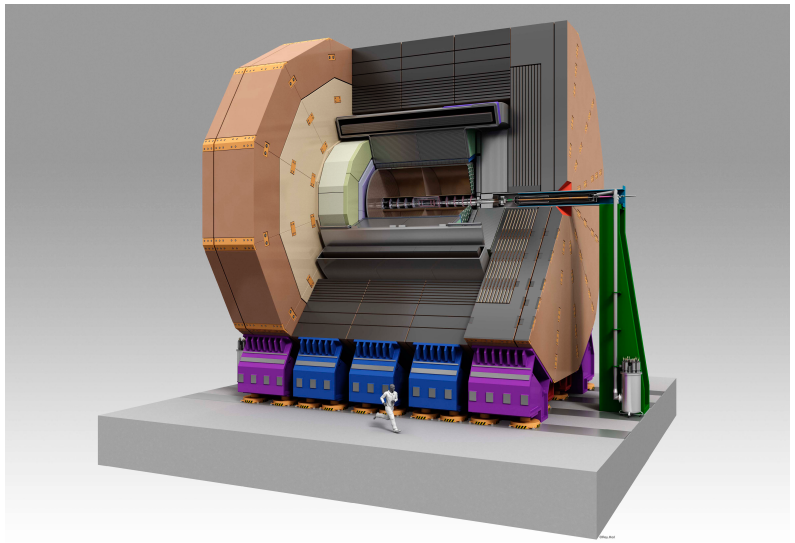


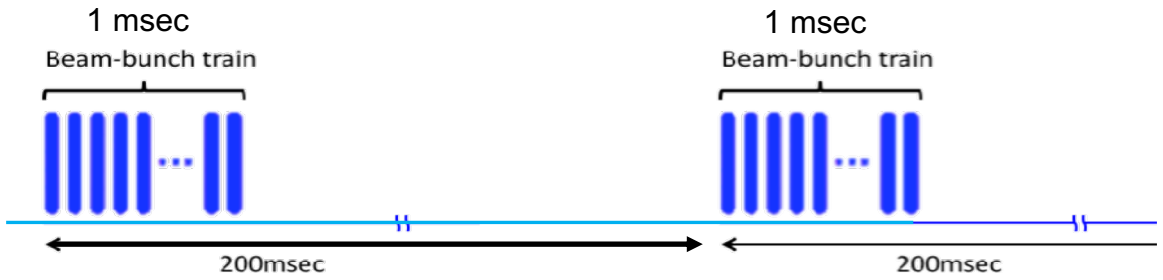
Large size by stitching of 3 reticule size sensor to one.

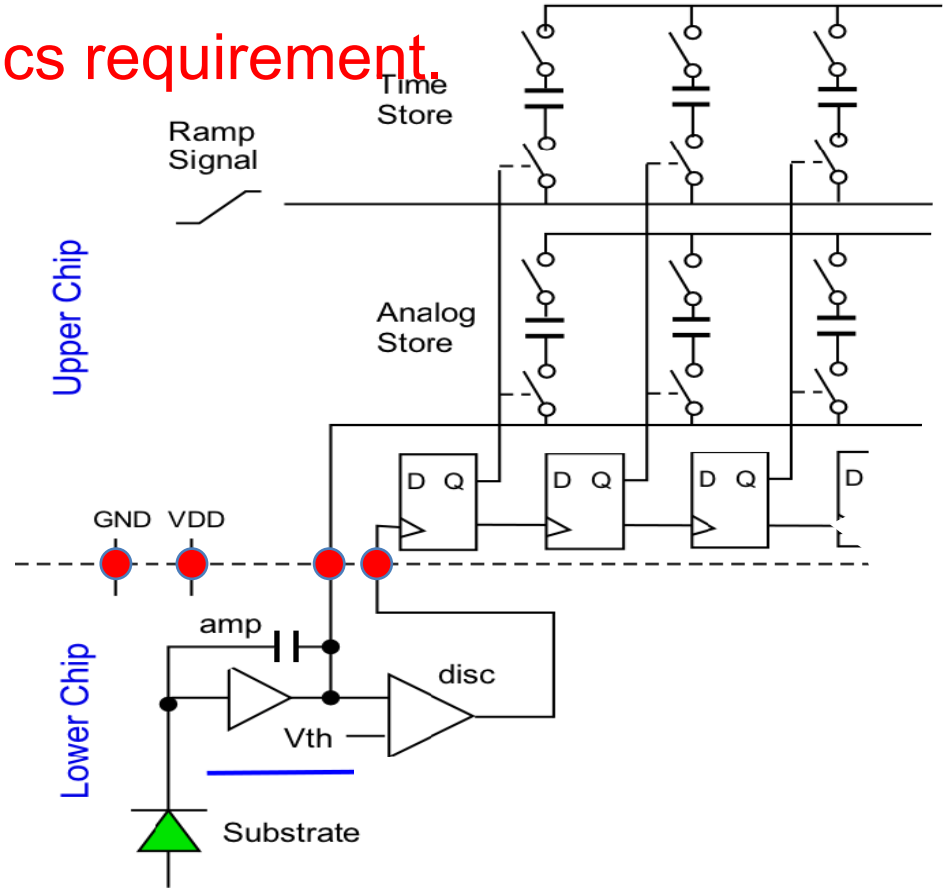
Large dynamic range by combining different gain circuit.

SOFIST (2016-) for the ILC pixel detector

- Beam collision occurs in every 554 ns for 1 msec.
- Hit information should be stored in each pixel and read out in the 200 ms collision interval.
- Pixel size: 20 μm x 20 μm from physics requirement.



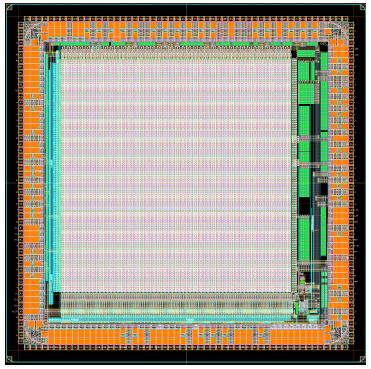




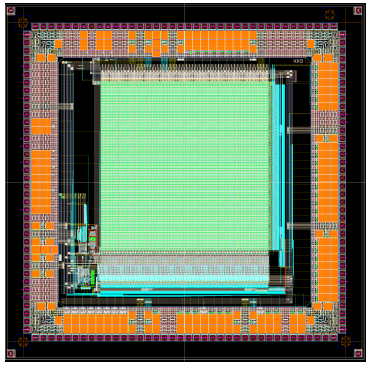
3D integration (2019-)
Stacking of CMOS circuit to achieve more complex function

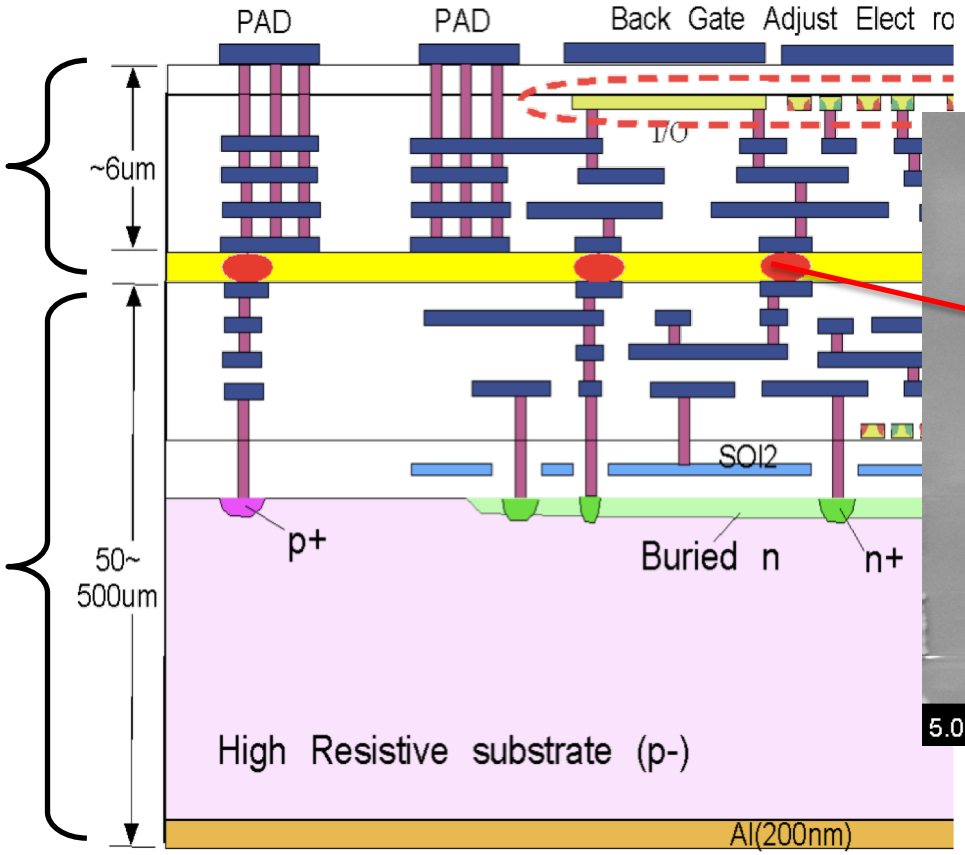
- To integrate such complex functions to a given pixel size (20 μm x 20 μm), we had to add a CMOS circuit onto a pixel sensor.

Upper chip (additional circuit) Thinned to 6 μm thick

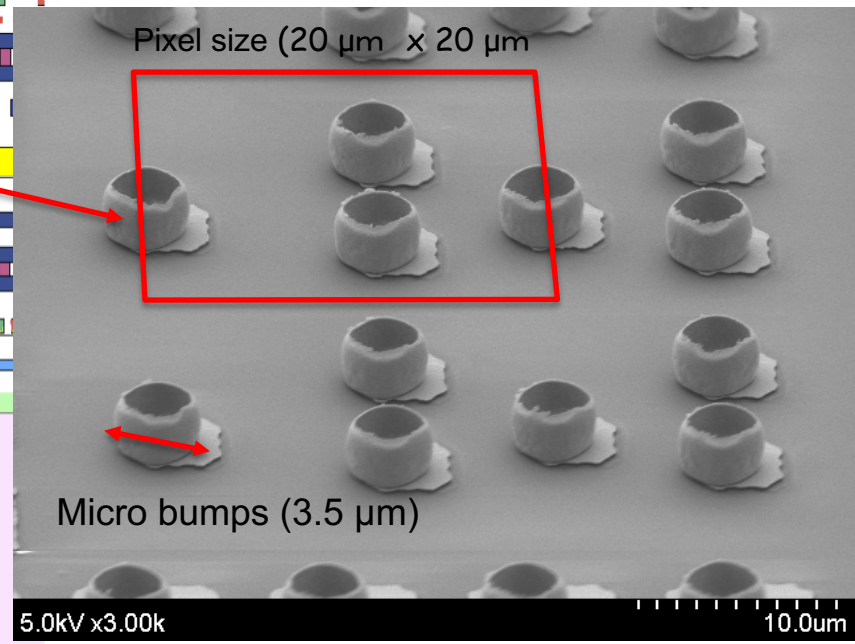


Lower chip (SOI pixel sensor)





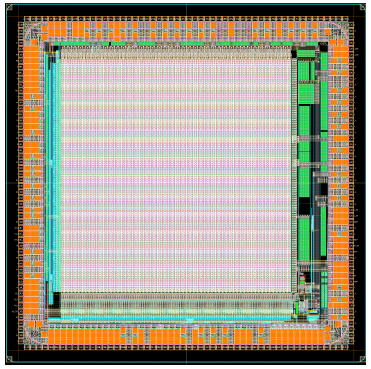
Micro bump for 3D integration



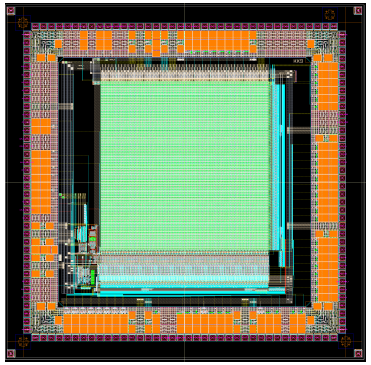
3D integration (2019-)
Stacking of CMOS circuit to achieve more complex function

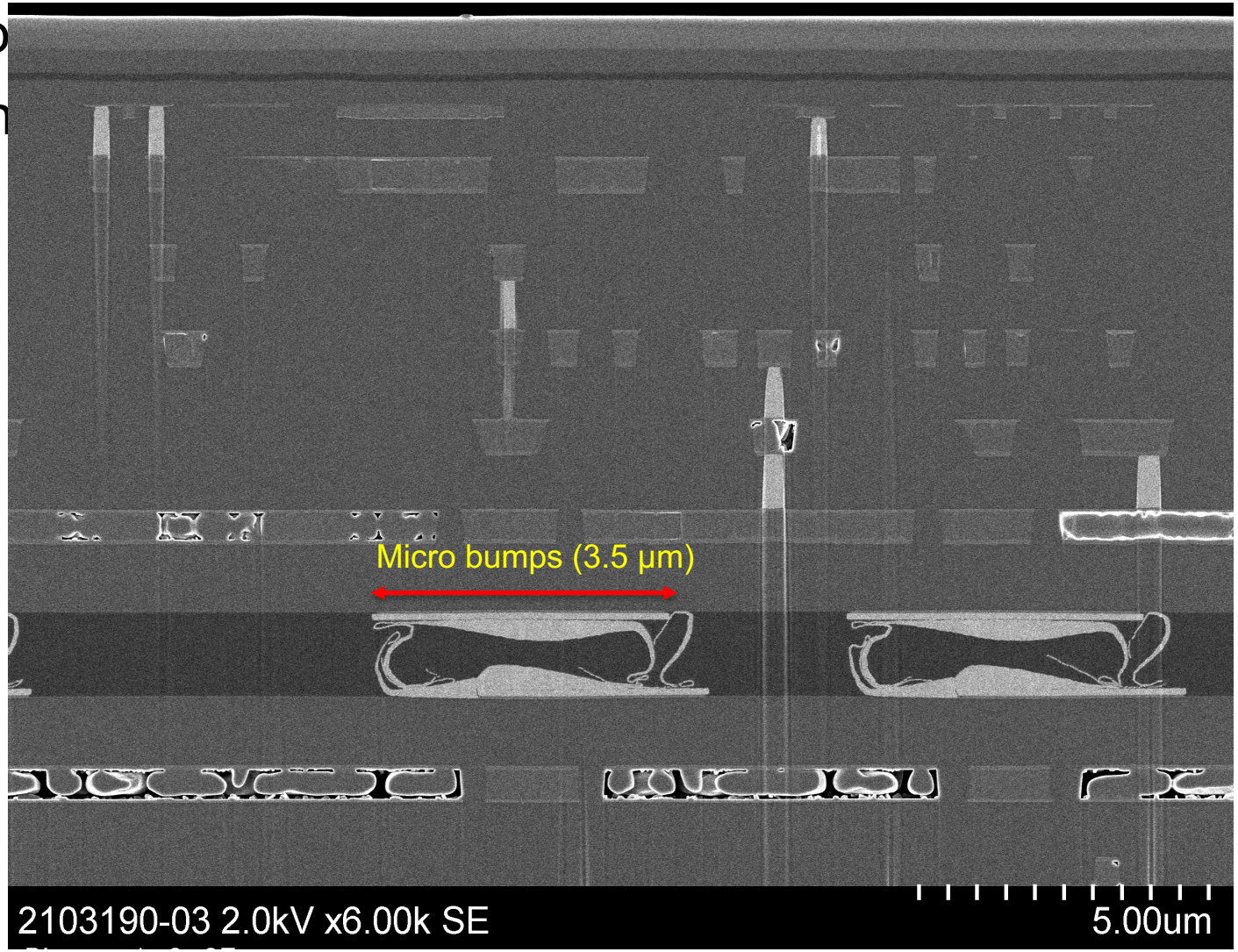
- To integrate such complex functions to a given pixel size (25 μm x 25 μm), we integrated a CMOS circuit to
- Four connection per pixel: Con

Upper chip (additional circuit) Thinned to 6 μm thick



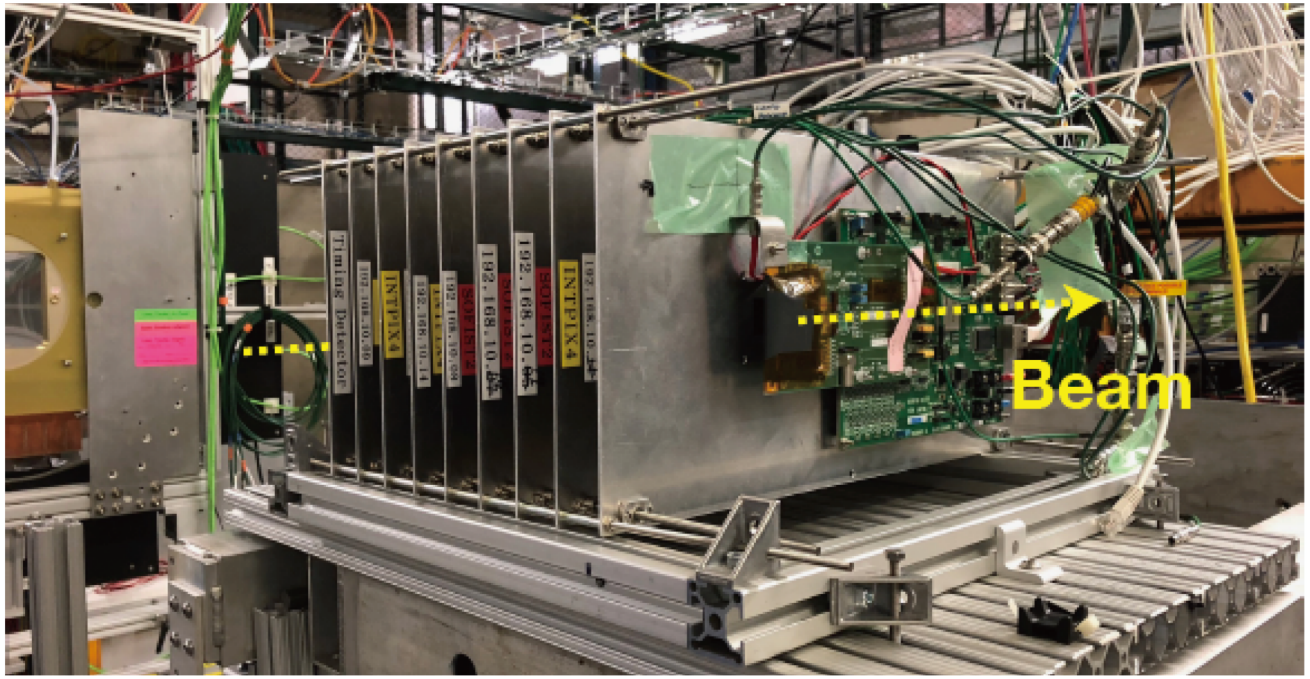
Lower chip (SOI pixel sensor)

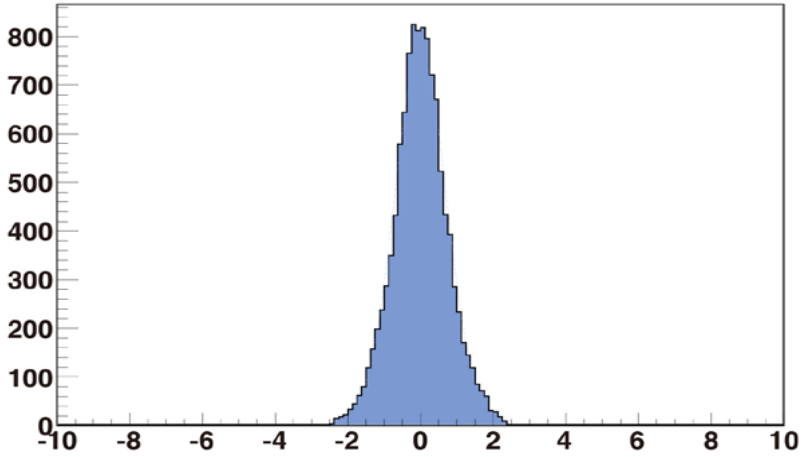




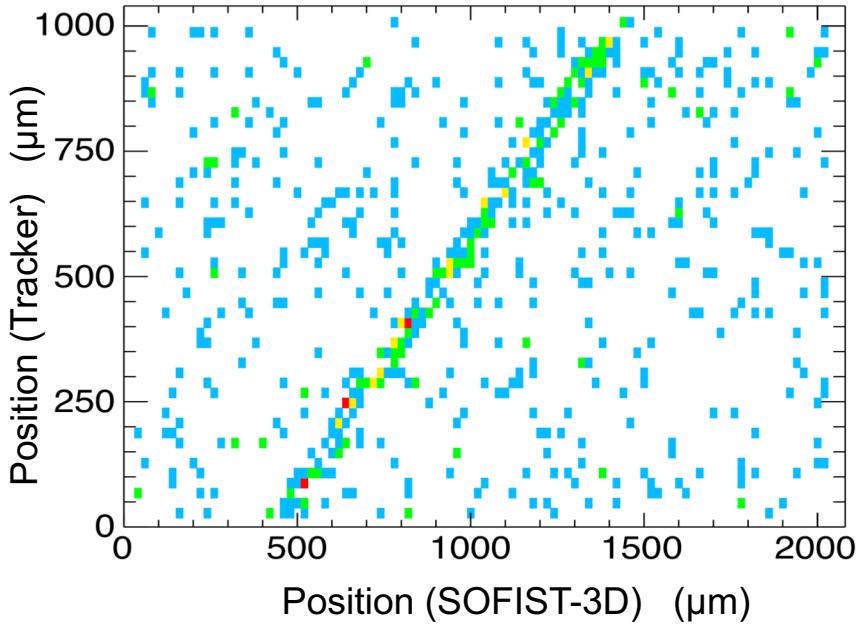
Beam tests at Fermilab 120 GeV proton beam

- 2017 with a 8 μm x 8 μm SOIPIX sensor, FPIX, better than 1 μm position resolution has been confirmed.
- 2020 with the SOFIST sensor (with 3D integration) the MIP particle was observed successfully.

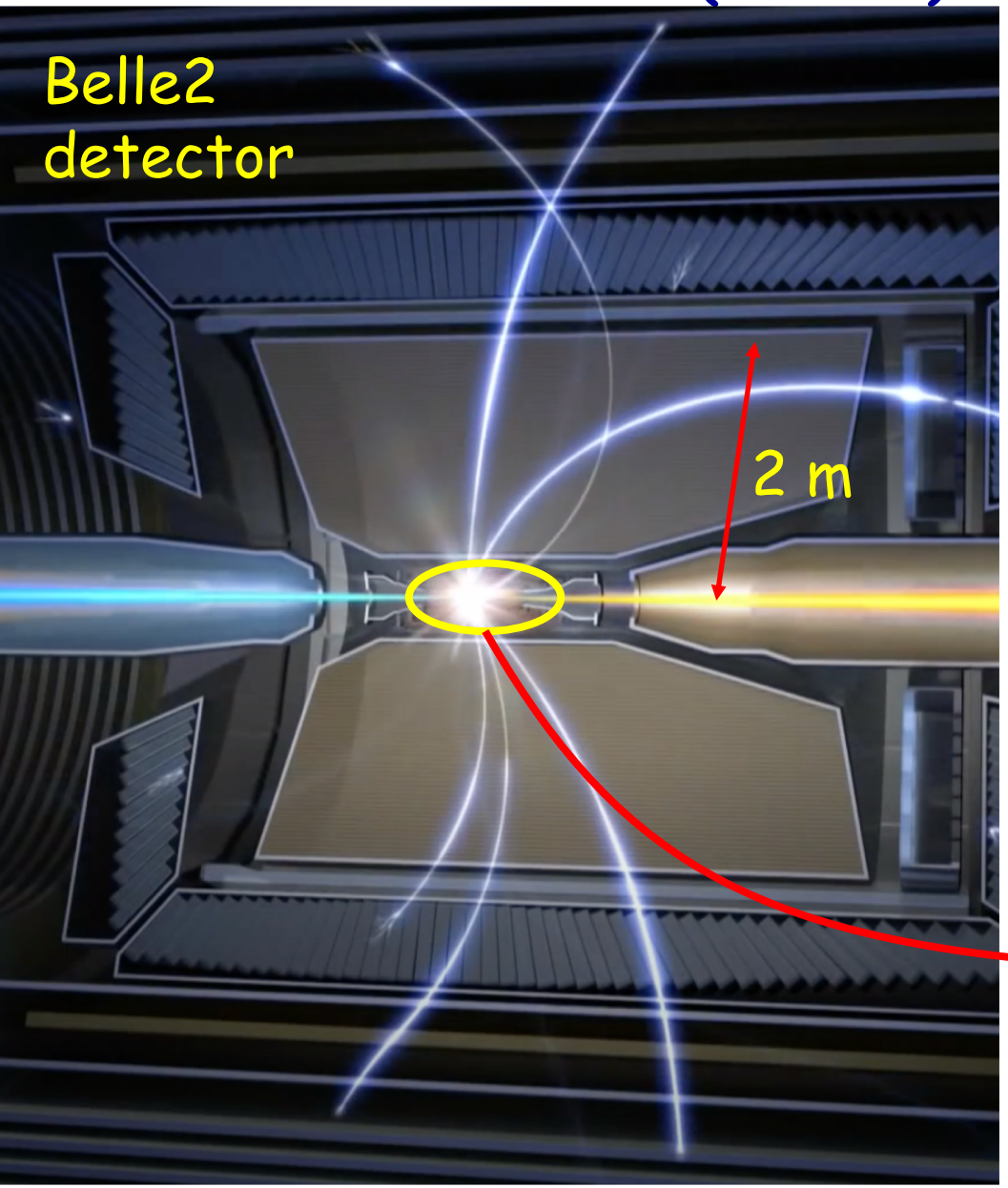




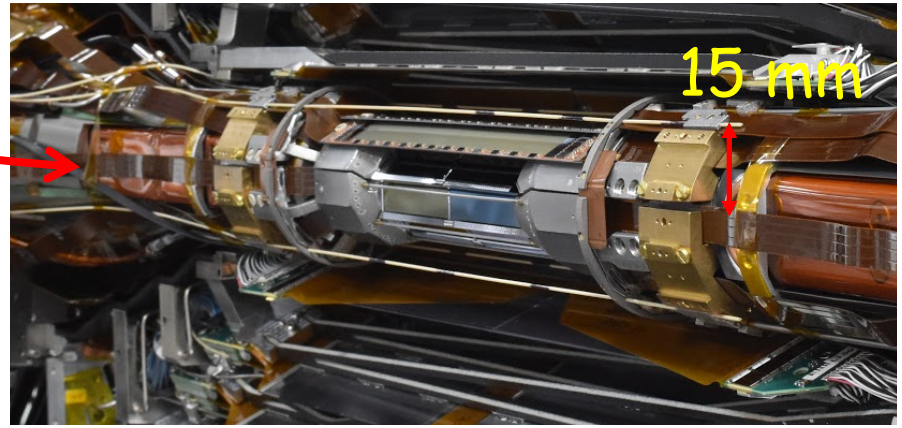
Residual: Tracker- DUT (μm)



DuTiP (2020-) for the Belle II upgrade pixel



- Pixel sensor will be placed 15 mm from Beam
- Beam back ground hits 133 MHz/cm^2.
- Trigger rate 30 kHz
- Trigger decision 5-10 μs
- Pixel size 40-45 μm
- Low power consumption

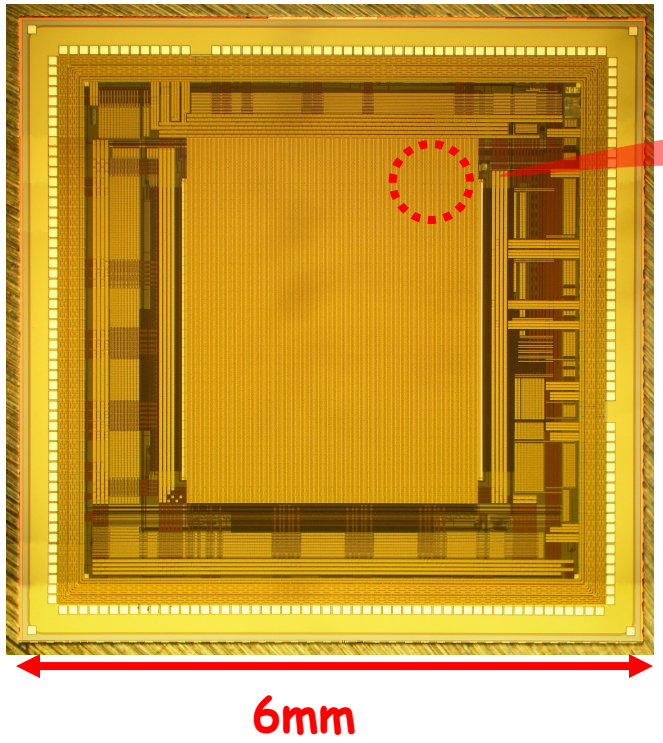


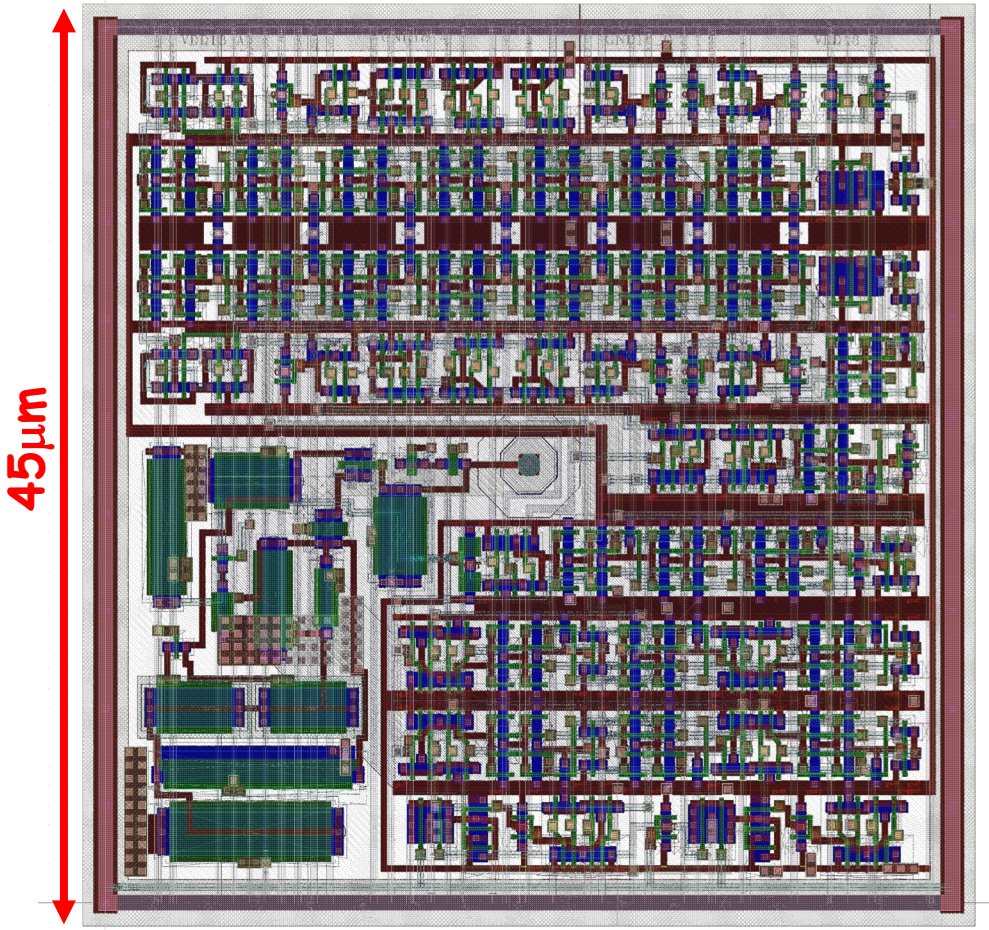
DuTiP (2020-) for the Belle II upgrade pixel detector

Hit reduction by taking coincidence hit with trigger in each pixel.

Hit information should be kept for the decision time in each pixel.

Most complex SOIPIX so far designed.





Belle event trigger (5-10 μs for decision)

100 MHz/cm² background + signal

0.1 μs signal window

Delay (5-10 μs for decision)

Back ground rate
< 0.001 hits/trigger/pixel

Efficient for physics signal.

What Can We Provide for the EIC ?

- Input parameters for pixel sensor design
  - Necessary spatial resolution → Sensor thickness and pixel size.
  - Distance from the collision point → Chip size
  - The following parameters are necessary to determine the circuit and readout scheme of the pixel sensor.
    - Beam collision frequency or interval
    - Trigger rate / Trigger latency /Data acquisition scheme.
    - Back ground rate.
    - Signal hits /event.

Summary

- SOIPIX is a monolithic pixel sensor with the standard CMOS circuit and (almost) arbitrary structure of the radiation sensor.
- We have developed various sensors for Xray.
- It also fits particle physics experiments.
- We have designed and produced the prototype sensors for the ILC and Belle pixel detector.
- Even small pixel size, we can integrate necessary circuits by using the 3D stacking.
- We need some more information to start chip design.