HINP16/32C

HINP for RIKEN – March 2011

Rebecca Shane

(for Lee Sobotka, Bob Charity, Jon Elson and George Engel)

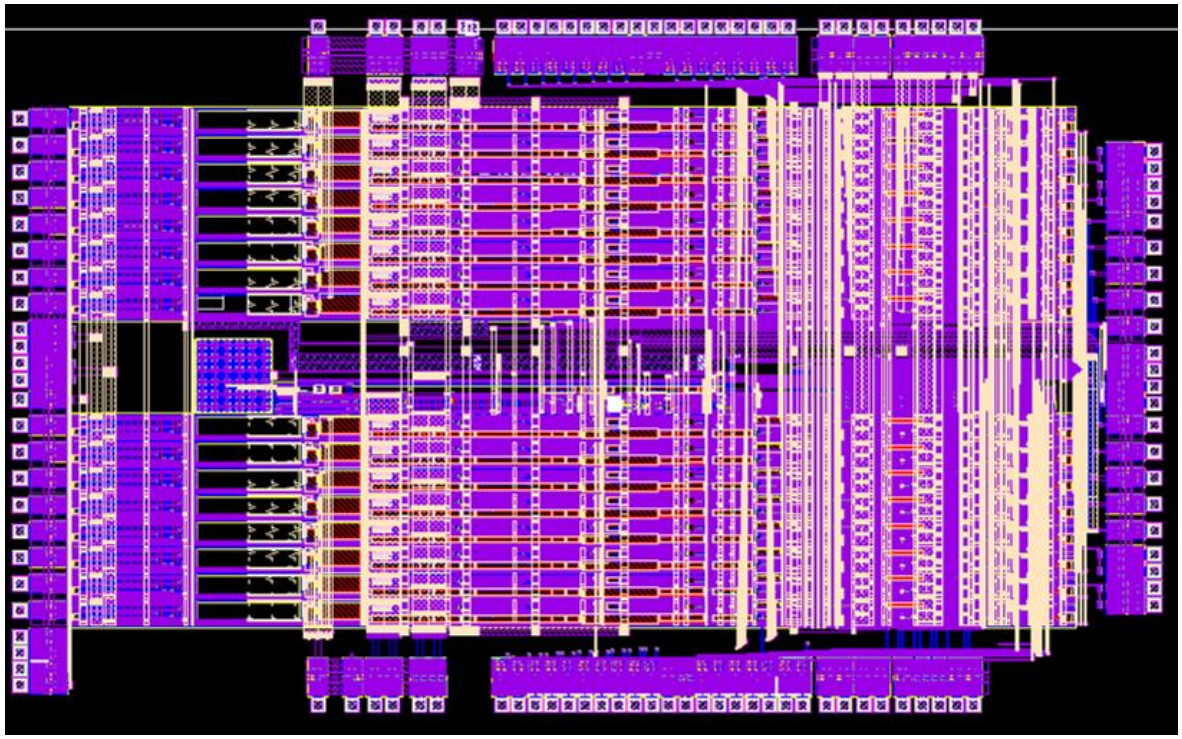
SIU

SOUTHERN ILLINOIS UNIVERSITY EDWARDSVILLE

VLSI Design Research Laboratory

Washington University in St. Louis

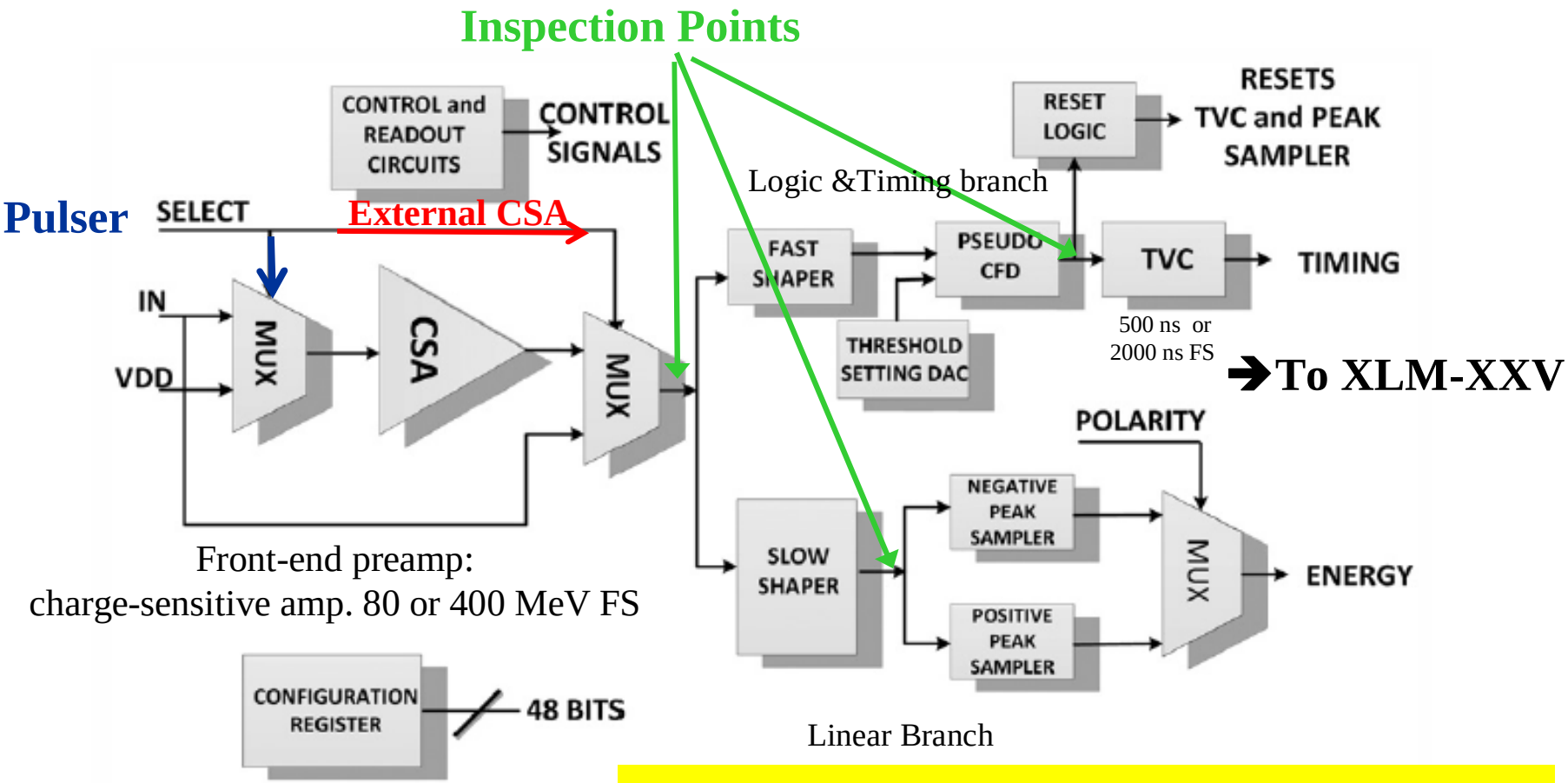
Nuclear Reactions Group Charity-Sobotka



Si ===> CSAs - Shaper - Peak Sen- DISC

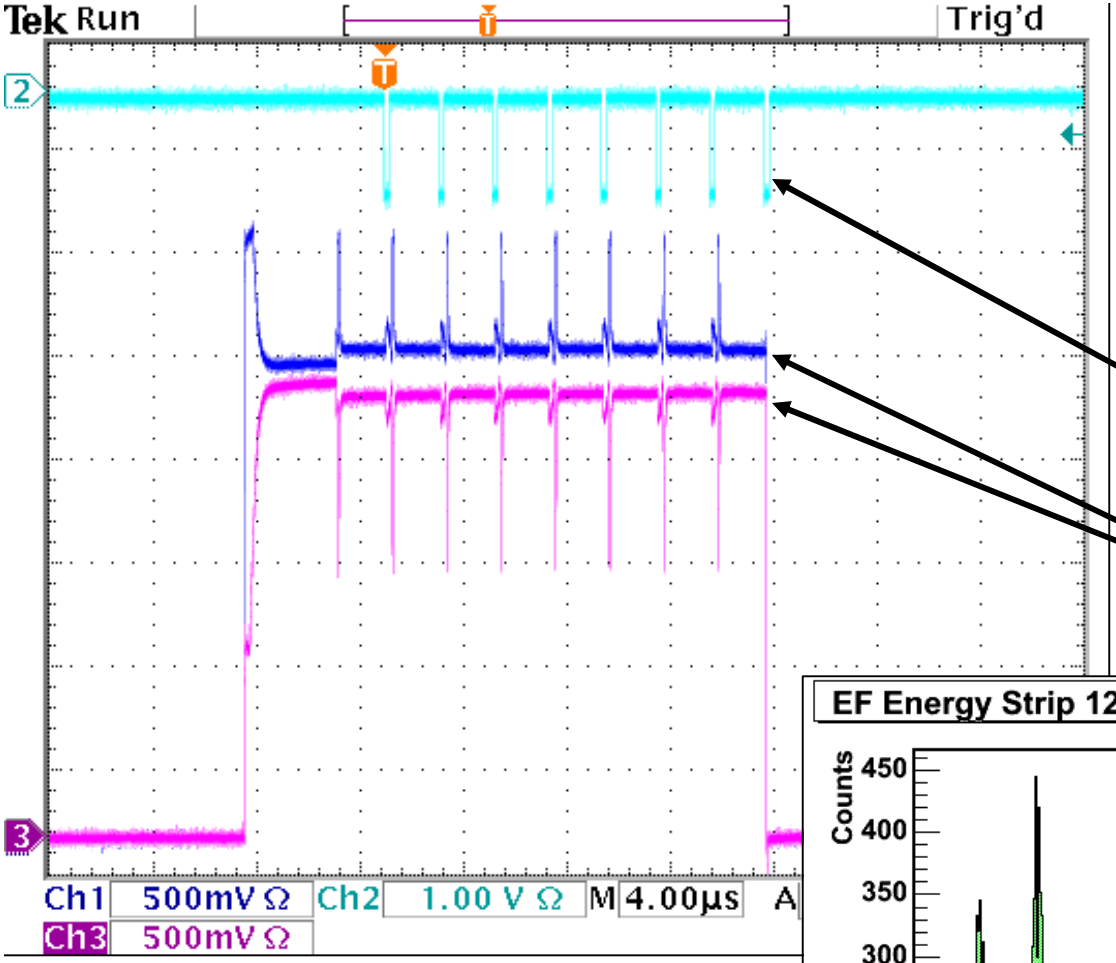
1. **Chip reference: G.L. Engel et al., NIM A573, 418 (2007)**
2. **Implementation documentation: On request**

HINP (REV3) Readout and Acquisition



Choice of
1.CSA: Internal 80 or 400 MeV or external CSA
2.TVA range: 500 or 2000 ns
3.Disc setting
4.Inspection mode
5.All readout timings
6.Chip is really 32 ch, only popoulated16 of the ch.

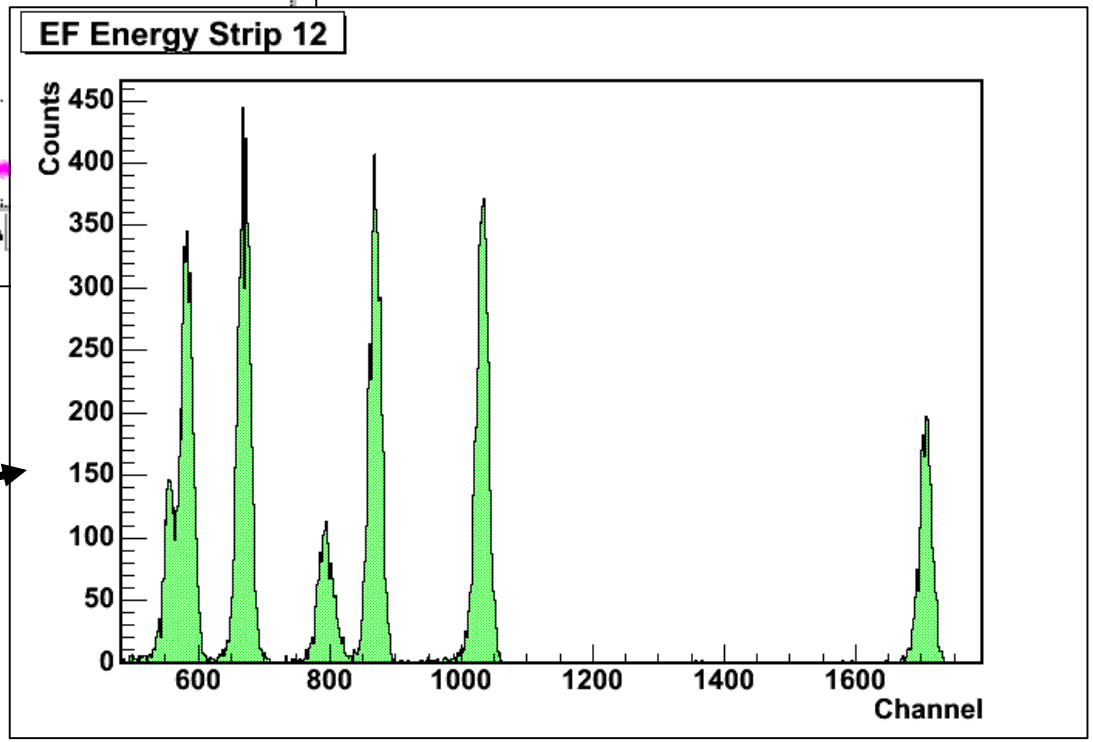
The XLM
a) controls the readout sequence and
b) Receives three "trains": Address, Timing, Energy



The Signals go from the ASIC chip to a differential amp and then to a pipeline ADC.

Strobes to pipeline ADC

Differential Signals



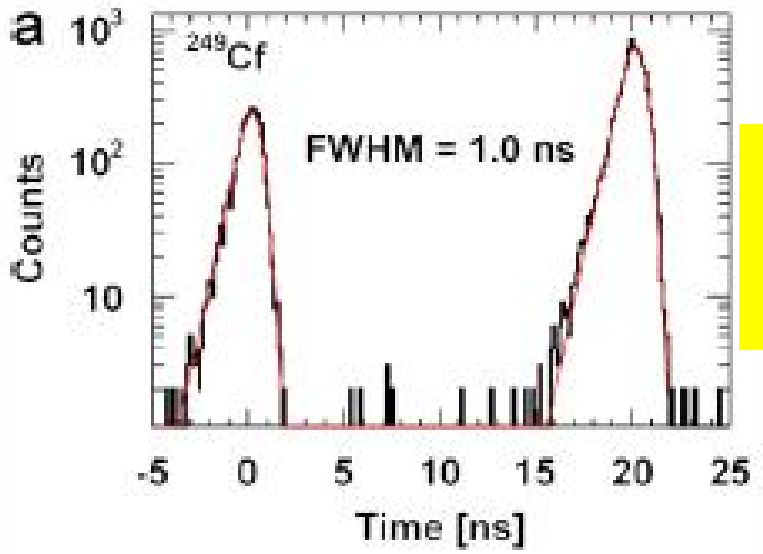
α spectrum ^{228}Th source

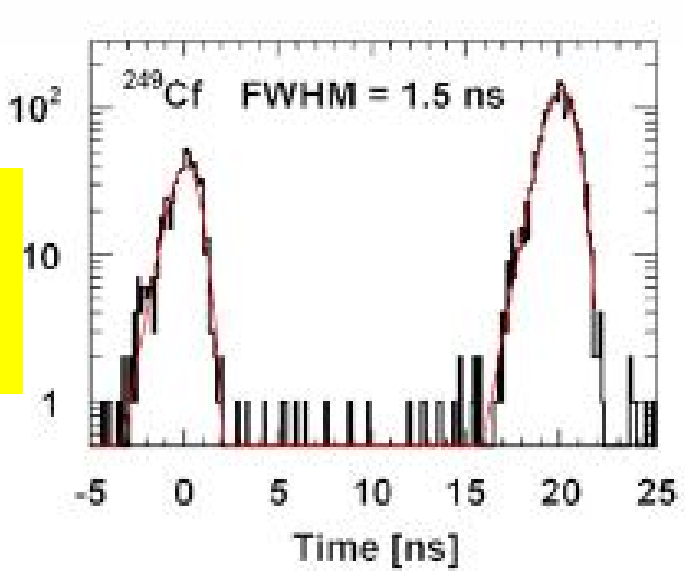
External and Internal CSA

τ_{decay} ~ 25 μs.

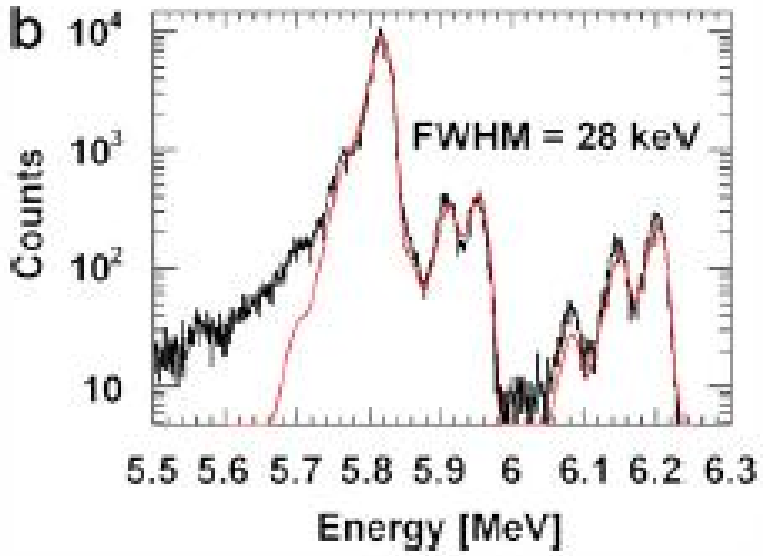
α – γ Coincidence

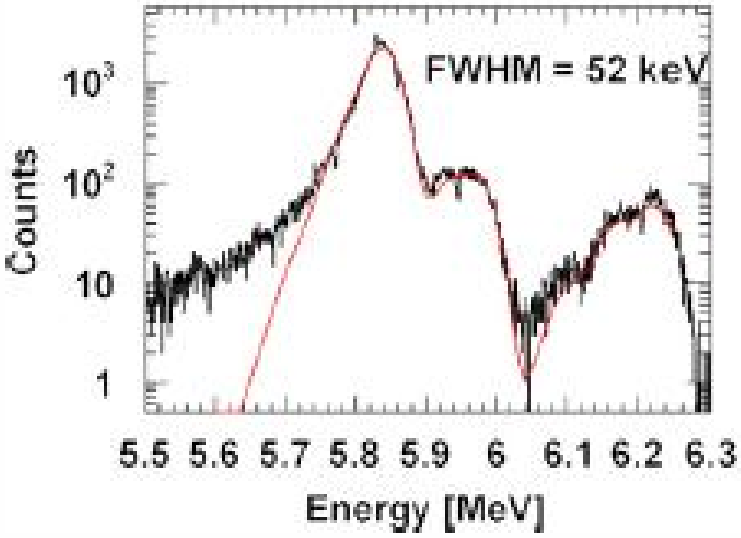
State has τ = 0.65 ns



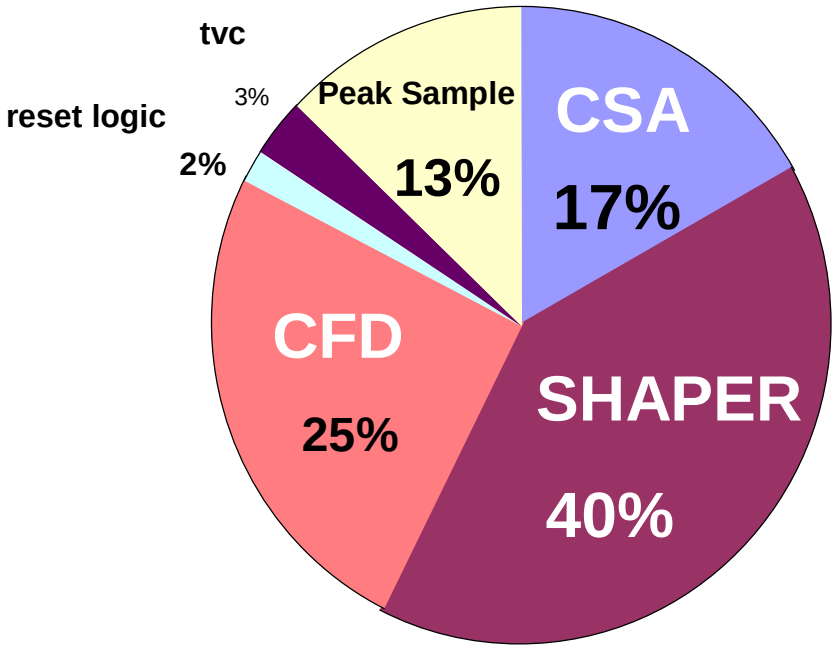


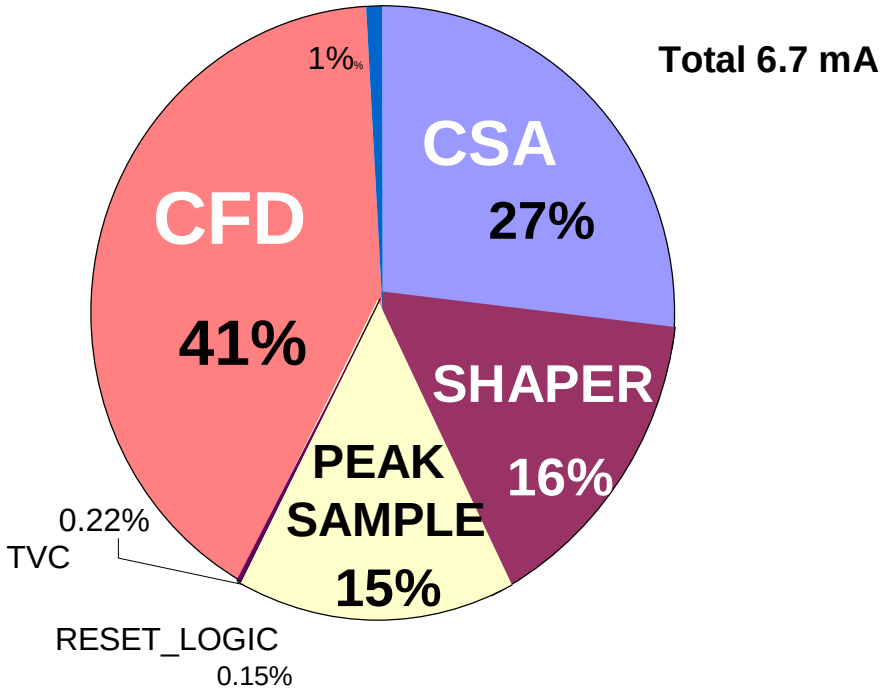
α spectra





Area and Power Breakdown





Shaper dominates

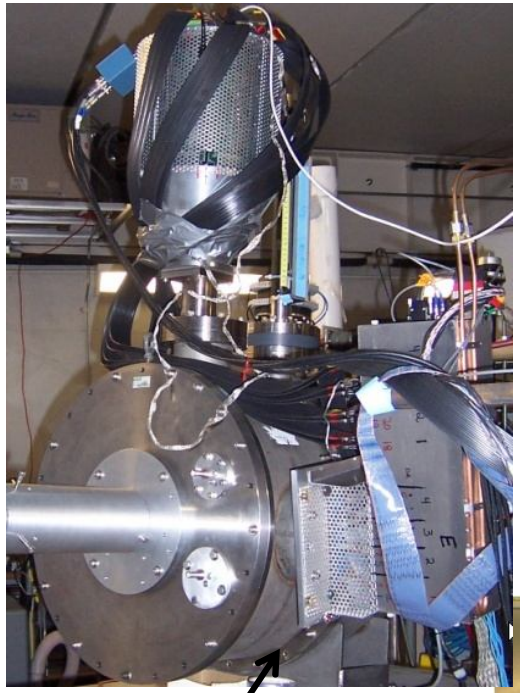
Lower-gains need larger shaper

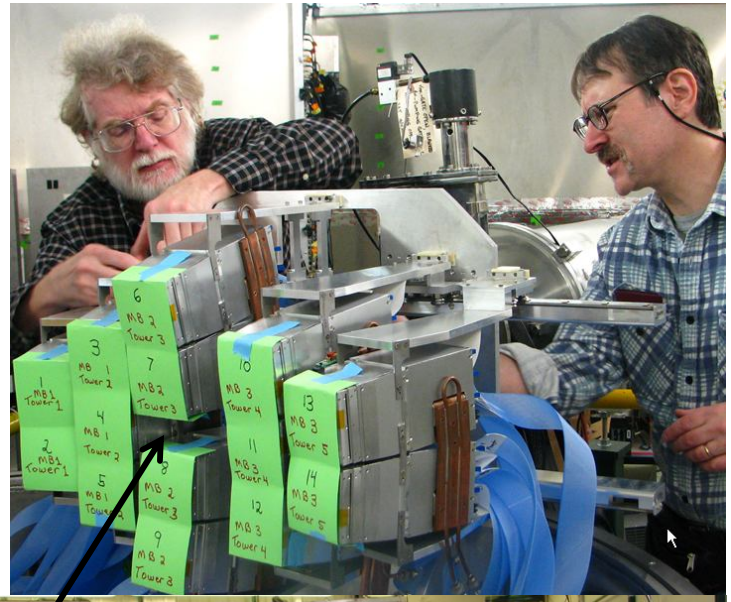
Higher gains need larger/different CSA design

Discriminator dominates

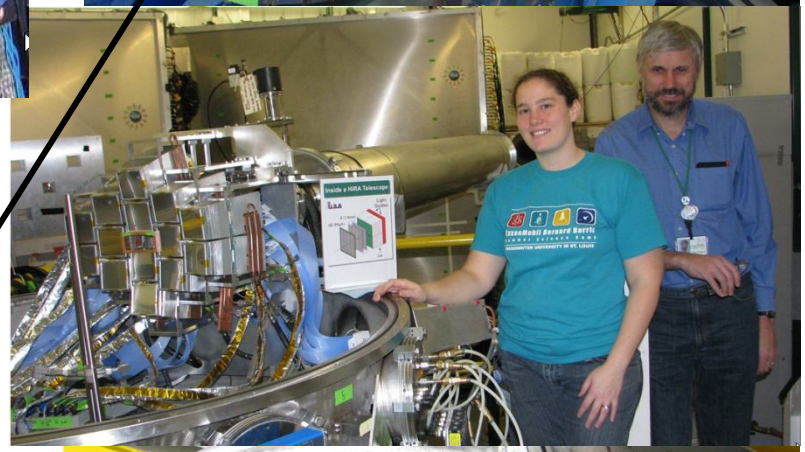
Total power ~ 30mW/ch ~ 1W/32ch

Air flow or active cooling (in vac) needed.





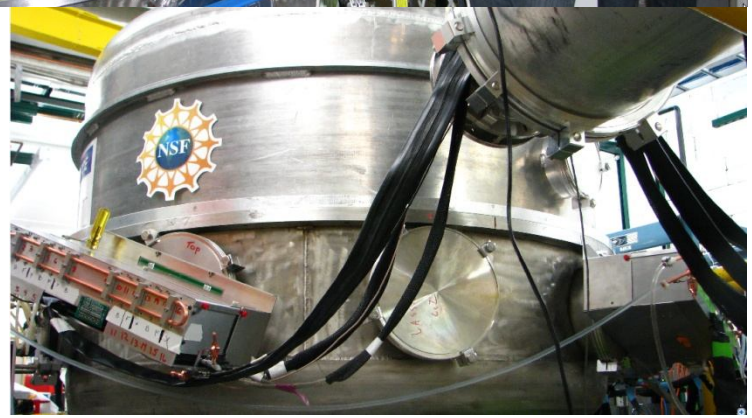
Si in vacuum
Ele. outside



1. **Initial test system at WU**
2. **Small-scale setup at TAMU** (~ 400 ch)

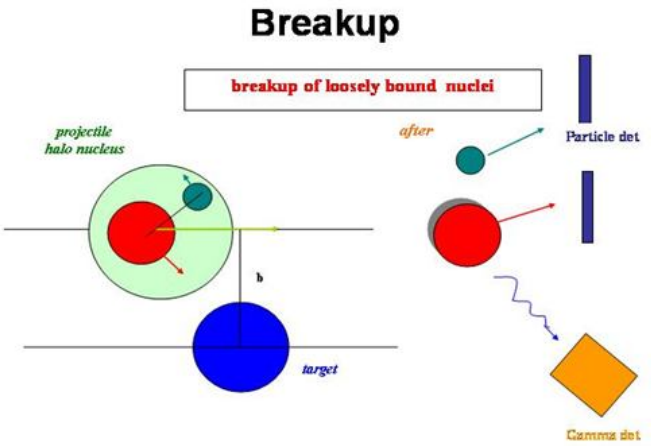
   dE's external CSA
3. **Large-scale setup at MSU (**1000-2000 ch)

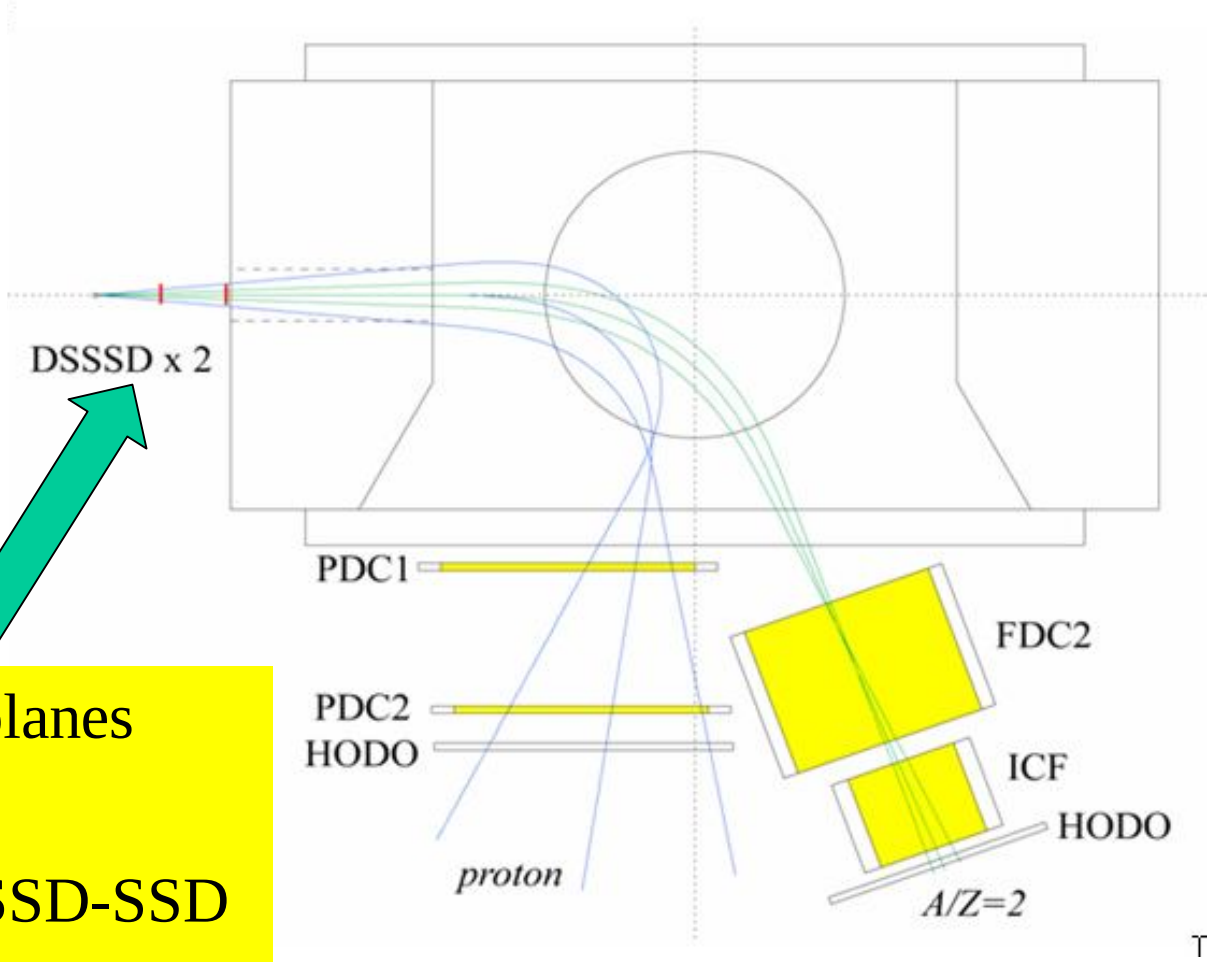
   dE's also run in external CSA mode



AT RIKEN

Secondary beam ➔ target ➔ LI +HI tracking ➔ SAMURAI ➔ proton and HI hodoscopes





XY – (W?) - UV Si planes

Either

a) SSD-SSD ---SSD --- SSD-SSD

b) DSSD ---- SSD ---- DSSD

b) Preferred due to:

i) Delta e- problem & ii) p threshold issue

Issue: dynamic range, p triggering , keeping HI on scale

Energy Loss in 300 μm Si (69.6 mg/cm^2)

Z	Ion	100 MeV*A	200 MeV*A	350 MeV*A	[dE(Z)-dE(Z-1)]/dE(Z) At 350 MeVA (same
1	**p**	**0.404 YES**	**0.250 NO with 300 μm YES with 500 μm**	**0.186 NO need ext CSA**	**Trigger with internal CSA**
3	^{6}Li	3.6 [MeV]	2.7 [MeV]	1.65 [MeV]	
6	^{12}C	14.6	9.1	6.6	30%
8	^{16}O	26.1	16.1	11.7	
10	^{20}Ne	40.9	25.4	18.4	19%
14	^{28}Si	80.5	49.9	36.3	
18	^{40}Ar	133.	82.7	60.2	11%
20	^{40}Ca	164.	102.	74.4	
26	^{56}Fe	277.	173.	126.4	8%
30	^{64}Zn	368.	231.	168.9	
36	^{86}Kr	526.	333.	244.3	5%
40	^{90}Zr	645.	411.	302.5	
50	^{120}Sn	986.	641.	475.2	3

Needs extended range ASIC

OPTION A

The “GLAST” Si
1D from Hamamatsu
384 ch, 228 um pitch (overkill)

OPTION B

TTT from Micron
(available in 2-sided)
128 ch, 758 um pitch

<u>COMMENT from WU:</u>

Prefer option B for the following reasons:

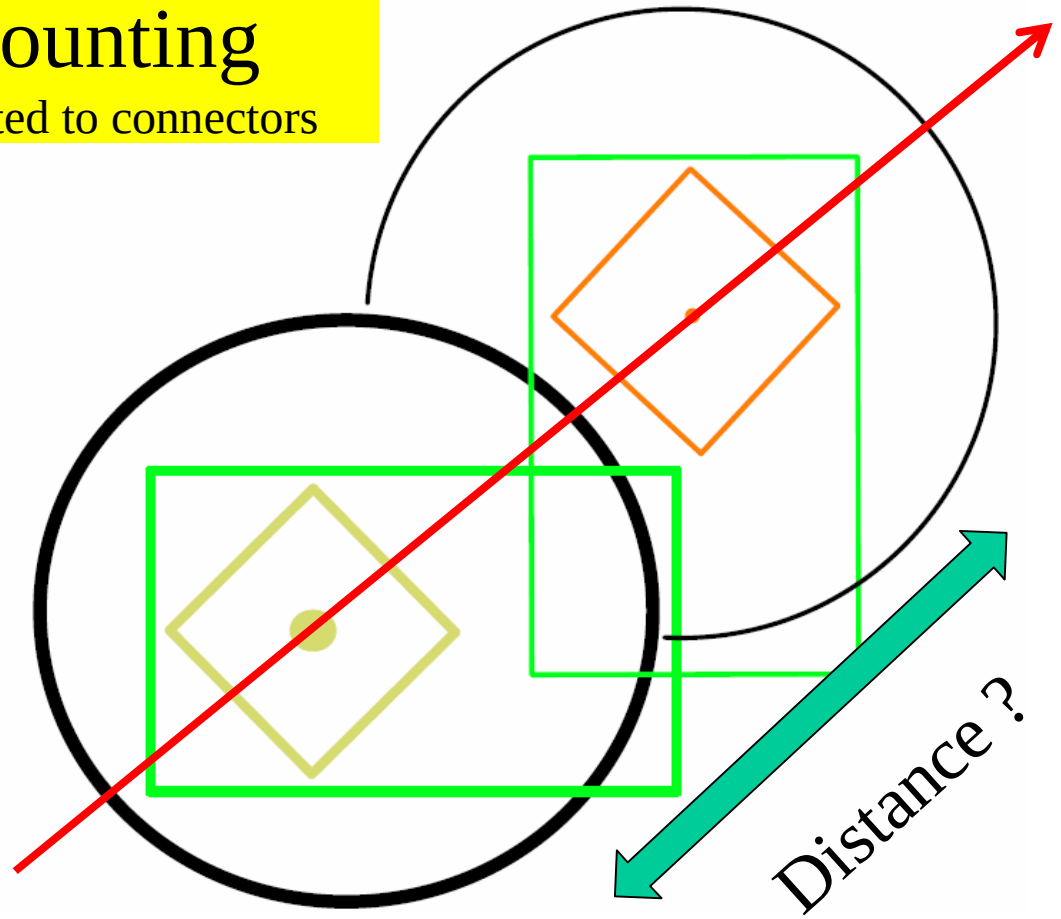
1. Reduces delta e^- problem
2. Can get 500 μm
   (need for p triggering > 150 MeV/A)
3. Perhaps can get with central hole

Table 1
Specifications of the GLAST-Flight-Model SSD

Items	Specifications (units)
Outer dimensions	$89{,}500 \pm 20 \times 89{,}500 \pm 20$ (μm^2)
Active area	$87{,}552 \times 87{,}552$ (μm^2)
Substrate thickness	410 ± 10 (μm)
Strip pitch	228 (μm)
Number of strips	384
Width of implant-strip	56 (μm)
Width of Al readout electrode	64 (μm)
Resistance of implant-strip	<30 (kΩ/cm)
Resistance of Al readout electrode	<50 (Ω/strip)
Full depletion voltage	<120 (V)
Resistance of isolation resistor (variation within a chip)	50 ± 30 (MΩ) ± 10 (MΩ)
Capacitance of coupling capacitor (at 10 kHz)	>500 (pF)
Leakage current	
(at $V_b = 150$ V)	<500 (nA)
(at $V_b = 200$ V)	<600 (nA)
Bad channel rate (average)	<0.2 (%)
Bad channels allowed in a chip	⩽3 (number of strips)

Concept Drawing
Diamond mounting

Traces from 2 sides routed to connectors

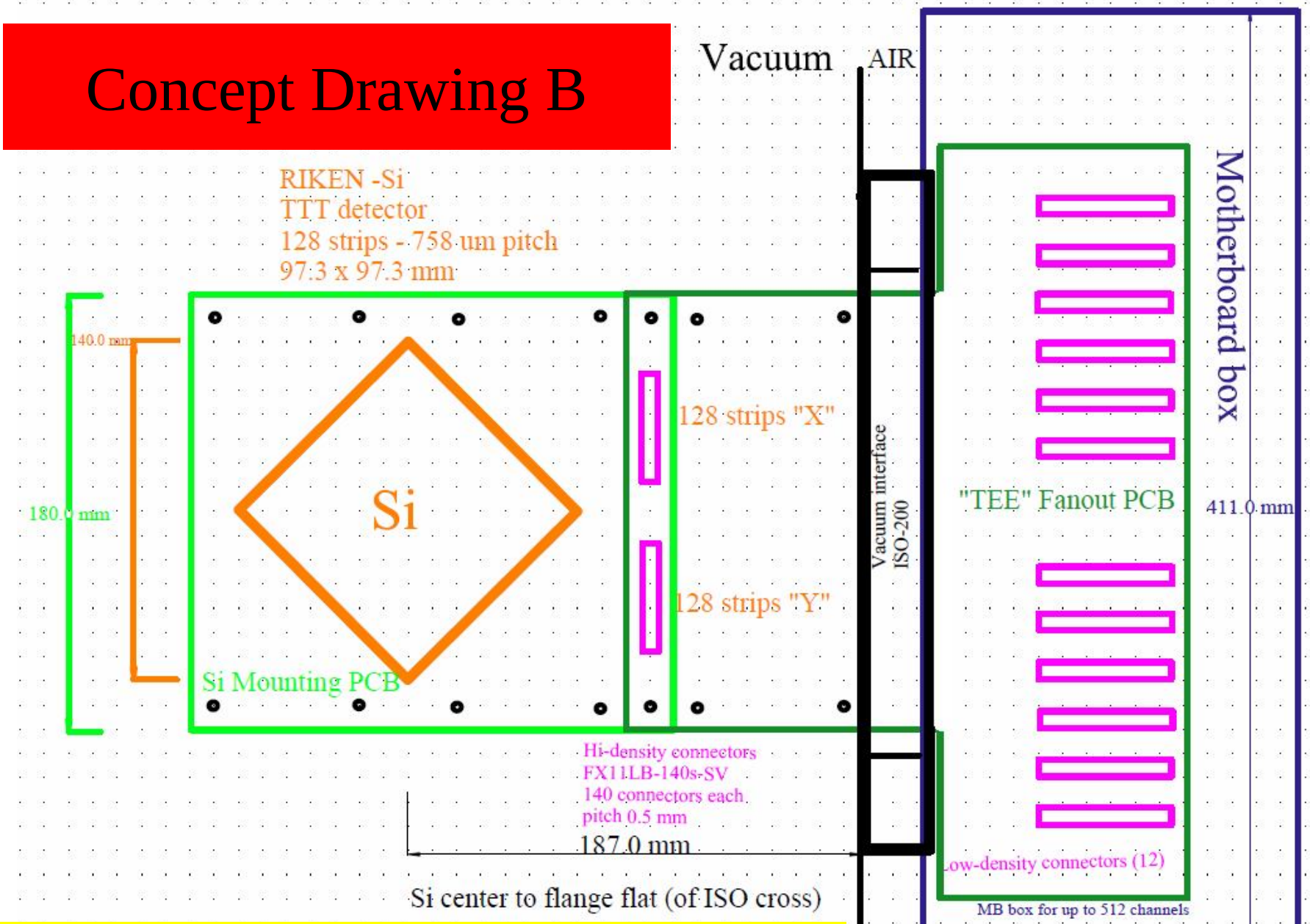


When do we need 5th ambiguity layer?

What if these were not exactly 90o?

In any event do not need for 1p knockout.

Concept Drawing B



Use MB for only 256?

If not, how to “TEE” in other 128 ch

Test rigs at WU and TAMU with existing PCB mounting

We have started to test with the 2D TTT (300 um)

AREA ➔97.3 x 97.3 mm

strips ➔128 x 128 ➔ 256 per Si, 512 per pair

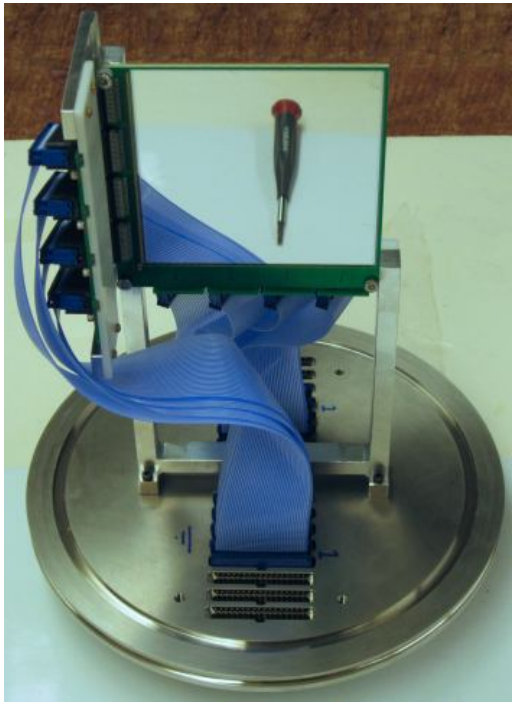
Pitch ➔ 756 um

Si type ➔ available in both n and p (intrinsic). We have one of each

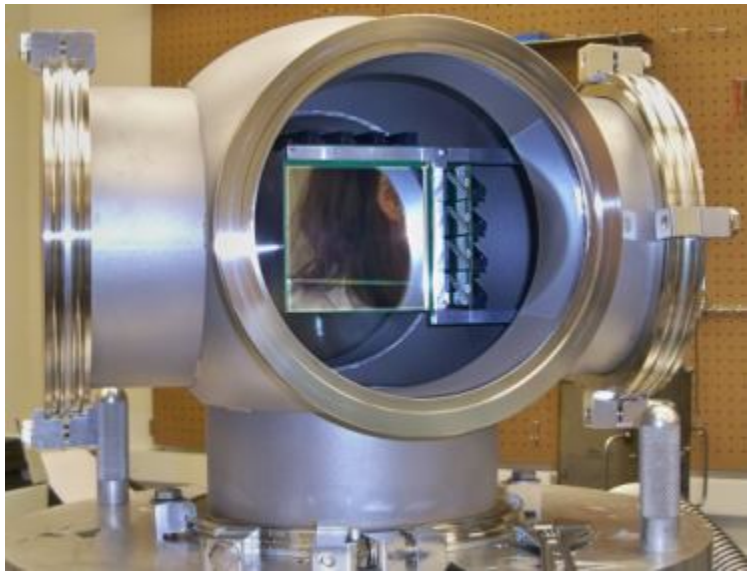
Thickness ➔ available in both 300 and 500 μm, we have 300 μm.

pf ➔ 300 μm: 0.35 pf/mm^2 = 26 pf/st; 500 μm: 0.21 pf/mm^2 = 15.4 pf/st

Si –TTT (WU)



Si in chamber (TAMU)



External view (WU)

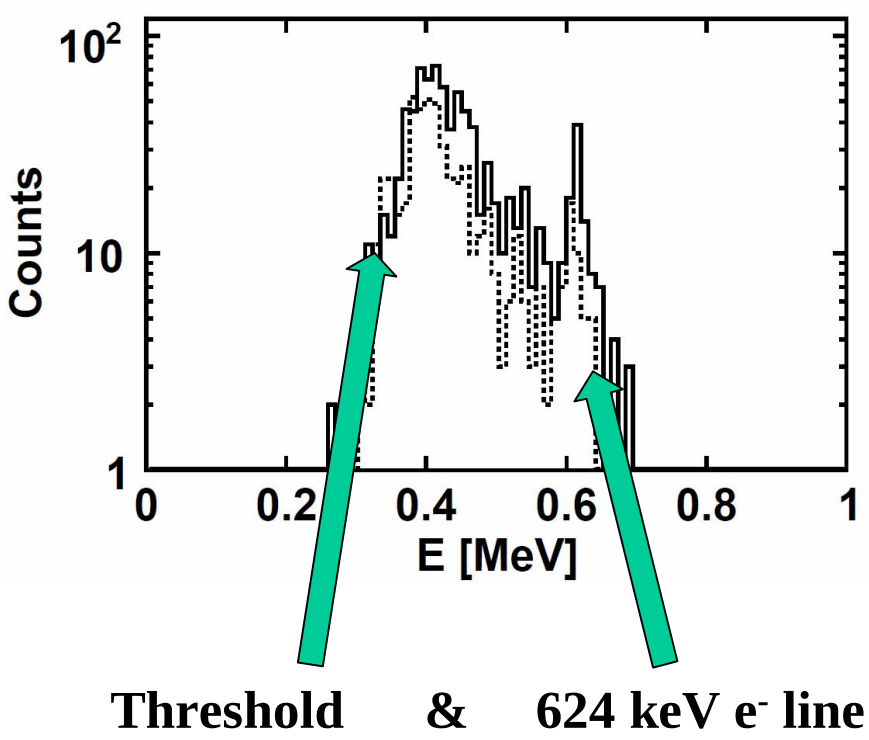
Results with TTT at WU

➔**Energy resolution** (80 MeV range) ➔ FWHM$_{e^-}$(624 keV) ~ 45 keV; FWHM$_{\alpha}$ ~ 50 keV

➔**Threshold$_{e^-}$** (80 MeV range) ➔Front ~324 +- 33 [keV] ; back ~ 304 +- 63 [keV]

These thresholds are a factor of 2-3 better than we could do with the 1.5 mm HiRA Si

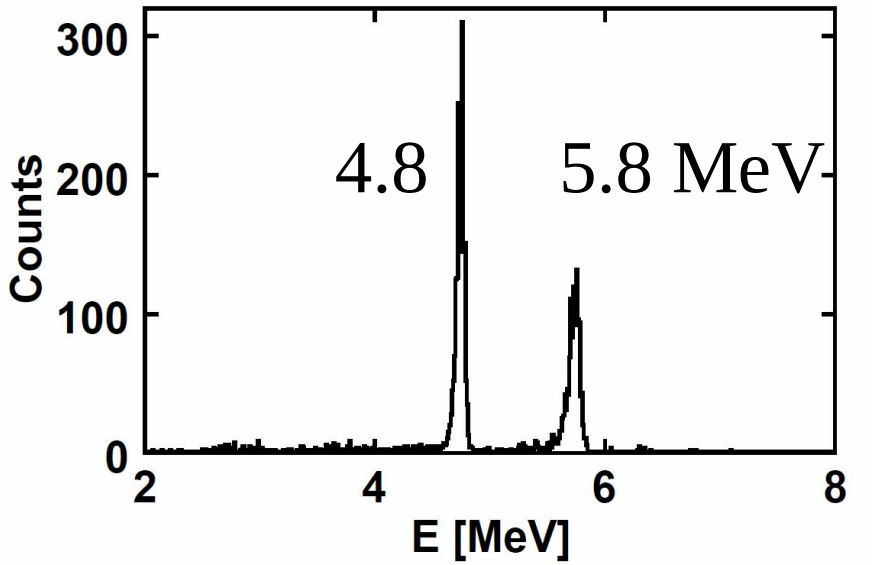
^{207}Bi (β^- & 624 keV conversion e$^-$)



Threshold & 624 keV e$^-$ line

Mixed Alpha source

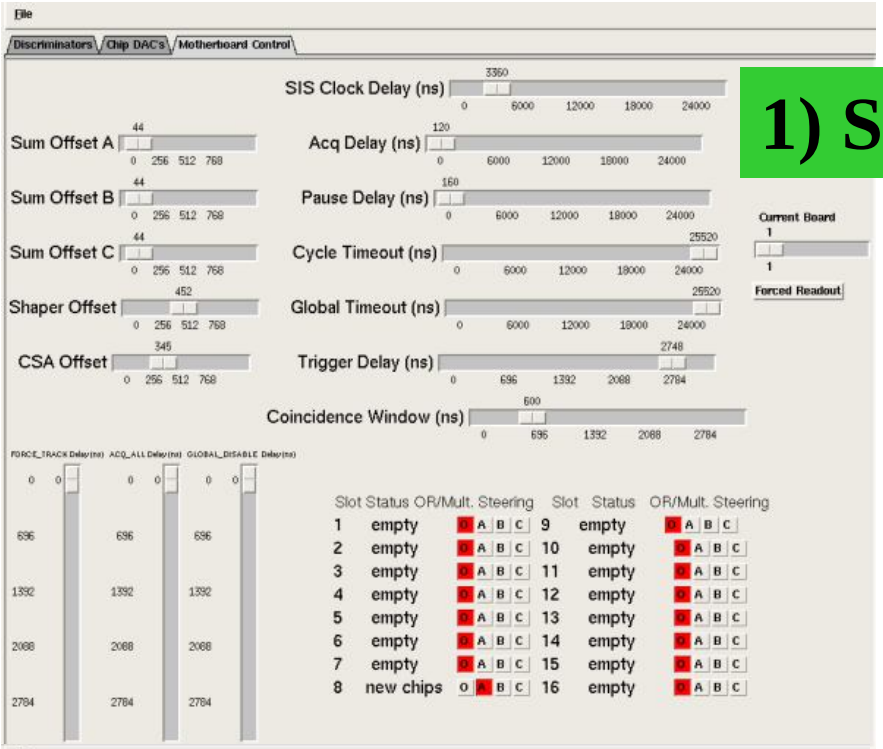
Doublet of doublets ➔ ^{233}U: 4.783 (13%) 4.824 (84%) +
^{244}Cm: 5.764 (23%) 5.805 (77%)



3 pt fit

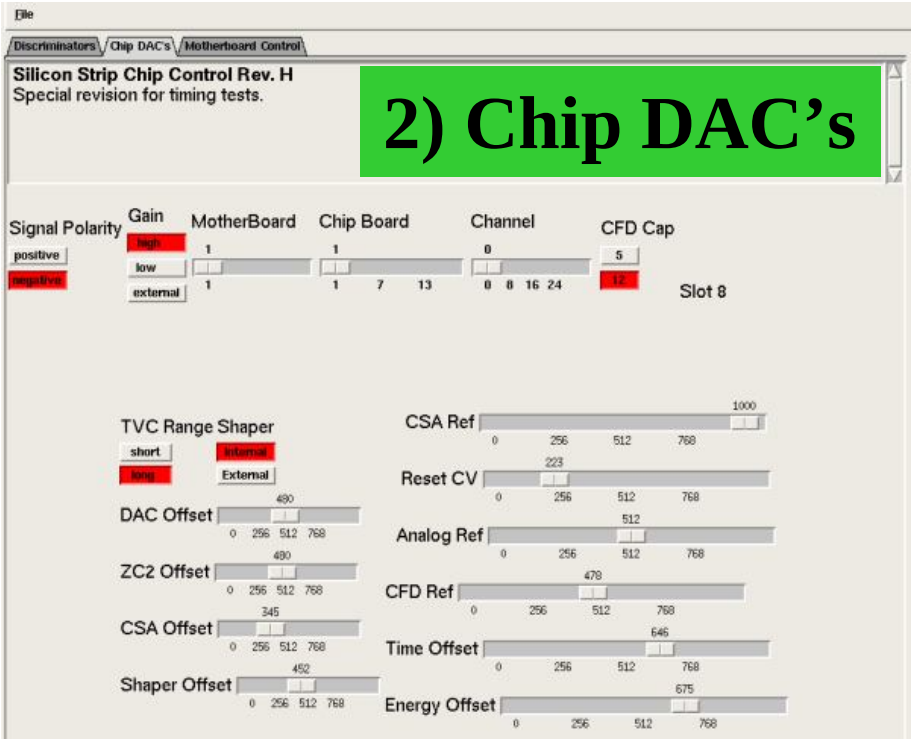
Conversion e$^-$ ensures ~ correctness of zero

On back: we see cross-talk on back at "E < 0"

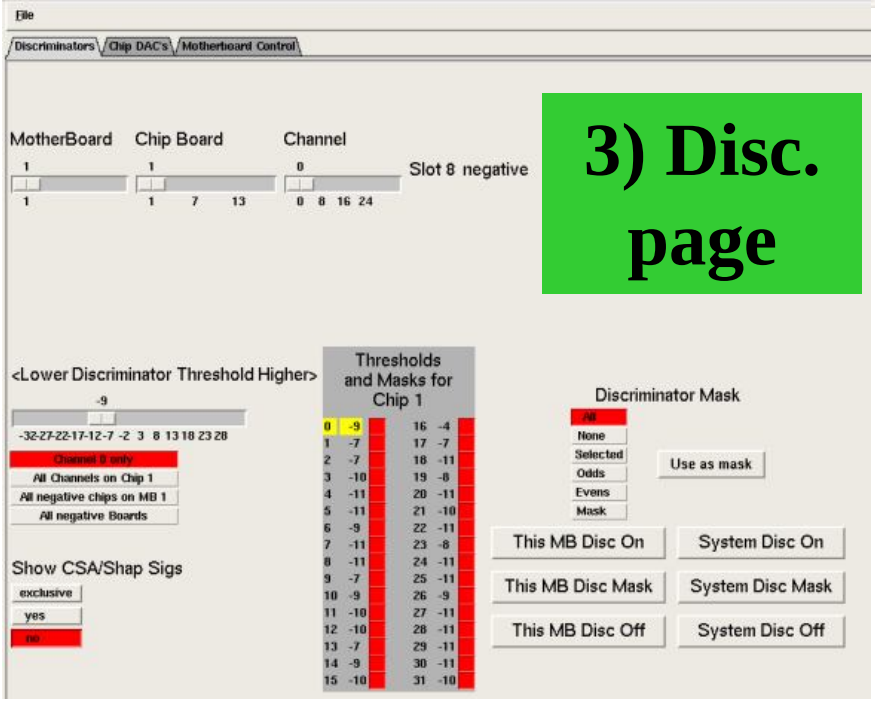


1) System

All new ACQ and control software
For
VME➔USB
(VME controller from Wiener/Jtek)



2) Chip DAC's



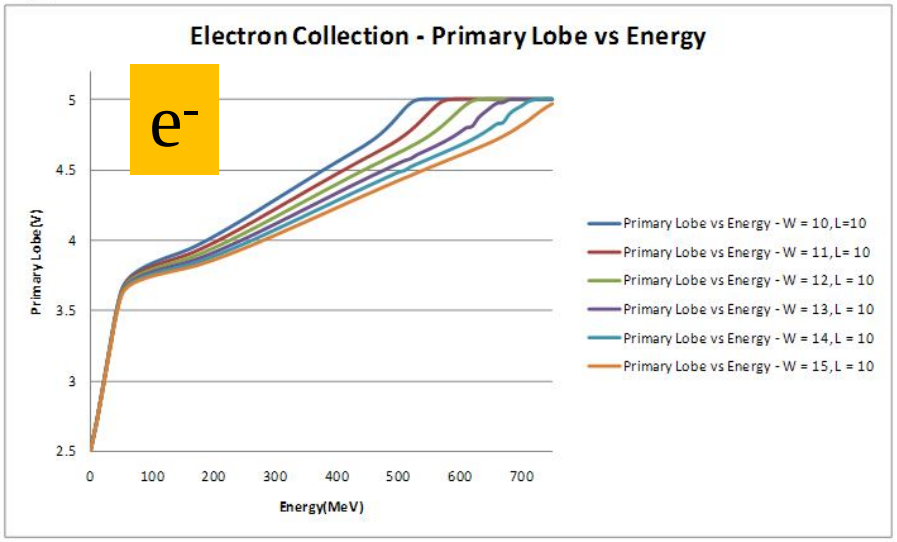
3) Disc. page

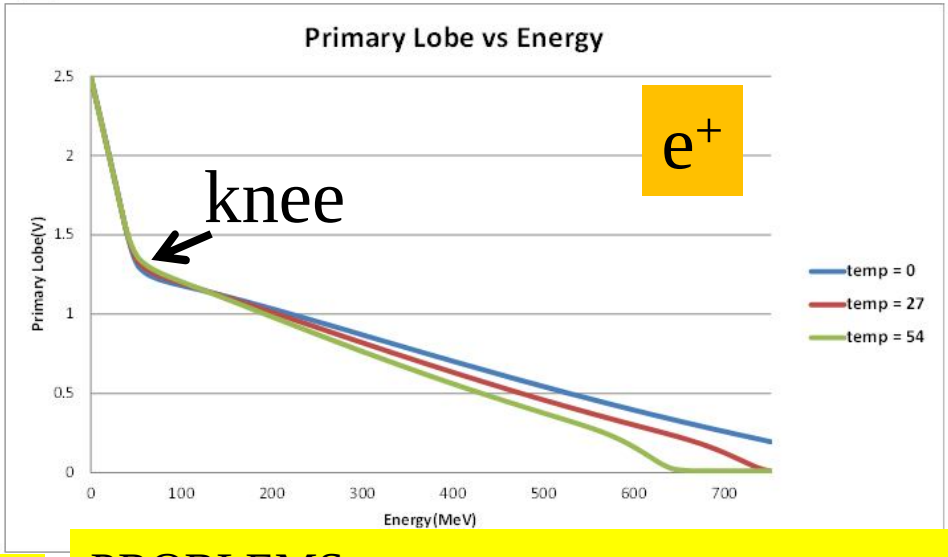
The 3 Tc-Tcl pages for Chip set-up and control.

Full documentation is now available.

ASIC plans

1. Extended-range version of HINP (upgrade REV-IV)
   a) Fix logical error and make time output independent of temp.
   b) Extended range **option** with **Knee** – see below
   c) Move ADC onto CB. (This reduces readout time and eliminates need for VME QDC.)
2. Integrate ASIC with vary large dynamic range EXTERNAL CSA. We would then instrument with TWO ASIC channels on single CSA output.





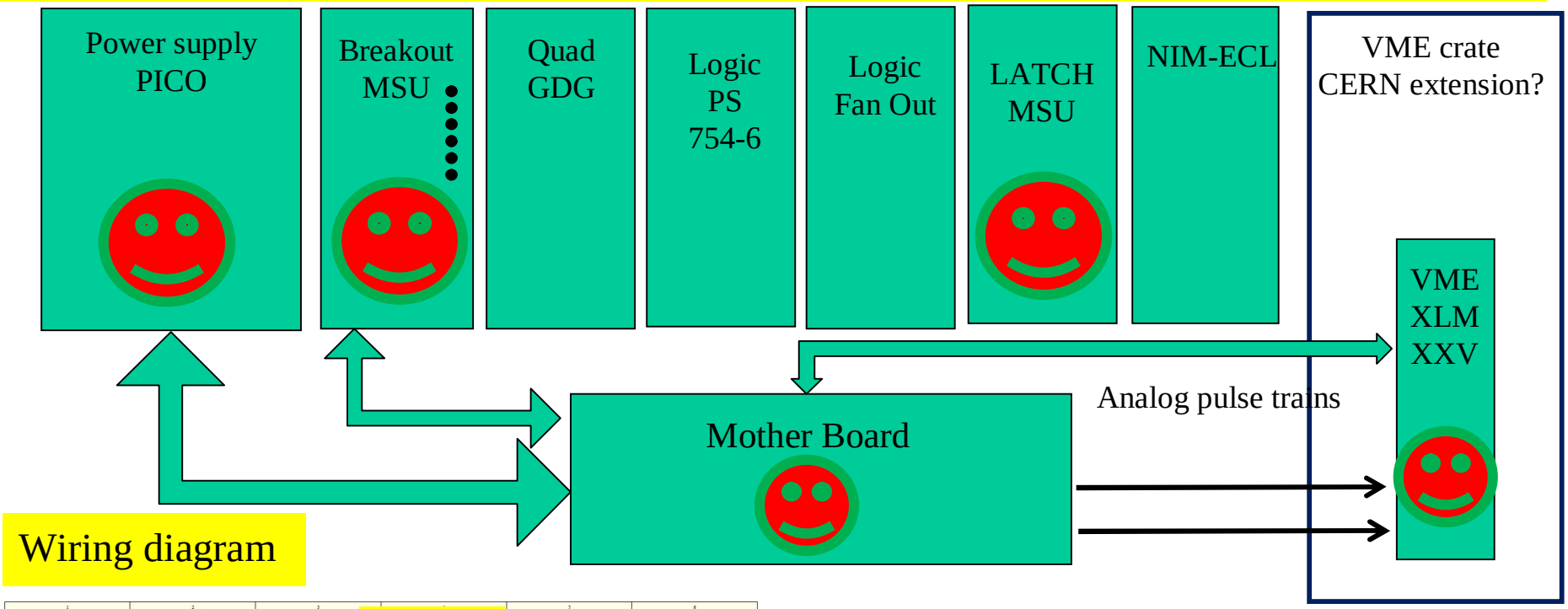
Can **SELECT** an extended range option with "knee". The placement of the knee & the slope are **fixed** by the design (cannot change.)

PROBLEMS:
1.e- non-linear above knee
2.there will be a T sensitivity above the knee

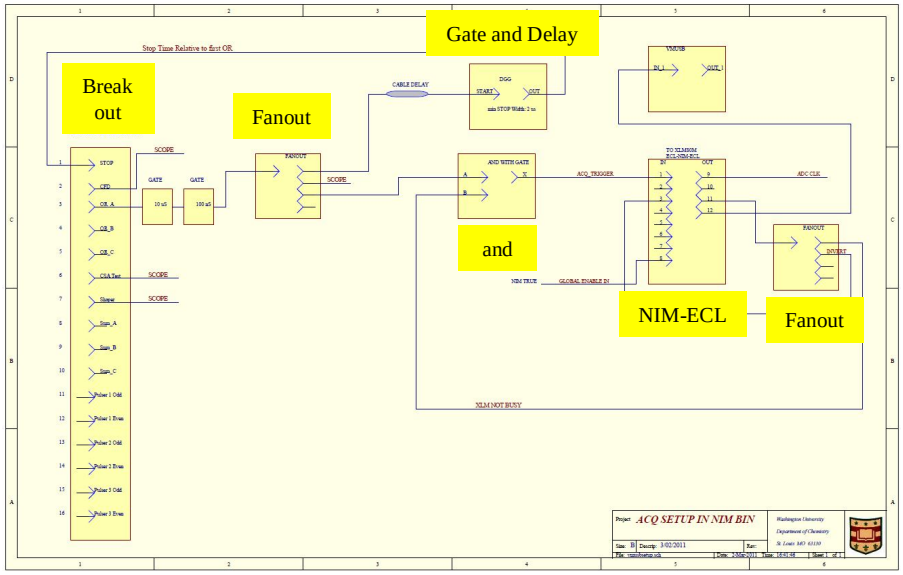
LOGIC for each MB. (Two MB per XLM-XXV)

System at TAMU ready to test drive

NIM **VME**



Wiring diagram



= WU delivered to TAMU

➔ Misc units of value ←

1.BNC PB-5 computer controlled pulser
2.PICO computer controlled switcher
3.Mesetec MHV-4 bias supply

WU Progress and plan

Chip purchase and initial evaluation

1. Purchased remaining 288 chips
2. Testing completed ~ 80 % tested perfect ➔ will get 225 chips > 3500 ch (many for NSCL and ORNL)

Conversion to VME-USB

1. NEW ASIC Control and ACQ software, all tested and working well.
2. Full documentation available .

TAMU system generation

All components delivered – ready for beam testing.

WU-SIUE work

Finish simulations of extended-range chip and begin layout

The latter will take six months!

WU-RIKEN work

Figure out how to incorporate RIKEN very -large range CSA

Thanks for your attention

EXTRAS

Tasks - Homework

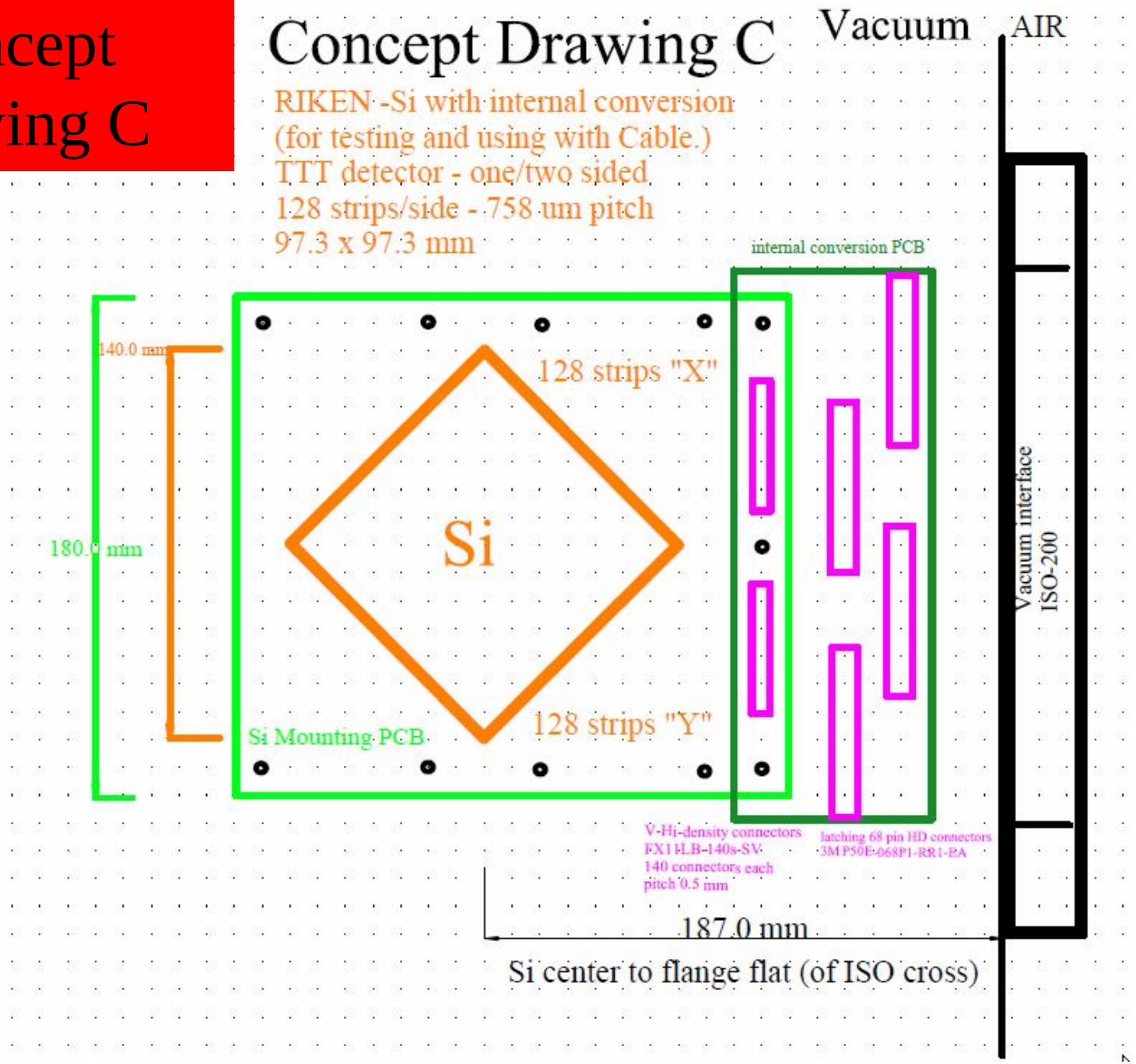
1. Reaction Simulations : **RIKEN/TAMU**
   What is channel requirement? Is 750 um pitch OK?
   When is 5th plane required?
2. Chamber design : **RIKEN/TAMU** ➔ **Must have similar hardware at RIKEN,TAMU,WU**
3. TTT Si PCB :**WU+MICRON** **(MICRON but 2 sided, i.e. twice signal for same Eloss)** ➔ **In progress**
4. GLAST Si PCB : **RIKEN** **(high quality Si, but only one sided)** ➔ **Need spice model for Si**
5. Bonding : **TAMU** **a)** FNAL Lenny Spiegel (lenny@FNAL.gov) or **b)** NSCL John Yurkon
6. Design I, I', II and III development : **RIKEN**

   Two interesting ideas were presented.
   a) A VERY large dynamic range external discrete CSA ➔ VLDR-CSA. **RIKEN**
   b) A compressional internal CSA. **WU+SIUE**

   If both worked, could choose which is better for a given experiment
7. Design of extended-range HINP with following options: **SIUE** ➔ **In progress**
   a) Two-gain (50/175 and 150/400MeV: LINEAR/knee)
   b) Independent selection of above for Even/Odd channels

   With all of these features, one generates options similar to II and III but without the need of a VLDR-CSA.
8. With a VLDR-CSA + Comp amp and HINP-IV (with features a, b, and c) one has the menu:
   a) Run with internal CSA's with knees
   b) Run with external splitter ➔ 2 HINP channels/strip (eg. Even ch➔ high gain, odd ch ➔ low gain.)
   c) Run with option II (external VLDR CSA+ splitter) ➔ 2 HINP channels (shaper+disc)/strip
   d) Run with option III (external VLDR CSA+compression) ➔ 1 HINP (shaper+disc)/strip
9. Creation of TAMU system and duplicate at WU ➔ **In progress**

Concept Drawing C



MICRON quote for our Concept design B

MICRON SEMICONDUCTOR LIMITED

1-3 Royal Buildings
Marlborough Road
LANCING
Sussex,
BN15 8SJ
UK

Telephone: 01903 755252
Fax: 01903 754155
E-mail: direct@micronsemiconductor.co.uk
www.micronsemiconductor.co.uk
VAT: GB 376 8710-14
Reg. №: 1694255 England

Cyclotron Institute
Texas A&M University
3366 TAMU
College Station
TX 77843-3366
United States of America

14th June 2010

QUOTATION NO: 6421
VAT No: GB 376 8710-14

For the attention of Dr Livius Trache (979 845 1411 ext 237)
Email: l-trache@tamu.edu
Subject: RIKEN Experiment

Detector: DSSD TTT2 – 300 Type 2M
Project: SAMURAI
Harsh Radiation Environment 105 p/cm2/sec
300MeV/ Nuclear/ Heavy Ions 370 MeV/ Nuclear
Element range: Oxygen to Tin
Requirement: Detection of Ions and Protons

Detector Options

1) TTT2 – 300 Type 2M N – Type Silicon (standard) (used on MUST 2/ PAX)
2) TTT2 – 300 Type 2M P-Type Silicon (New) (P Type silicon is considered to be more radiation resistant for protons, no information on Ions – used at GSI)
3) TTT4 – 300 Strip pitch same but interstrip oxide reduced to 30 micron and detector design for thinner window

Package Custom Design

Design will be supplied by Dr. Susanne Walsh (design@micronsemiconductor.co.uk). Concept drawing B (interface to be finalised by Washington University who will be developing the interface electronics).
Detector orientation 45 degrees.
TTT DSSD 128 strips per side 758 micron pitch.
Package 180mm x 200mm
Connector: Hi-density FX11 LB – 140s-SV
(140 channels/ pitch 0.5 mm)

Detector
Design TTT2 (DS) – 300 Type 2M (N-Type)
DSSD Double Sided Silicon Detector
See Catalogue page 60 / 61 for pictures and details

DC detector: Structure Ion implanted multiguard with Field Plate

MICRON SEMICONDUCTOR LIMITED

1-3 Royal Buildings
Marlborough Road
LANCING
Sussex,
BN15 8SJ
UK

Telephone: 01903 755252
Fax: 01903 754155
E-mail: direct@micronsemiconductor.co.uk
www.micronsemiconductor.co.uk
VAT: GB 376 8710-14
Reg. №: 1694255 England

Standard detector N Type Silicon
Active area: 97.30 mm x 97.30mm
Window: Tpe 2M < 1 micron
No. of strips: 256 (128 per side)
Strip pitch: 758 micron
Strip width: 702 micron
Strip length: 96968 micron
Thickness: 300 micron
Full Depletion (FD) 40V typ, 70 V max
Operating voltage FD to FD + 30V
Total Current (FD + 30V) (20C) 2uA typical 4uA max
Interstrip resistance (ohmic) 100K min, 10M typical
Minimum Acceptance level: All channels operational
Quality Standard: 2 channels per side permitting with excess currents to the mean value across the detector

Financial
Development of Detector Board for Custom TTT2 detectors to sketch Concept B from Texas A & M
Design / CAD/ Physicist Interface/ Engineering to produce 6 working defect free boards for assembly of N Tpe and P Type detectors
Interface to 2 x FX11 LB – 140 – SV on each PCB
Quantity 6

$12,000

Note: Detectors cannot be totally checked prior to assembly. Additional assemblies will be needed to deliver a detector to specification.

Supply DSSD Detector with N – Type Silicon TTT2 – 300 on Custom PCB using N Type Silicon	$11,000
Supply DSSD Detector with P – Type Silicon TTT2-300 on Custom PCB using P Type Silicon	$12,000
Total Proposal	$35,000

?

Prices: US Dollars, FOB College Station, Texas. Part payment requested for NRE completion and detectors as delivered.

Delivery: 4 – 5 months subject to Design approvals received from Texas A & M