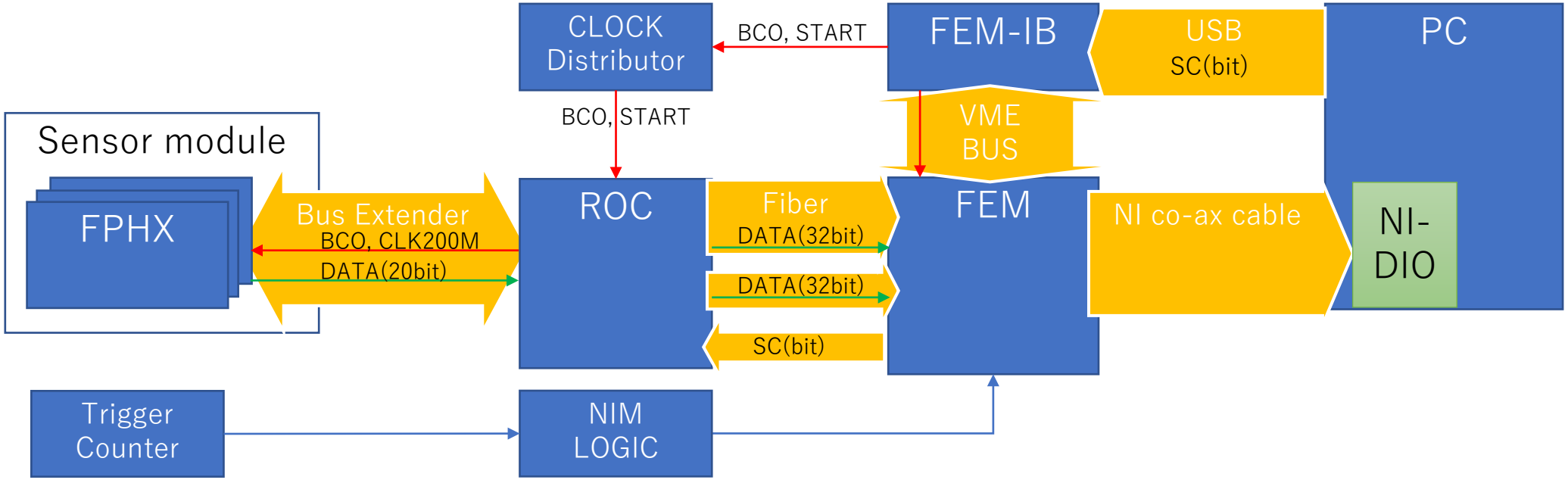
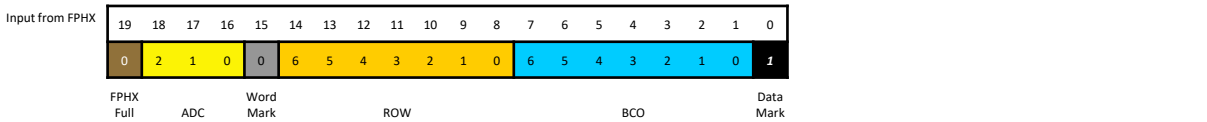
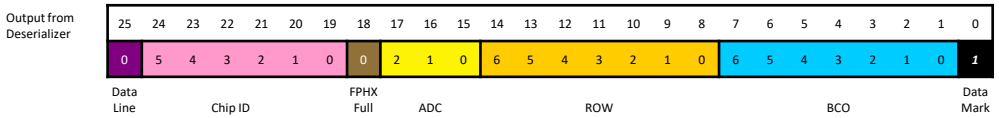
ROC_FEMデータの流れ

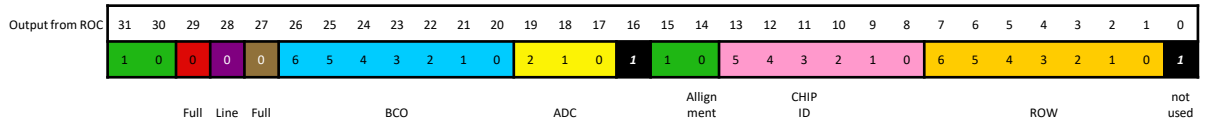
蜂谷　崇
奈良女子大

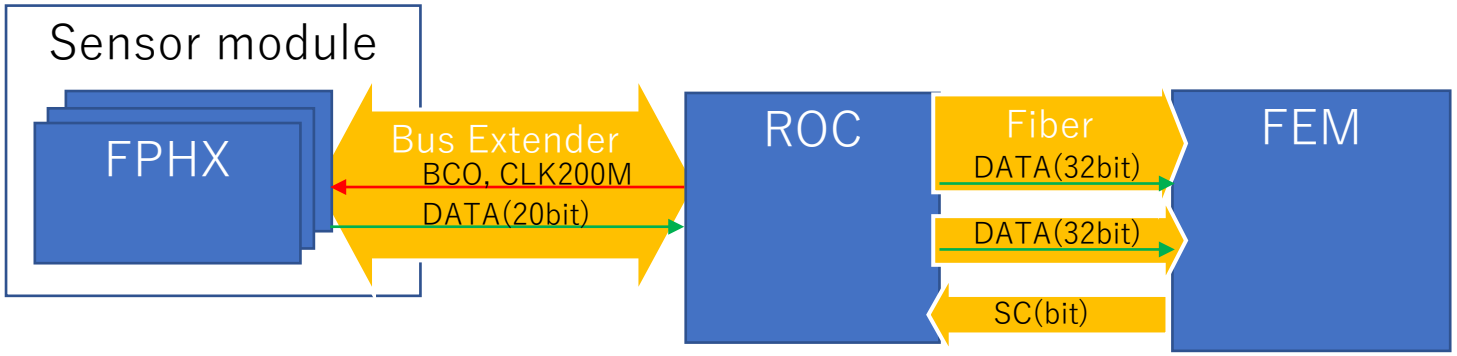
INTT readout system @ Test Bench



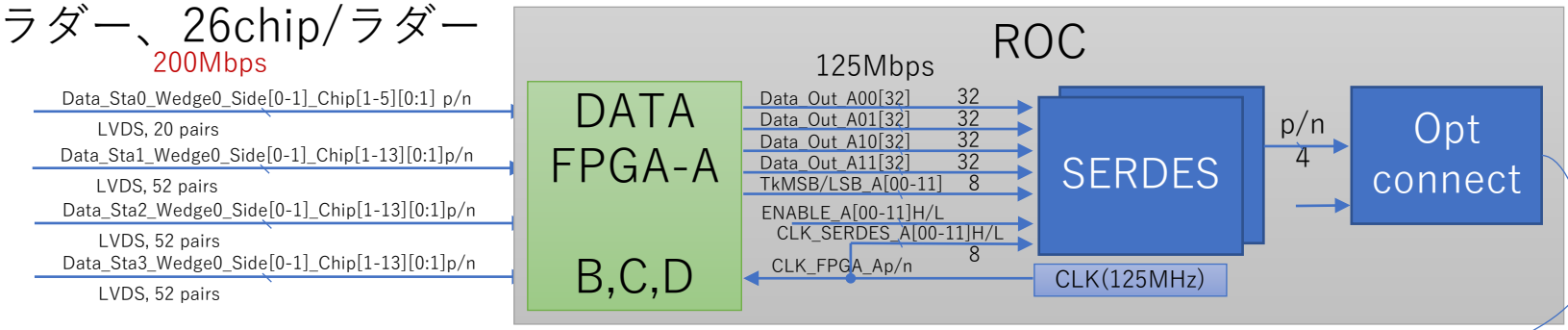








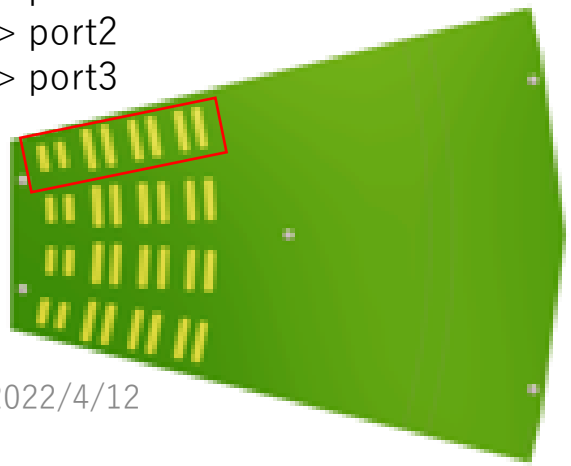
各チップから20bitデータ
4ラダー、26chip/ラダー



各ラダーから32ビットを
2本のファイバーで送る(16x2)

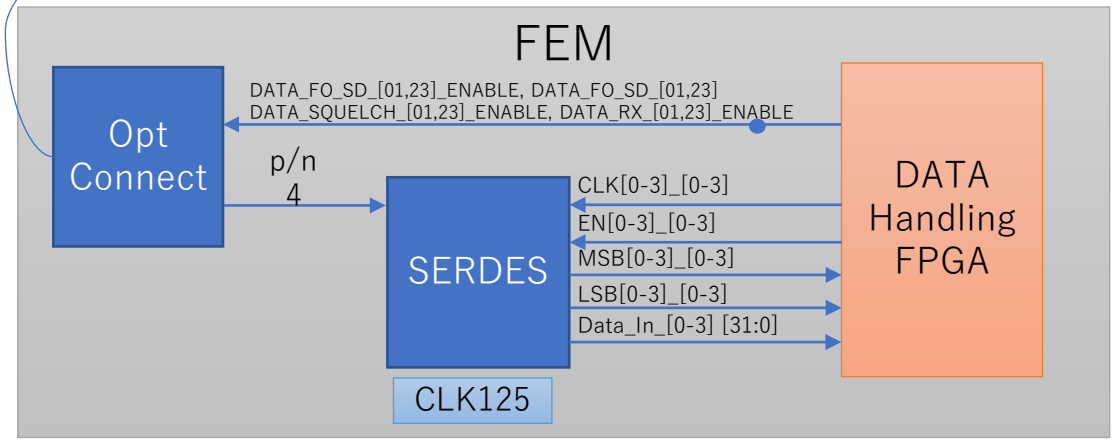
4ラダー分=8本のファイバー

ポートに対応
Sta0 -> port0
Sta1 -> port1
Sta2 -> port2
Sta3 -> port3



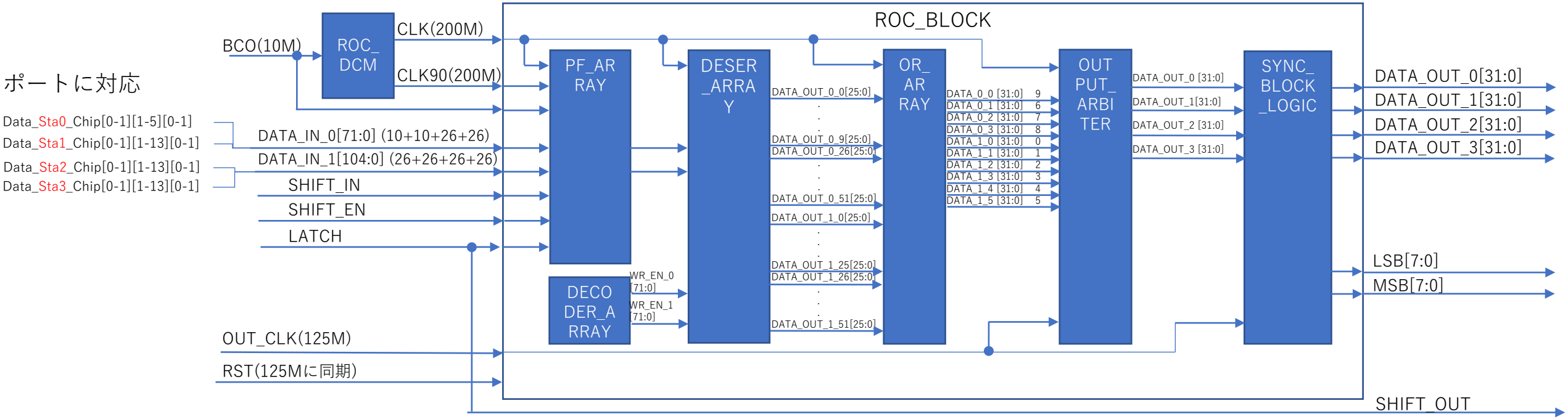
8x

受信後、32ビットx4ラダーの
データに復元

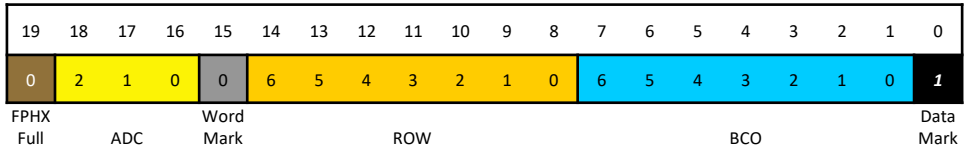


DATA_FPGAの中身

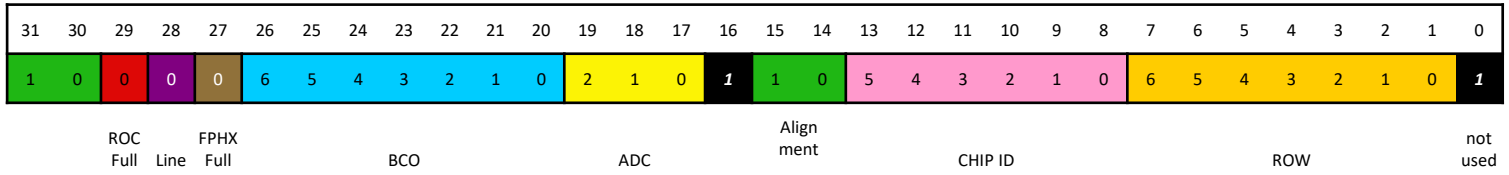
ポートに対応



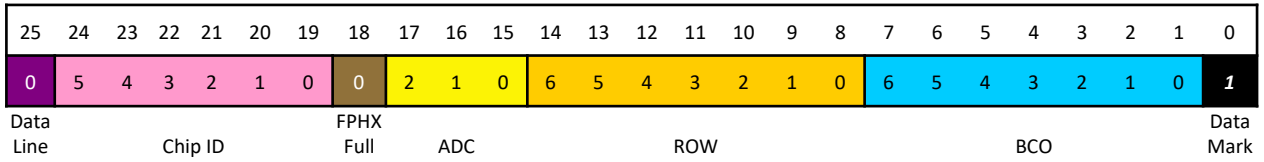
Input from FPHX (20bit)



Output from ROC (32bit) = Deser+Alignment (port)

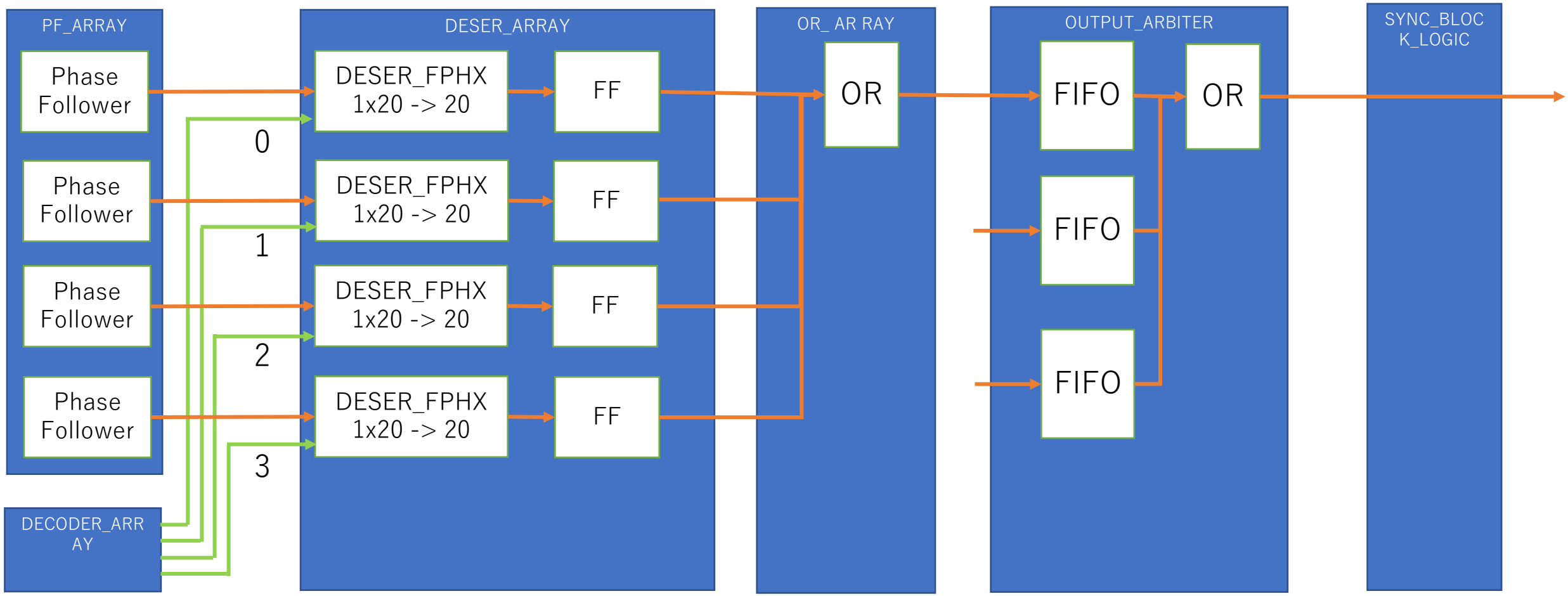


Output from Deserializer (26bit) = FPHX+chipID

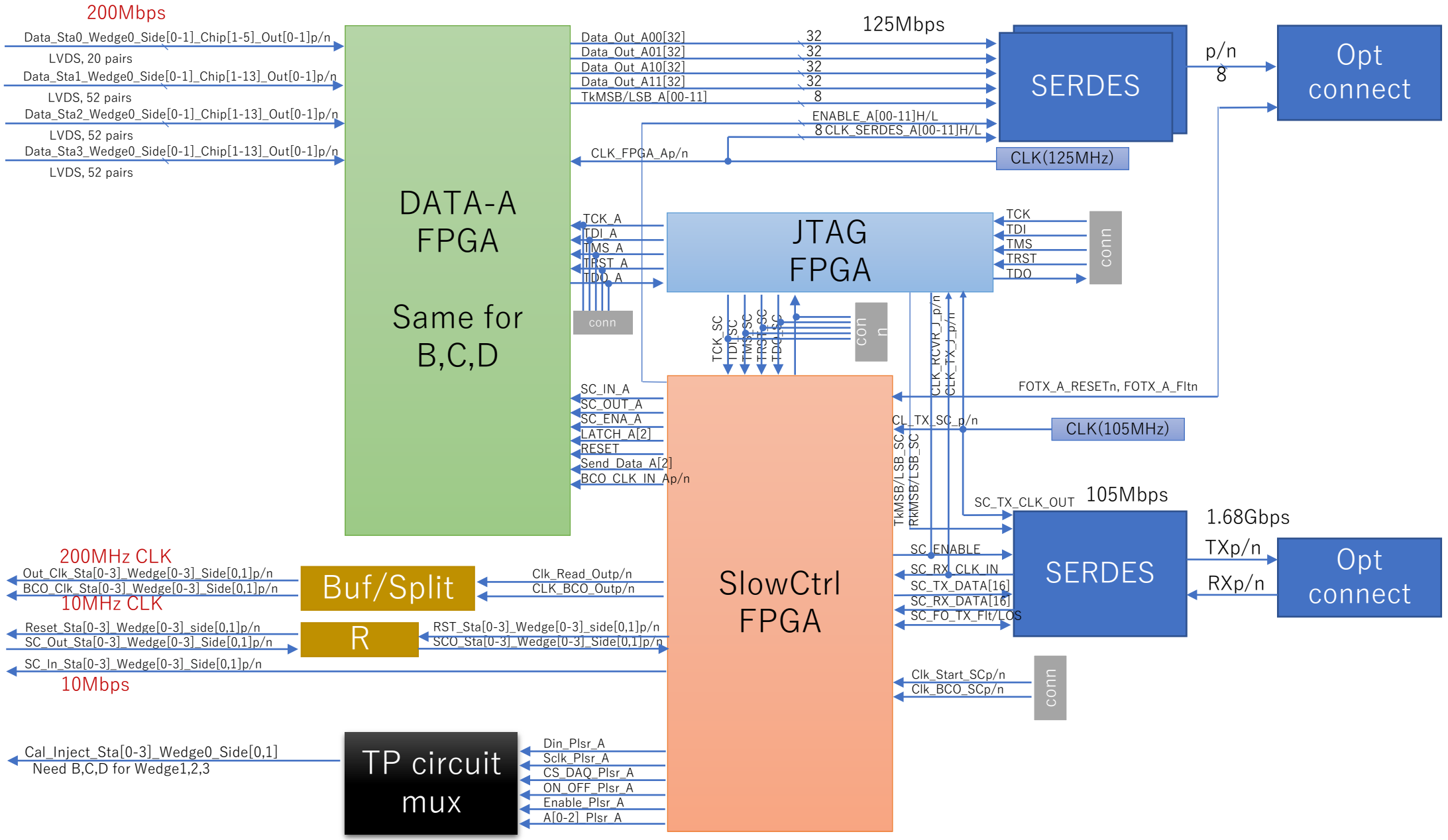


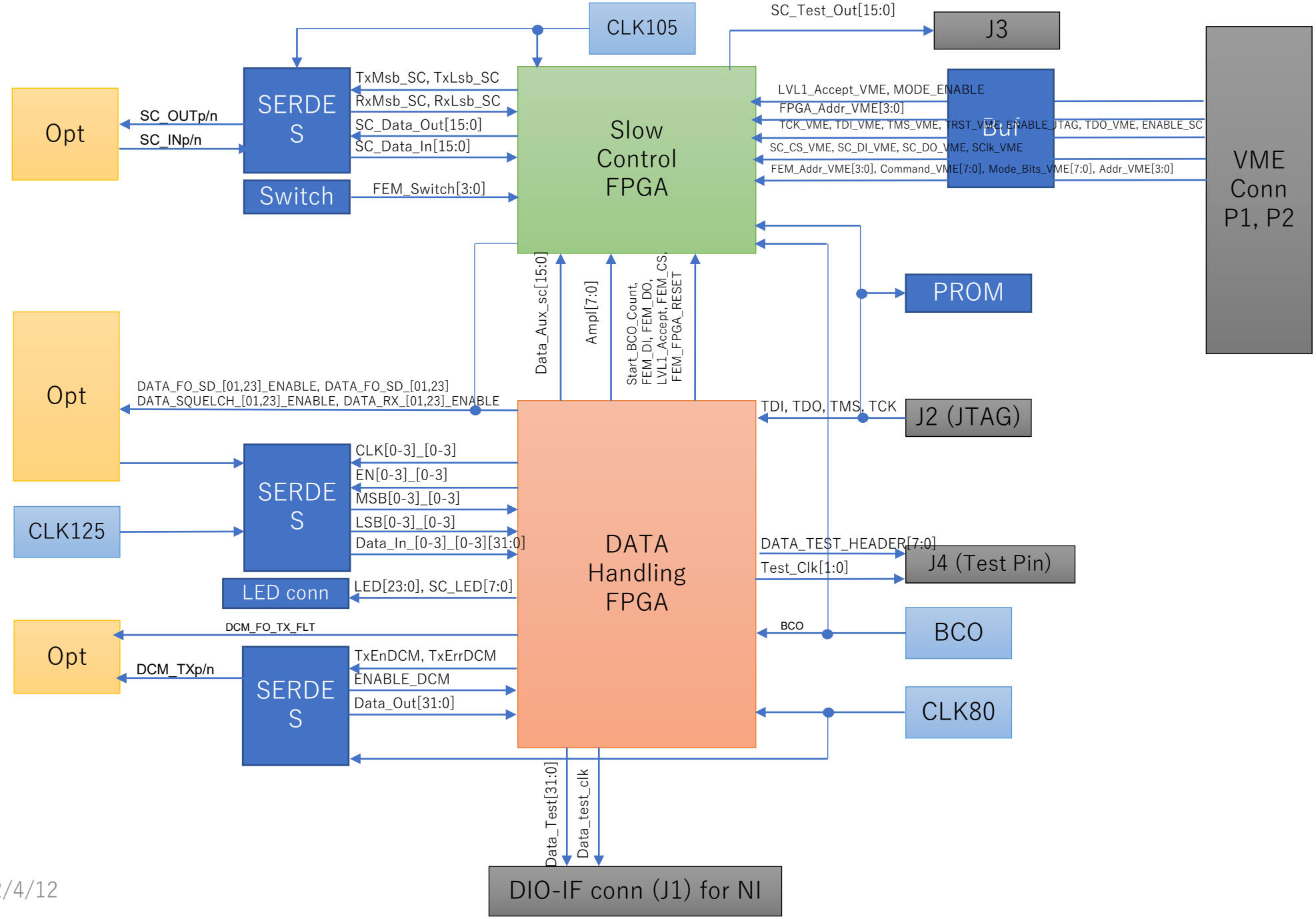
ROC：データ加工と圧縮の流れ

26(ライン＝チップ)　→　3ライン　→　1ライン



ROC												FEM	
		FPGA								ROC	FEM		
ポート番号		Deserialize ->	OR_ARRAY	Output_Arbiter	Sync_block_logic			ROC	SERDES	HFBR-772	HFBRT-782_R1	回路図	
B0	STA0_Side0_p/n[5:1][1:0]	DATA_IN_0_p/n[18:0] 1つ飛び	DATA_0_0[25:0]	DATA_IN_9[31:0]	DATA_OUT_3[31:0]	DATA_OUT_0_1[31:0]	DATA_OUT_0_1[15:0]	Data_Out_B01[15:0]	B01_L_P/N	DIN2+/-	DOUT2+/-	Data_in_0_1[15:0]	DATA_IN_0_1[15:0]
B0	STA0_Side1_p/n[5:1][1:0]	DATA_IN_0_p/n[19:1] 1つ飛び					DATA_OUT_0_1[31:16]	Data_Out_B01[31:16]	B01_H_P/N	DIN3+/-	DOUT3+/-	Data_in_0_1[31:16]	DATA_IN_0_1[31:16]
B1	STA1_Side0_p/n[13:1][1:0]	DATA_IN_0_p/n[70:20] 1つ飛び	DATA_0_1,2,3[25:0]	DATA_IN_6,7,8[31:0]	DATA_OUT_2[31:0]	DATA_OUT_0_0[31:0]	DATA_OUT_0_0[15:0]	Data_Out_B00[15:0]	B00_L_P/N	DIN0+/-	DOUT0+/-	Data_in_0_0[15:0]	DATA_IN_0_0[15:0]
B1	STA1_Side1_p/n[13:1][1:0]	DATA_IN_0_p/n[71:21] 1つ飛び					DATA_OUT_0_0[31:16]	Data_Out_B00[31:16]	B00_H_P/N	DIN1+/-	DOUT1+/-	Data_in_0_0[31:16]	DATA_IN_0_0[31:16]
B2	STA2_Side0_p/n[13:1][1:0]	DATA_IN_1_p/n[50:0] 1つ飛び	DATA_1_0,1,2[25:0]	DATA_IN_0,1,2[31:0]	DATA_OUT_0[31:0]	DATA_OUT_1_0[31:0]	DATA_OUT_1_0[31:16]	Data_Out_B10[15:0]	B10_L_P/N	DIN8+/-	DOUT8+/-	Data_in_1_0[31:16]	DATA_IN_1_0[31:16]
B2	STA2_Side1_p/n[13:1][1:0]	DATA_IN_1_p/n[51:1] 1つ飛び					DATA_OUT_1_0[15:0]	Data_Out_B10[31:16]	B10_H_P/N	DIN9+/-	DOUT9+/-	Data_in_1_0[15:0]	DATA_IN_1_0[15:0]
B3	STA3_Side0_p/n[13:1][1:0]	DATA_IN_1_p/n[102:52] 1つ飛び	DATA_1_3,4,5[25:0]	DATA_IN_3,4,5[31:0]	DATA_OUT_1[31:0]	DATA_OUT_1_1[31:0]	DATA_OUT_1_1[31:16]	Data_Out_B11[15:0]	B11_L_P/N	DIN10+/-	DOUT10+/-	Data_in_1_1[31:16]	DATA_IN_1_1[31:16]
B3	STA3_Side1_p/n[13:1][1:0]	DATA_IN_1_p/n[103:53] 1つ飛び					DATA_OUT_1_1[15:0]	Data_Out_B11[31:16]	B11_H_P/N	DIN11+/-	DOUT11+/-	Data_in_1_1[15:0]	DATA_IN_1_1[15:0]
A/B/C/Dのどれでも同じ（はず）		この変換で、Sideの情報は無くなり、26チップを1グループとして扱う	ここから1グループにしている					A, Cでは、ファイバーの間違いがあり、入れ替えが起こっている。				FEMのファイバーがフリップしているので、ROCで直している。	
												FEMの上下のどちらのコネクタにファイバーを付けているかによって変わる。今の場合は上。	


200Mbps
Data_Sta0_Wedge0_Side[0-1]_Chip[1-5]_Out[0-1]p/n
LVDS, 20 pairs
Data_Sta1_Wedge0_Side[0-1]_Chip[1-13]_Out[0-1]p/n
LVDS, 52 pairs
Data_Sta2_Wedge0_Side[0-1]_Chip[1-13]_Out[0-1]p/n
LVDS, 52 pairs
Data_Sta3_Wedge0_Side[0-1]_Chip[1-13]_Out[0-1]p/n
LVDS, 52 pairs
DATA-A FPGA
Same for B,C,D
Data_Out_A00[32]
Data_Out_A01[32]
Data_Out_A10[32]
Data_Out_A11[32]
TkMSB/LSB_A[00-11]
32
32
32
32
8
125Mbps
SERDES
p/n
8
Opt connect
ENABLE_A[00-11]H/L
8 CLK_SERDES_A[00-11]H/L
CLK_FPGA_Ap/n
CLK(125MHz)
TCK_A
TDI_A
TMS_A
TRST_A
TDO_A
conn
JTAG FPGA
TCK
TDI
TMS
TRST
TDO
conn
TCK_SC
TDI_SC
TMS_SC
TRST_SC
TDO_SC
conn
CLK_RCVR_J_p/n
CLK_TX_J_p/n
FOTX_A_RESETn, FOTX_A_FItn
SC_IN_A
SC_OUT_A
SC_ENA_A
LATCH_A[2]
RESET
Send_Data_A[2]
BCO_CLK_IN_Ap/n
CL_TX_SC_p/n
CLK(105MHz)
TkMSB/LSB_SC
RkMSB/LSB_SC
SC_TX_CLK_OUT
105Mbps
1.68Gbps
SC_ENABLE
SC_RX_CLK_IN
SC_TX_DATA[16]
SC_RX_DATA[16]
SC_FO_TX_Flt/LOS
SERDES
TXp/n
RXp/n
Opt connect
SlowCtrl FPGA
200MHz CLK
Out_Clk_Sta[0-3]_Wedge[0-3]_Side[0,1]p/n
BCO_Clk_Sta[0-3]_Wedge[0-3]_Side[0,1]p/n
Buf/Split
Clk_Read_Outp/n
CLK_BCO_Outp/n
10MHz CLK
Reset_Sta[0-3]_Wedge[0-3]_side[0,1]p/n
SC_Out_Sta[0-3]_Wedge[0-3]_Side[0,1]p/n
R
RST_Sta[0-3]_Wedge[0-3]_side[0,1]p/n
SCO_Sta[0-3]_Wedge[0-3]_Side[0,1]p/n
SC_In_Sta[0-3]_Wedge[0-3]_Side[0,1]p/n
10Mbps
Clk_Start_SCp/n
Clk_BCO_SCp/n
conn
Cal_Inject_Sta[0-3]_Wedge0_Side[0,1]
Need B,C,D for Wedge1,2,3
TP circuit mux
Din_Plsr_A
Sclk_Plsr_A
CS_DAQ_Plsr_A
ON_OFF_Plsr_A
Enable_Plsr_A
A[0-2]_Plsr_A


CLK105
SC_Test_Out[15:0]
J3
Opt
SC_OUTp/n
SC_INp/n
SERDES
TxMsb_SC, TxLsb_SC
RxMsb_SC, RxLsb_SC
SC_Data_Out[15:0]
SC_Data_In[15:0]
Switch
FEM_Switch[3:0]
Slow Control FPGA
LVL1_Accept_VME, MODE_ENABLE
FPGA_Addr_VME[3:0]
TCK_VME, TDI_VME, TMS_VME, TRST_VME, ENABLE_JTAG, TDO_VME, ENABLE_SC
SC_CS_VME, SC_DI_VME, SC_DO_VME, SClk_VME
FEM_Addr_VME[3:0], Command_VME[7:0], Mode_Bits_VME[7:0], Addr_VME[3:0]
Buf
VME Conn P1, P2
PROM
Data_Aux_sc[15:0]
Ampl[7:0]
Start_BCO_Count, FEM_DI, FEM_DO, LVL1_Accept, FEM_CS, FEM_FPGA_RESET
Opt
DATA_FO_SD_[01,23]_ENABLE, DATA_FO_SD_[01,23]
DATA_SQUELCH_[01,23]_ENABLE, DATA_RX_[01,23]_ENABLE
TDI, TDO, TMS, TCK
J2 (JTAG)
CLK125
SERDES
CLK[0-3]_[0-3]
EN[0-3]_[0-3]
MSB[0-3]_[0-3]
LSB[0-3]_[0-3]
Data_In_[0-3]_[0-3][31:0]
DATA Handling FPGA
DATA_TEST_HEADER[7:0]
Test_Clk[1:0]
J4 (Test Pin)
LED conn
LED[23:0], SC_LED[7:0]
BCO
DCM_FO_TX_FLT
Opt
DCM_TXp/n
SERDES
TxEnDCM, TxErrDCM
ENABLE_DCM
Data_Out[31:0]
CLK80
Data_Test[31:0]
Data_test_clk
DIO-IF conn (J1) for NI

ROC内の接続バグ修正

B/D

```
--DATA_OUT need one extra clock delay to be in time with LSBs:
DATA_OUT_0_0 <= DATA_OUT_0_0_tmp;
DATA_OUT_0_1 <= DATA_OUT_0_1_tmp;
--Station 3 needs to have 16 bit chunks inverted:
DATA_OUT_1_0(31 downto 16) <= DATA_OUT_1_0_tmp(15 downto 0);
DATA_OUT_1_0(15 downto 0) <= DATA_OUT_1_0_tmp(31 downto 16);
--DATA_OUT_1_0_int <= DATA_OUT_1_0_tmp;
--Test inverting 16 bit chunks for station 4:
DATA_OUT_1_1(31 downto 16) <= DATA_OUT_1_1_tmp(15 downto 0);
DATA_OUT_1_1(15 downto 0) <= DATA_OUT_1_1_tmp(31 downto 16);
--DATA_OUT_1_1_int <= DATA_OUT_1_1_tmp;
```

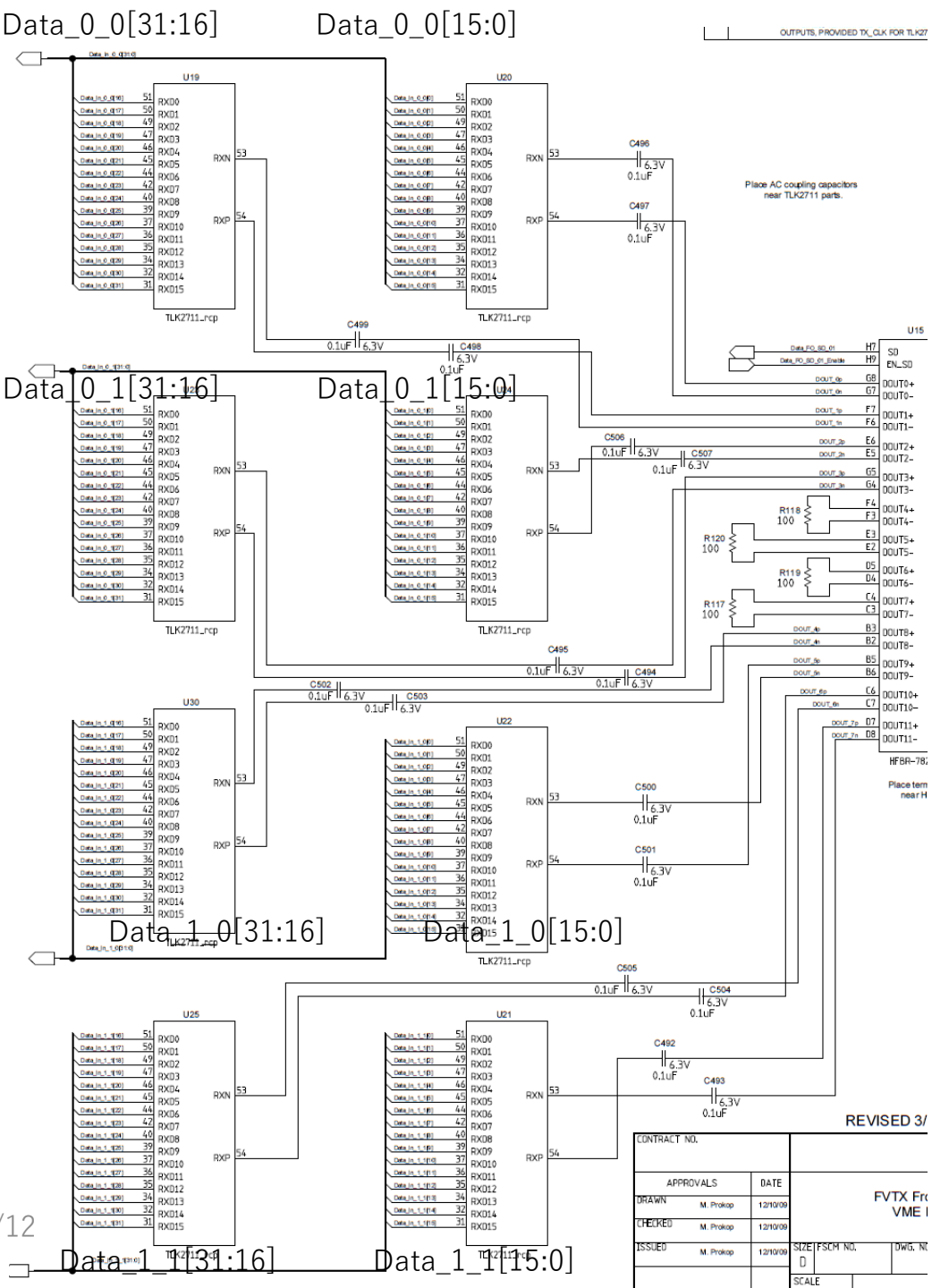
A

```
--13-Jul-11: found that fibers on ROC FPGA A are all mixed up.  Unmix them here to
--match what the FEM has:
--A_00 --> fibers 11 and 1
--A_01 --> fibers 2 and 0
--A_10 --> fibers 9 and 10
--A_11 --> fibers 3 and 8
DATA_OUT_0_0_tmp <= DATA_OUT_0_0_int;
DATA_OUT_0_1_tmp <= DATA_OUT_0_1_int;
DATA_OUT_1_0_tmp <= DATA_OUT_1_0_int;
DATA_OUT_1_1_tmp <= DATA_OUT_1_1_int;
DATA_OUT_0_0(15 downto 0) <= DATA_OUT_1_1_tmp(15 downto 0);
DATA_OUT_0_0(31 downto 16) <= DATA_OUT_0_0_tmp(31 downto 16);
DATA_OUT_0_1(15 downto 0) <= DATA_OUT_0_1_tmp(15 downto 0);
DATA_OUT_0_1(31 downto 16) <= DATA_OUT_0_0_tmp(15 downto 0);
DATA_OUT_1_0(15 downto 0) <= DATA_OUT_1_0_tmp(15 downto 0);
DATA_OUT_1_0(31 downto 16) <= DATA_OUT_1_1_tmp(31 downto 16);
DATA_OUT_1_1(15 downto 0) <= DATA_OUT_0_1_tmp(31 downto 16);
DATA_OUT_1_1(31 downto 16) <= DATA_OUT_1_0_tmp(31 downto 16);
```

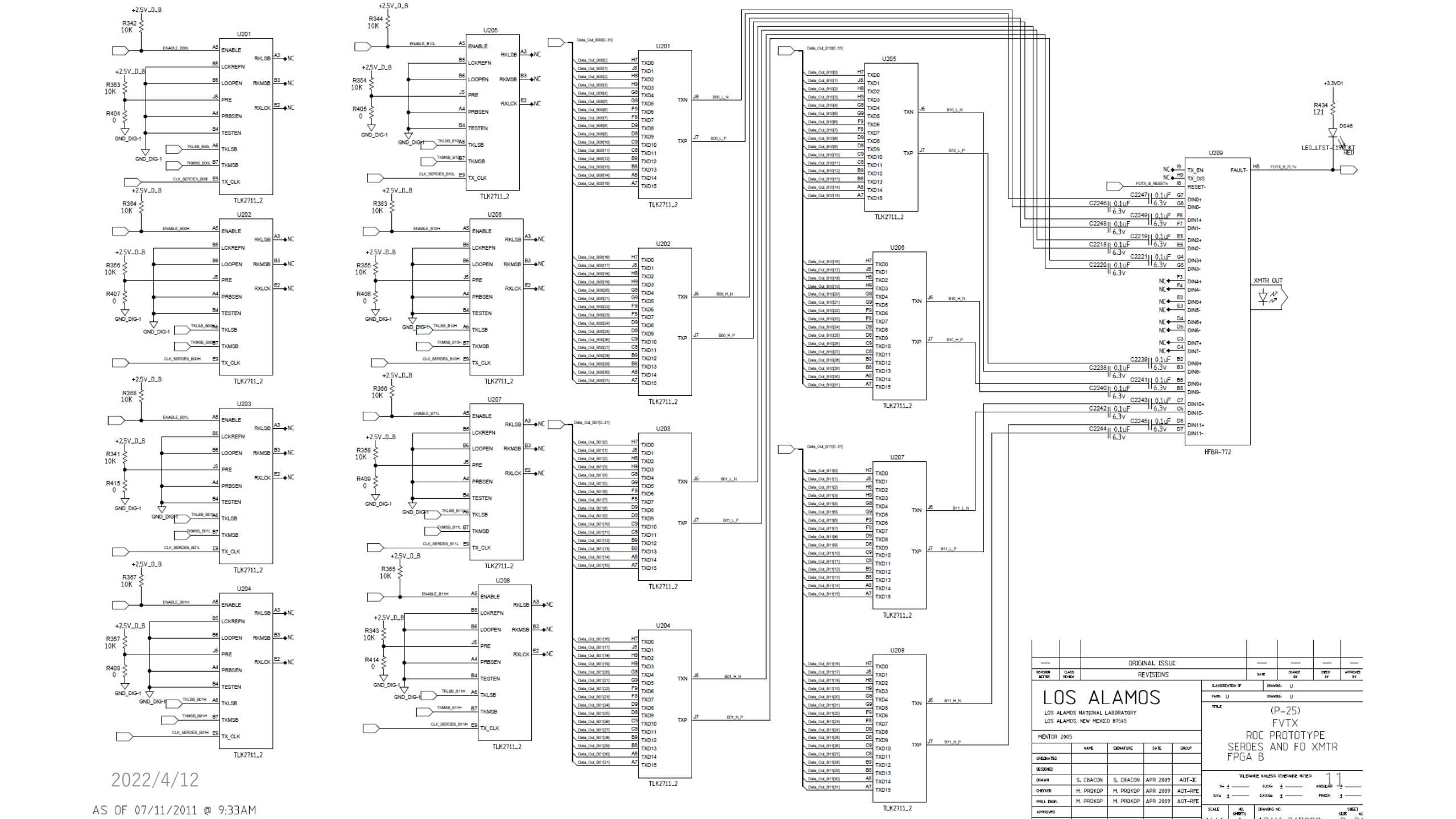
C

```
--13-Jul-11: found that fibers on ROC FPGA A are all mixed up.  Unmix them here to
--match what the FEM has:
--21-Jul-11: found that C fibers are mixed up a little differently from A fibers. Code
--here is now for C fibers.
--C_00 --> fibers 11 and 0; A_00 --> fibers 11 and 1
--C_01 --> fibers 1 and 2;  A_01 --> fibers 2 and 0
--C_10 --> fibers 9 and 10; A_10 --> fibers 9 and 10
--C_11 --> fibers 3 and 8;  A_11 --> fibers 3 and 8
DATA_OUT_0_0_tmp <= DATA_OUT_0_0_int;
DATA_OUT_0_1_tmp <= DATA_OUT_0_1_int;
DATA_OUT_1_0_tmp <= DATA_OUT_1_0_int;
DATA_OUT_1_1_tmp <= DATA_OUT_1_1_int;
DATA_OUT_0_0(15 downto 0) <= DATA_OUT_1_1_tmp(15 downto 0);
DATA_OUT_0_0(31 downto 16) <= DATA_OUT_0_0_tmp(15 downto 0);
DATA_OUT_0_1(15 downto 0) <= DATA_OUT_0_0_tmp(31 downto 16);
DATA_OUT_0_1(31 downto 16) <= DATA_OUT_0_1_tmp(15 downto 0);
DATA_OUT_1_0(15 downto 0) <= DATA_OUT_1_0_tmp(15 downto 0);
DATA_OUT_1_0(31 downto 16) <= DATA_OUT_1_1_tmp(31 downto 16);
DATA_OUT_1_1(15 downto 0) <= DATA_OUT_0_1_tmp(31 downto 16);
DATA_OUT_1_1(31 downto 16) <= DATA_OUT_1_0_tmp(31 downto 16);
```

FEM



これが正しいはず


U201
U202
U203
U204
U205
U206
U207
U208
U209
TLK2711_2
HFBR-772
XMTR OUT
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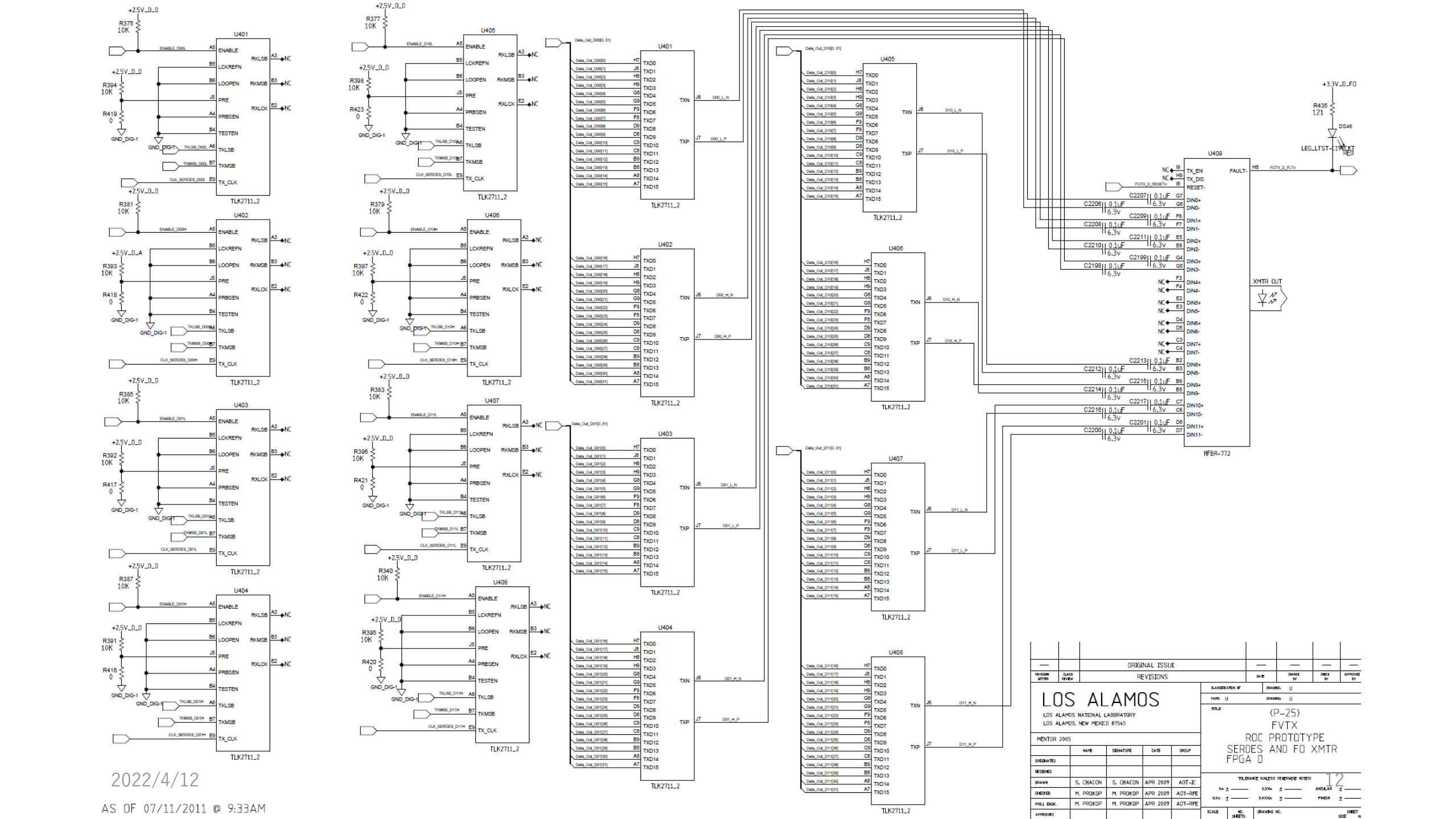
LOS ALAMOS NATIONAL LABORATORY
LOS ALAMOS, NEW MEXICO 87545
MENTOR 2005
ORIGINAL ISSUE
REVISIONS
(P-25)
FVTX
ROC PROTOTYPE
SERDES AND FO XMTR
FPGA B
2022/4/12
AS OF 07/11/2011 @ 9:33AM



2022/4/12

AS OF 07/11/2011 @ 9:33AM

REVISION LETTER	CLASS REVIEW	REVISIONS	DATE	DRAWN BY	CHKD BY	APPROVED BY
—		ORIGINAL ISSUE	—	—	—	—

LOS ALAMOS

LOS ALAMOS NATIONAL LABORATORY
LOS ALAMOS, NEW MEXICO 87545

MENTOR 2005

	NAME	SIGNATURE	DATE	GROUP
ORIGINATED				
DESIGNED				
DRAWN	S. CHACON	S. CHACON	APR 2009	AOT-JC
CHECKED	M. PROKOP	M. PROKOP	APR 2009	AOT-RFE
PHYS ENGR.	M. PROKOP	M. PROKOP	APR 2009	AOT-RFE
APPROVED				

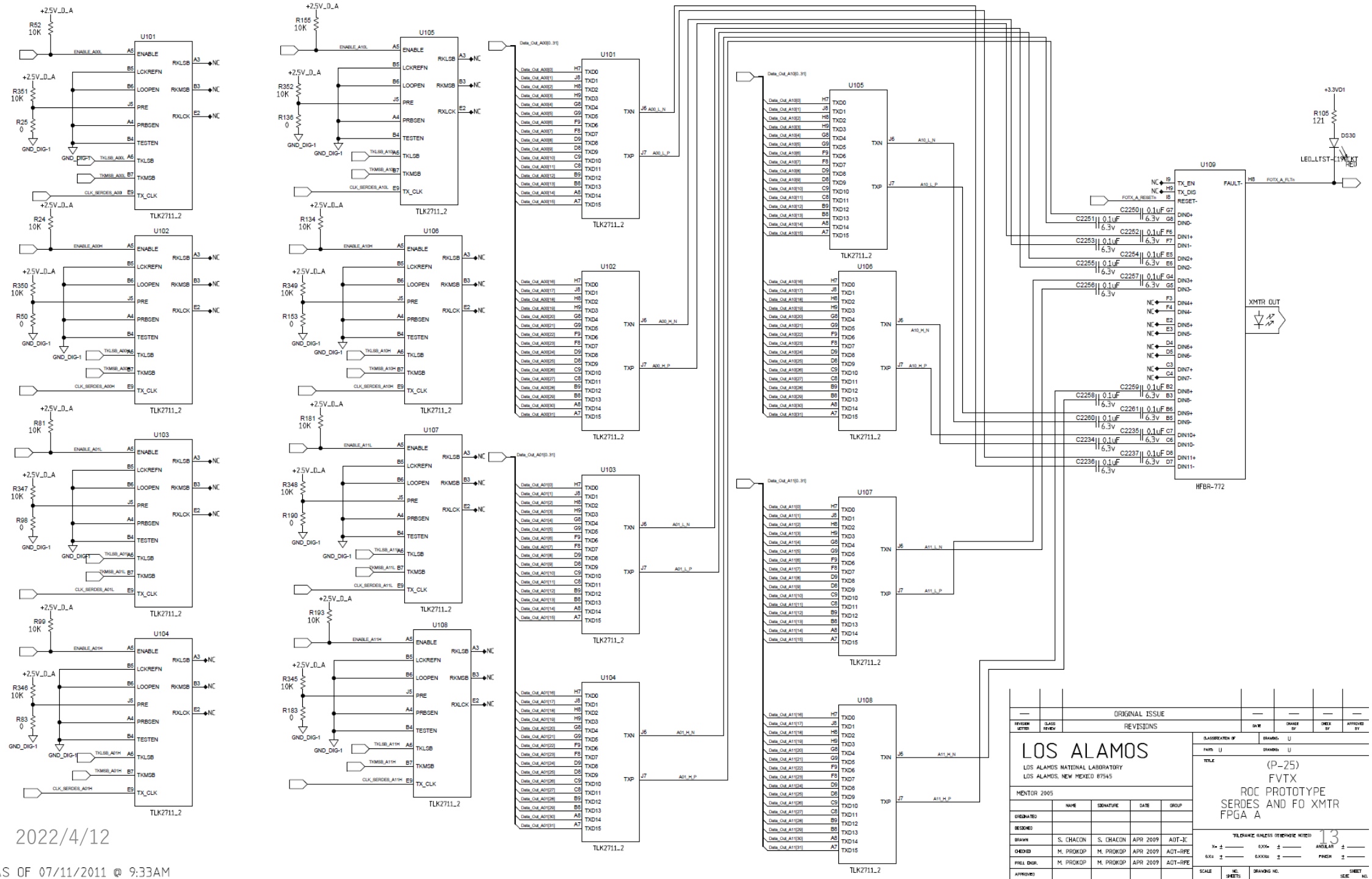
CLASSIFICATION OF: U
FAITH: U
DRAWING: U

TITLE
(P-25)
FVTX
ROC PROTOTYPE
SERDES AND FO XMTR
FPGA D

TOLERANCE UNLESS OTHERWISE NOTED
X= ± 0.XX= ± ANGULAR ±
0.XX= ± 0.XXX= ± FINISH ±

SCALE | NO. SHEETS | DRAWING NO. | SHEET SIZE N

12


U101
U102
U103
U104
U105
U106
U107
U108
U109
TLK2711_2
HFBR-772
R52 10K
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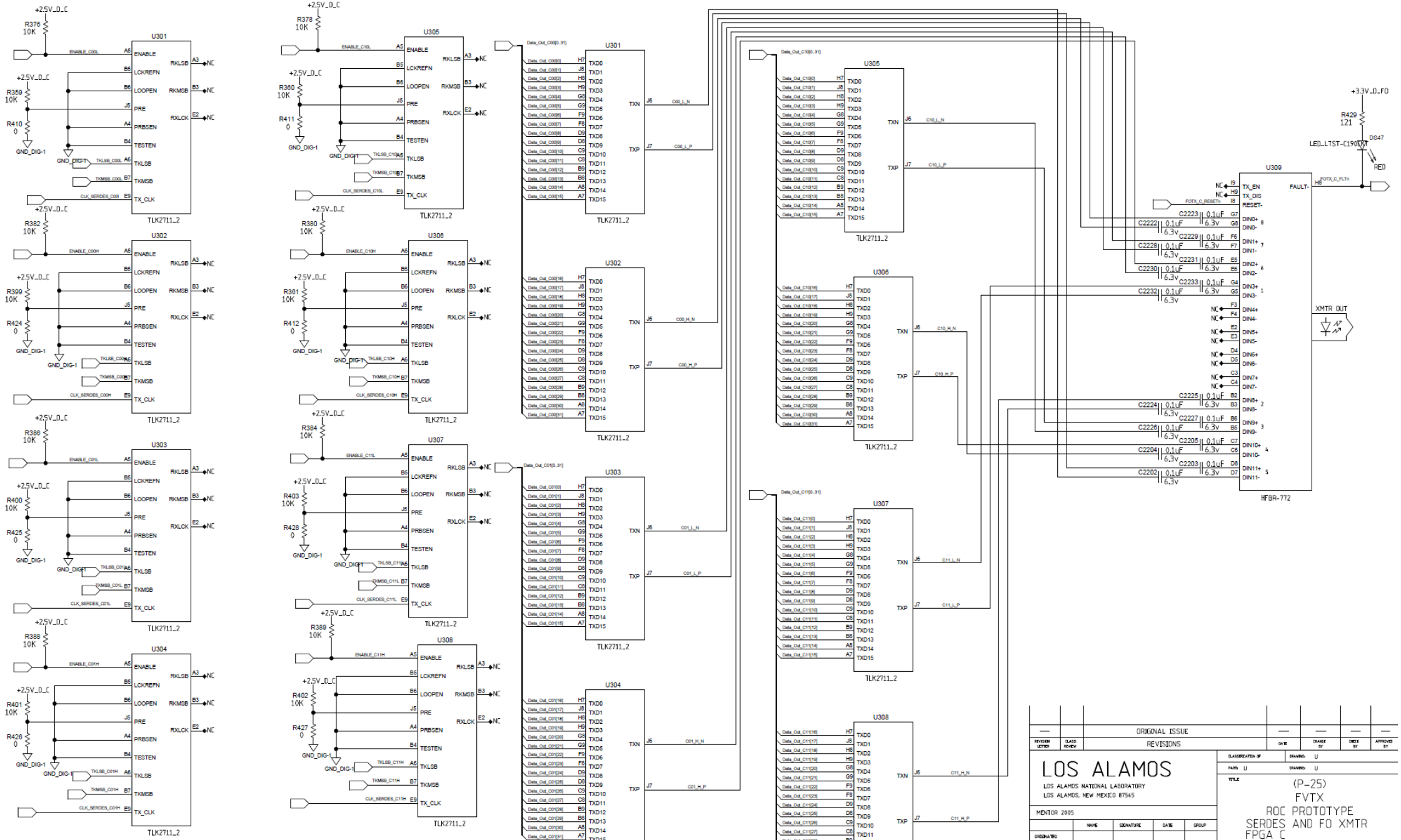
R81 10K
R99 10K
R155 10K
R134 10K
R181 10K
R193 10K
R351 10K
R350 10K
R347 10K
R346 10K
R352 10K
R349 10K
R348 10K
R345 10K
R25 0
R50 0
R98 0
R83 0
R136 0
R153 0
R190 0
R183 0
+2.5V_D_A
GND_DIG-1
R105 121
DS30
LED_LTST-C190KKT
+3.3VD1
XMTR OUT
FOTX_A_FLTn
FOTX_A_RESETn
2022/4/12
AS OF 07/11/2011 @ 9:33AM
ORIGINAL ISSUE
REVISIONS
LOS ALAMOS
LOS ALAMOS NATIONAL LABORATORY
LOS ALAMOS, NEW MEXICO 87545
MENTOR 2005
(P-25)
FVTX
ROC PROTOTYPE
SERDES AND FO XMTR
FPGA A
13



2022/4/12

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ORIGINAL ISSUE

REVISIONS

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LOS ALAMOS, NEW MEXICO 87545

MENTOR 2005

(P-25)
FVTX
ROC PROTOTYPE
SERDES AND FO XMTR
FPGA C

	NAME	SIGNATURE	DATE	GROUP
DESIGNATED				
DESIGNED				
DRAWN	S. CHACON	S. CHACON	APR 2009	AGT-JC
CHECKED	M. PROKOP	M. PROKOP	APR 2009	AGT-RFE
FULL ENGR.	M. PROKOP	M. PROKOP	APR 2009	AGT-RFE
APPROVED				

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