Fiber Sync Error Debug

RIKEN/RBRC

Itaru Nakagawa

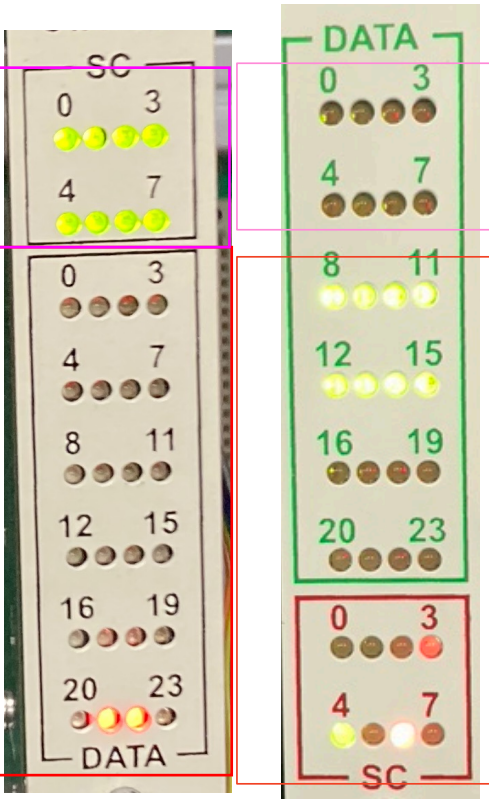
LEDの位置とポートの関係

Detail: FEM LED position and the meaning

Numbers which are written on FEM board panel are **different** from numbers of FPGA codes.

LED_OUT(7)~LED_OUT(0) of FPGA code (SlowControl_FEM.vhd)
=
No.0~7 of DATA on FEM board panel

LED_OUT(23)~LED_OUT(0) of FPGA code (FEM_top.vhd)
=
No.8~23 of DATA and No.0~7 of SC on FEM board panel



SlowControl_FEM.vhd
LED_OUT( )

7	6	5	4
3	2	1	0

FEM_top.vhd
LED_OUT( )

23	22	21	20
19	18	17	16
15	14	13	12
11	10	9	8
7	6	5	4
3	2	1	0

SYNC_OK	COMMAND_VME(2) = '1' and ((FEM_ADDR_VME = FEM_ADDR_REF) or FEM_ADDR_VME = x"F")	COMMAND_VME(1) = '1' and ((FEM_ADDR_VME = FEM_ADDR_REF) or FEM_ADDR_VME = x"F")	COMMAND_VME(0) = '1' and ((FEM_ADDR_VME = FEM_ADDR_REF) or FEM_ADDR_VME = x"F")
FEM_LVL1_DELAY(3 downto 1)	FEM_LVL1_DELAY(3 downto 1)	FEM_LVL1_DELAY(3 downto 1)	FEM_COMB_MODE

Station-1	SYNC_OK_3_3	SYNC_OK_3_2	SYNC_OK_3_1	SYNC_OK_3_0	Station-0
Station-3	SYNC_OK_2_3	SYNC_OK_2_2	SYNC_OK_2_1	SYNC_OK_2_0	Station-2
Station-3	SYNC_OK_1_3	SYNC_OK_1_2	SYNC_OK_1_1	SYNC_OK_1_0	Station-2
Station-1	SYNC_OK_0_3	SYNC_OK_0_2	SYNC_OK_0_1	SYNC_OK_0_0	Station-0
	DATA_IN_0_BUF(0)	DATA_IN_1_BUF(0)	DATA_IN_2_BUF(0)	DATA_IN_3_BUF(0)	
	ENPTY	BUSY	MODE	Z	

bottom

top

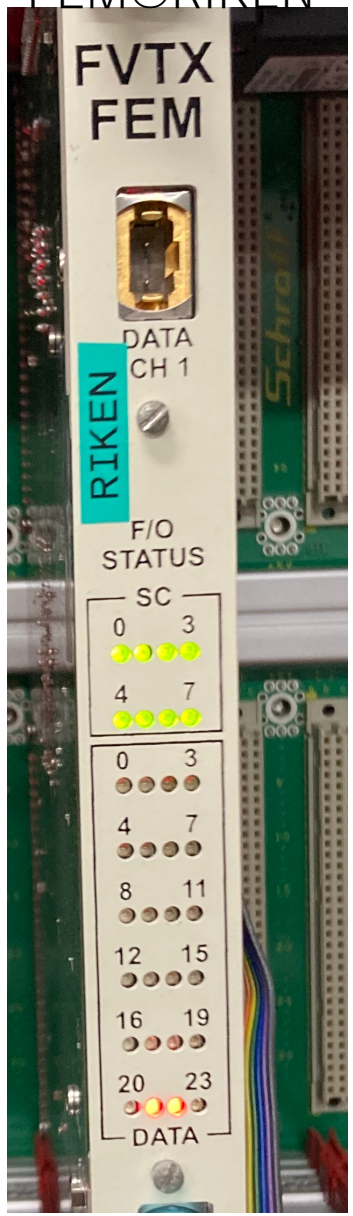
ENPTY and BUSY flash when calibration test is running

Codes in previous page is consistent with Mika Shibata's FEM-IB debugging (LED_Instruction.pdf)

FEM_DATA_Fiber_Mapping.xlsx

Data Signal Name	Sync Signal	Fiber Location	Station	TEST_OUTPUT	LED Location
DATA_IN_0_0	SYNC_OK_0_0, SYNC_OK_0_1	top	0	0	8,9
DATA_IN_0_1	SYNC_OK_0_2, SYNC_OK_0_3	top	1	4	10,11
DATA_IN_1_0	SYNC_OK_1_0, SYNC_OK_1_1	top	2	1	12,13
DATA_IN_1_1	SYNC_OK_1_2, SYNC_OK_1_3	top	3	5	14,15
DATA_IN_3_0	SYNC_OK_3_0, SYNC_OK_3_1	bottom	0	3	20,21
DATA_IN_3_1	SYNC_OK_3_2, SYNC_OK_3_3	bottom	1	7	22,23
DATA_IN_2_0	SYNC_OK_2_0, SYNC_OK_2_1	bottom	2	2	16,17
DATA_IN_2_1	SYNC_OK_2_2, SYNC_OK_2_3	bottom	3	6	18,19

FEM@RIKEN



This table has been provided from FVTX group for FVTX trigger development.

BottomファイバーのLED

FEM_DATA_Fiber_Mappingと柴田さんの予想

LED位置				
	23 Station-1	22 Station-1	21 Station-0	20 Station-0
	19 Station-3	18 Station-3	17 Station-2	16 Station-2

今井さんの観測*

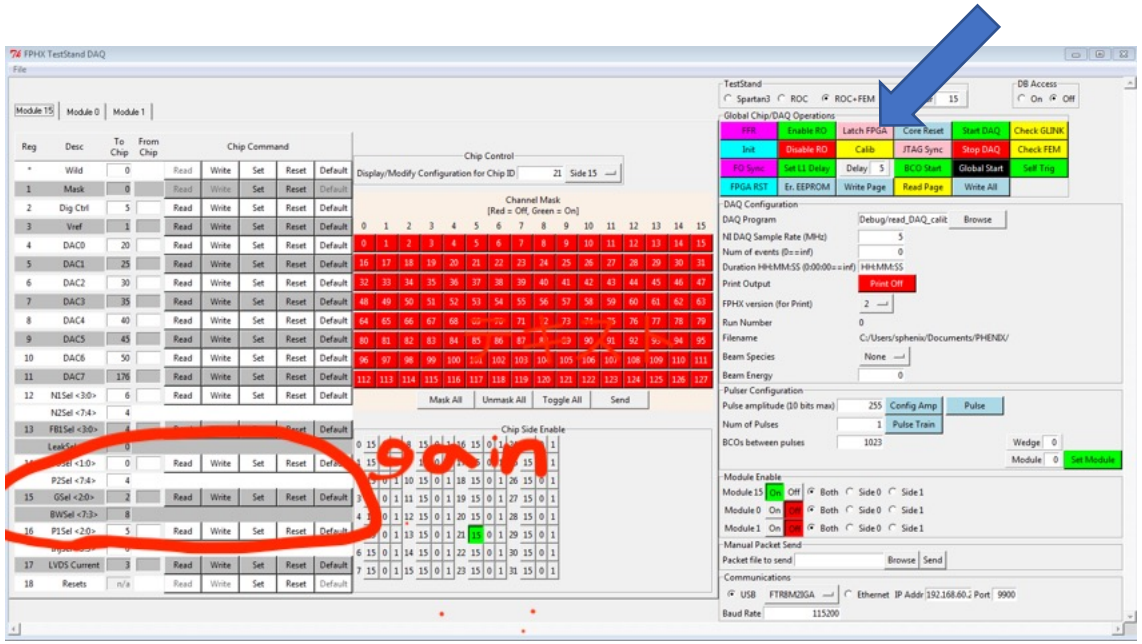
23 Station-2	22 Station-2	21 Station-3	20 Station-3
19 Station-0	18 Station-0	17 Station-1	16 Station-1

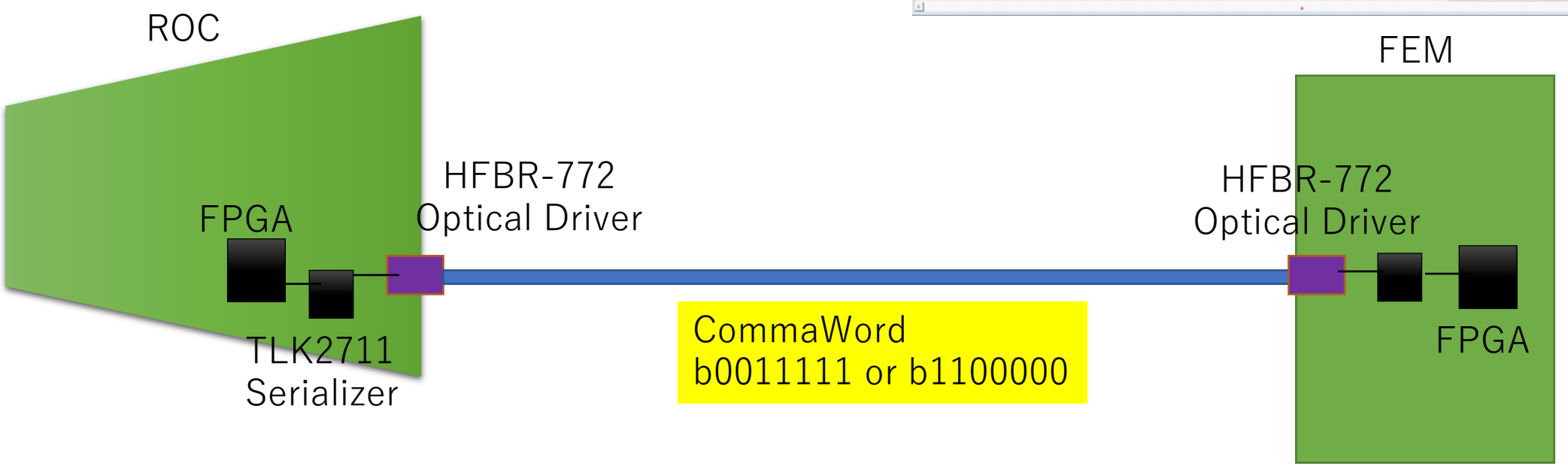
*LEDの不点灯時に、どのポートのキャリブレーションが失敗するかで相関をとった。

Fiber Sync Error Debug

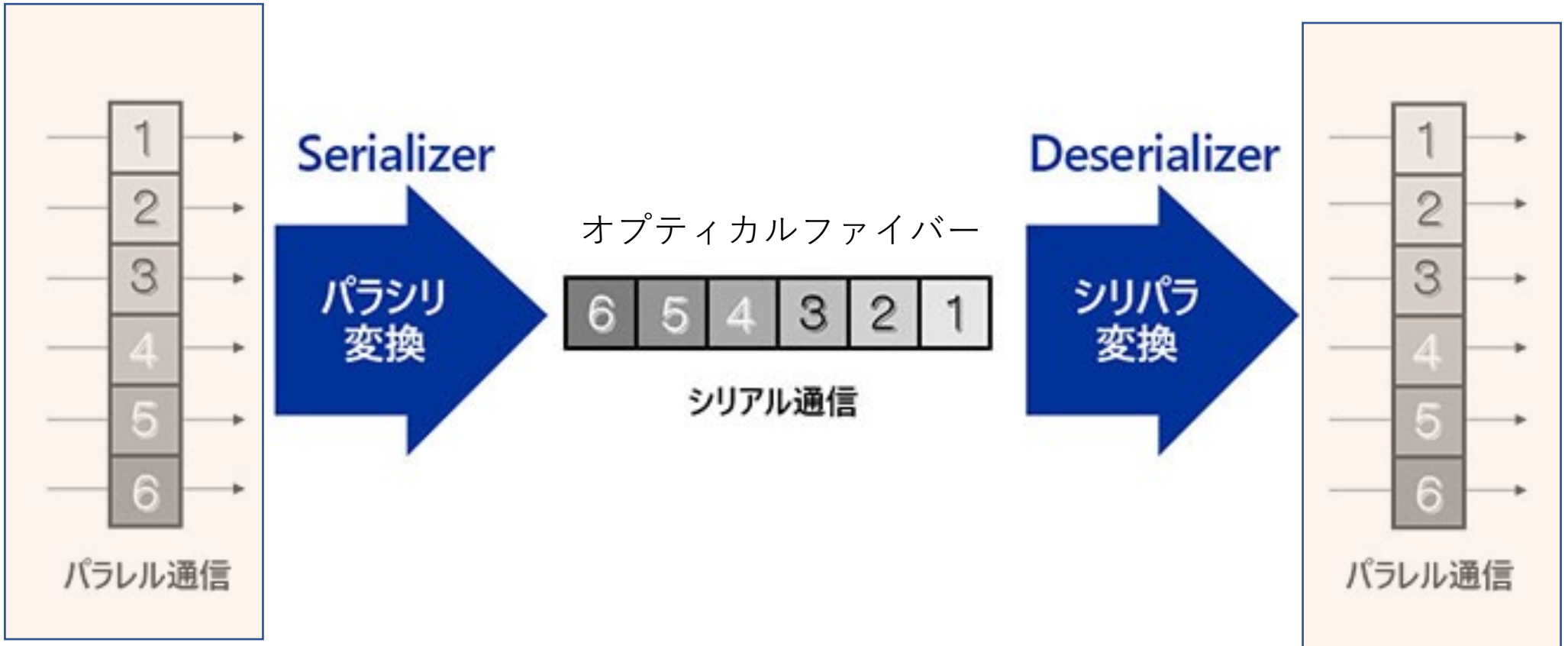
Fiber Synchronization

データ通信前の下準備





パラレル⇄シリアル変換



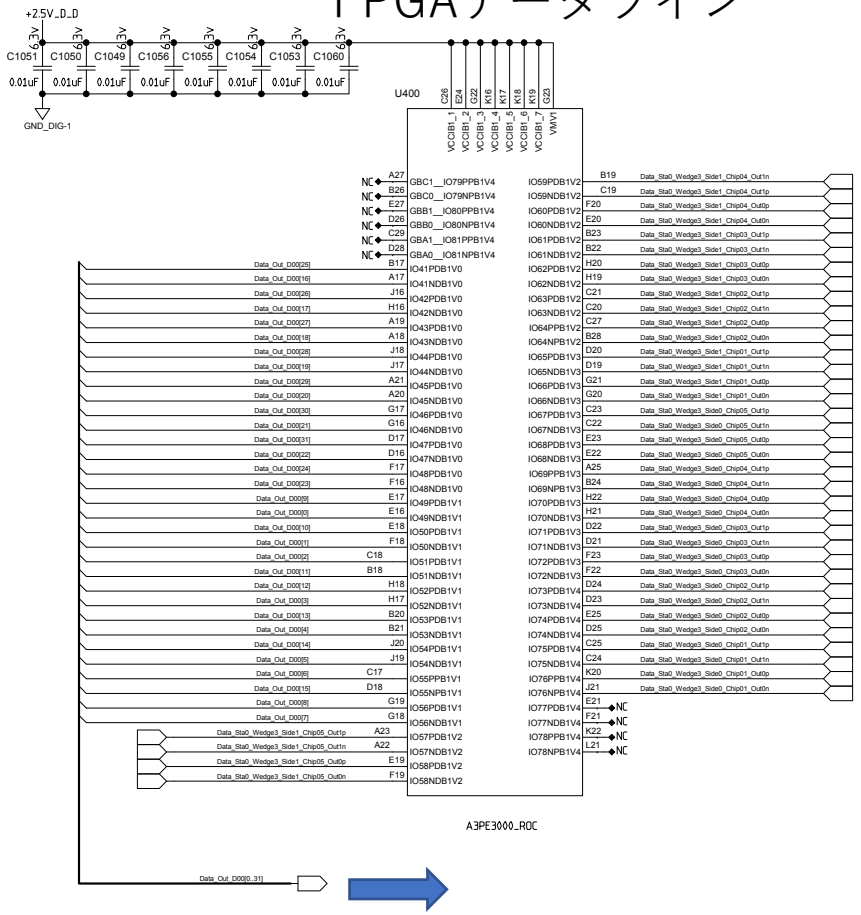
ROC FPGA内処理

FEM FPGA内処理

https://www.net-vision.co.jp/solution/serdes.html

Data FPGA Column-D

FPGAデータライン

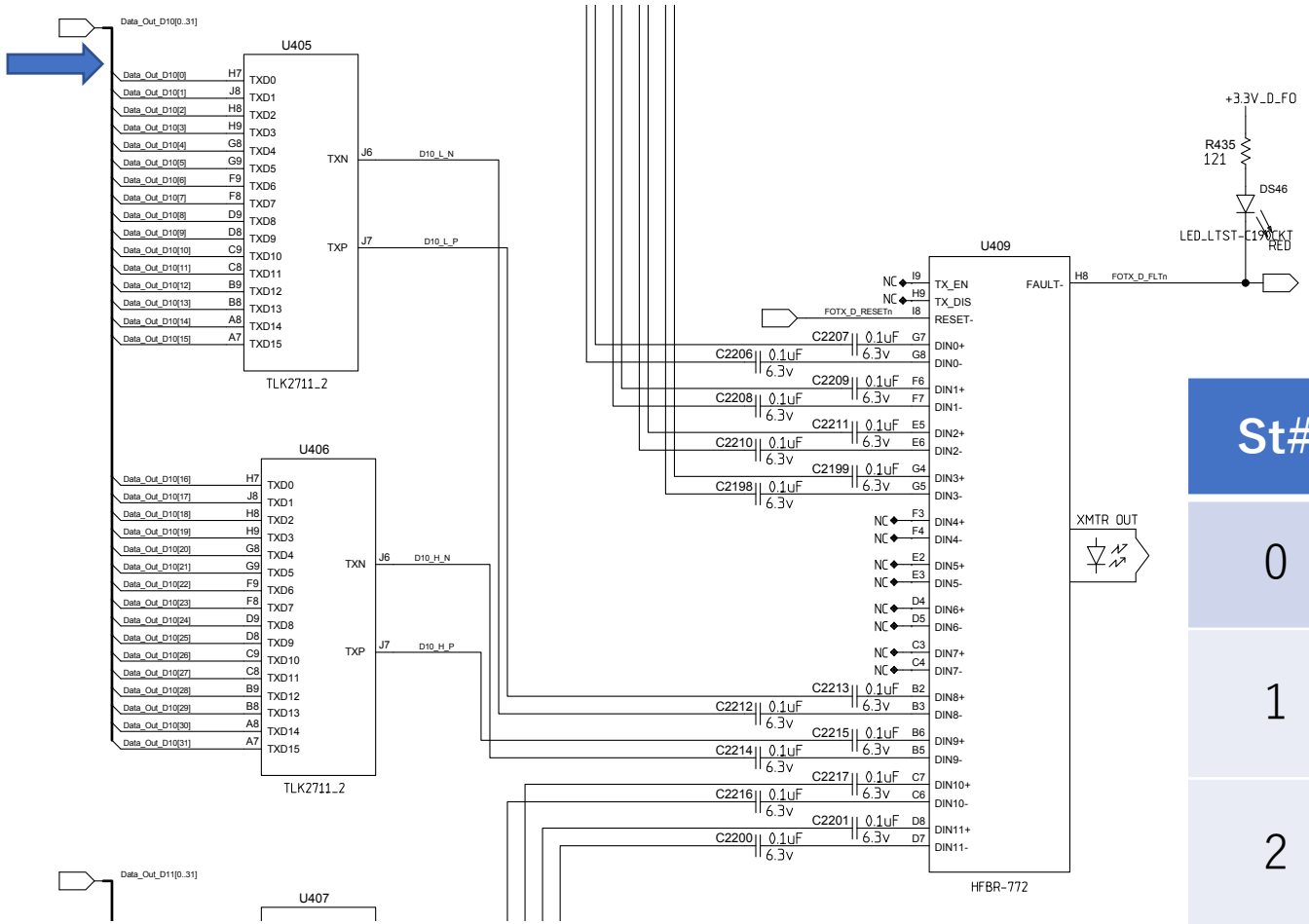


TLK2711 Serializerへ

Station	Data
0	Data_Out_D00[0-31]
1	Data_Out_D01[0-31]
2	Data_Out_D10[0-31]
3	Data_Out_D11[0-31]

TLK2711 Serializer

FPGAから



8.3.12 Comma Detect and 8-Bit/10-Bit Decoding

The TLK2711-SP has two parallel 8-bit/10-bit decode circuits. Each 8-bit/10-bit decoder converts 10-bit encoded data (half of the 20-bit received word) back into 8 bits. The comma-detect circuit is designed to provide for byte synchronization to an 8-bit/10-bit transmission code. When parallel data is clocked into a parallel-to-serial converter, the byte boundary that was associated with the parallel data is now lost in the serialization of the data. When the serial data is received and converted to parallel format again, a method is needed to recognize the byte boundary. Typically, this is accomplished through the use of a synchronization pattern. This is typically a unique pattern of 1s and 0s that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. The 8-bit/10-bit encoding contains a character called the comma (b0011111 or b1100000), which is used by the comma-detect circuit on the TLK2711-SP to align the received serial data back to its original byte boundary. The decoder detects the comma, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding; the comma is mapped into the LSB. The decoder then converts the data back into 8-bit data. The output from the two decoders is latched into the 16-bit register synchronized to the recovered parallel data clock (RXCLK) and output valid on the rising edge of the RXCLK.

NOTE

The TLK2711-SP only achieves byte alignment on the 0011111 comma.

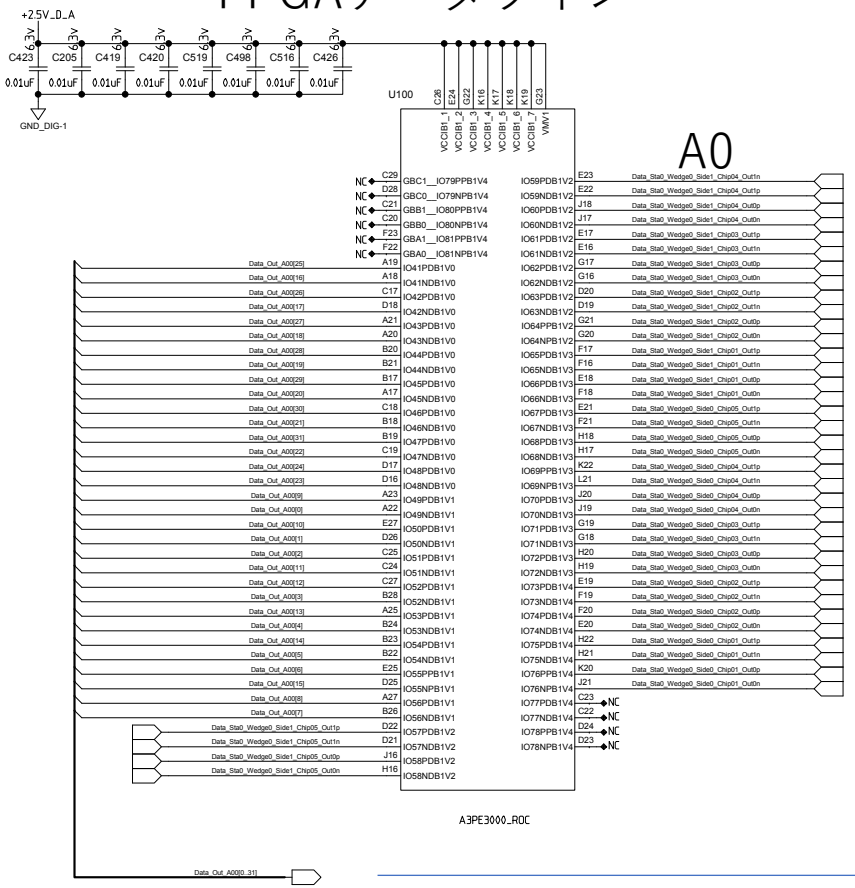
Decoding provides two additional status signals, RKLSB and RKMSB. When RKLSB is asserted, an 8-bit/10-bit K code is received and the specific K code is presented on the data bits RXD0 to RXD7; otherwise, an 8-bit/10-bit D code is received. When RKMSB is asserted, an 8-bit/10-bit K code is received and the specific K-code is presented on data bits RXD8 to RXD15; otherwise, an 8-bit/10-bit D code is received (see Table 3). The valid K codes the TLK2711-SP; decodes are provided in Table 4. An error detected on either byte, including K codes not in Table 4, causes that byte only to indicate a K0.0 code on the RKxSB and associated data pins, where K0.0 is known to be an invalid 8-bit/10-bit code. A loss of input signal causes a K31.7 code to be presented on both bytes, where K31.7 is also known to be an invalid 8-bit/10-bit code.

St#	Data	Serializer	HFBR-772
0	Data_Out_D00 [0-31]		
1	Data_Out_D01 [0-31]		
2	Data_Out_D10 [0-31]	U405	DIN8+/-
		U406	DIN9+/-
3	Data_Out_D11 [0-31]		

A0 Portのデータライン

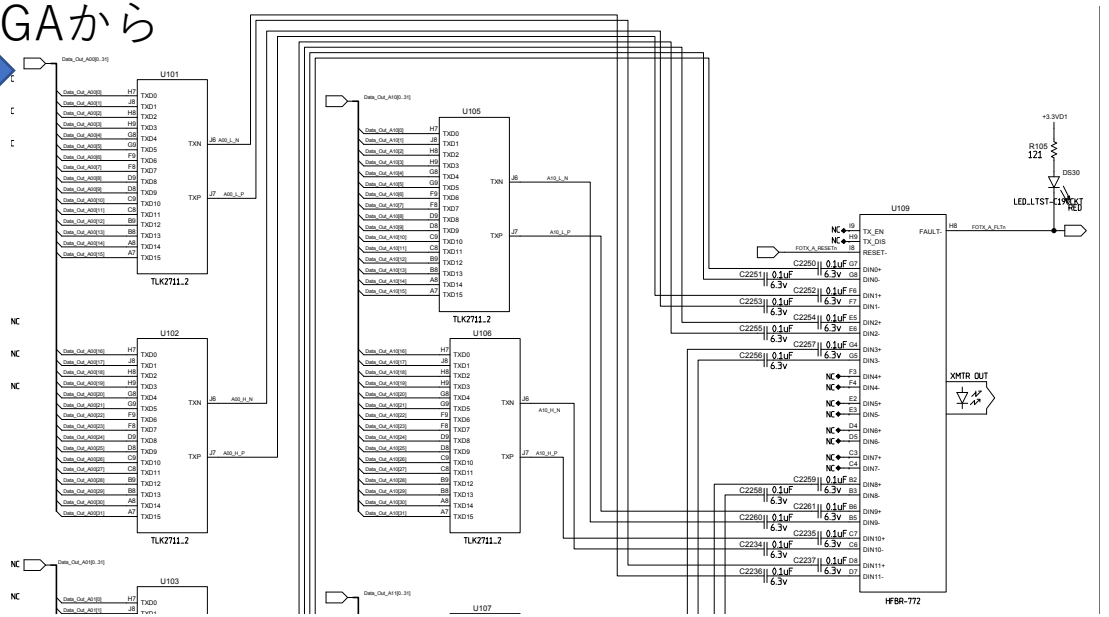
St#	Data	Serializer	HFBR-772
0	Data_Out_A00 [0-31]	U101	DIN11+/-
		U102	DIN1+/-
1	Data_Out_A01 [0-31]		
2	Data_Out_A10 [0-31]		
3	Data_Out_A11 [0-31]		

FPGAデータライン



TLK2711 Serializerへ

FPGAから



Transmitter Pad Assignment

TRANSMITTER MODULE PAD ASSIGNMENT
(TOWARD MTP® CONNECTOR)

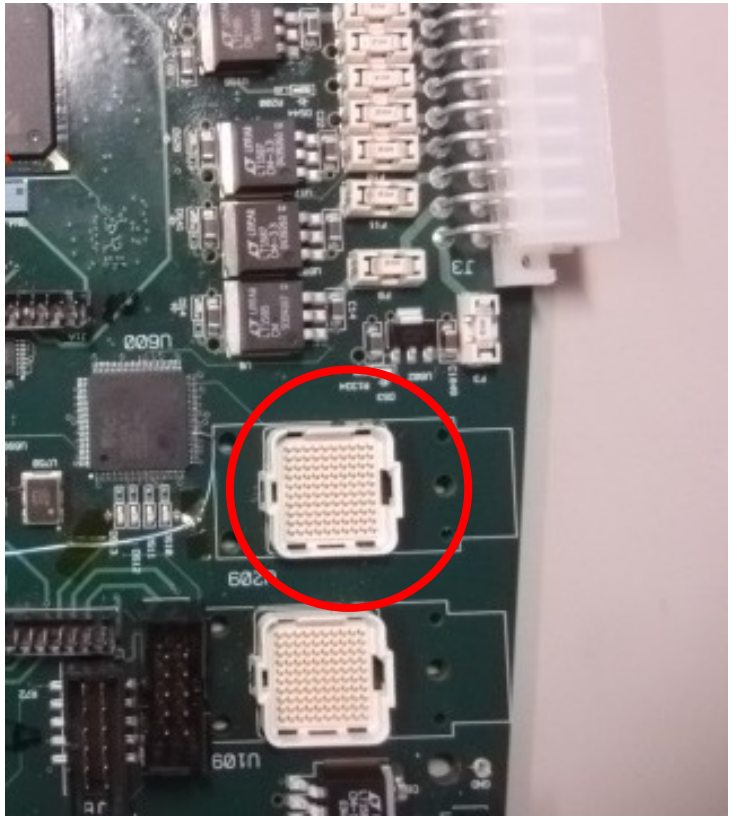
	J	I	H	G	F	E	D	C	B	A
1	DNC	DNC	DNC	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	DNC
2	DNC	DNC	DNC	V_{EE}	V_{EE}	DIN5+	V_{EE}	V_{EE}	DIN8+	V_{EE}
3	DNC	V_{CCT}	V_{CCT}	V_{EE}	DIN4+	DIN5-	V_{EE}	DIN7+	DIN8-	V_{EE}
4	DNC	V_{CCT}	V_{CCT}	DIN3+	DIN4-	V_{EE}	DIN6+	DIN7-	V_{EE}	DNC
5	DNC	V_{CCT}	V_{CCT}	DIN3-	V_{EE}	DIN2+	DIN6-	V_{EE}	DIN9-	V_{EE}
6	DNC	V_{CCT}	V_{CCT}	V_{EE}	DIN1+	DIN2-	V_{EE}	DIN10-	DIN9+	V_{EE}
7	DNC	DNC	DNC	DIN0+	DIN1-	V_{EE}	DIN11-	DIN10+	V_{EE}	DNC
8	DNC	RESET-	FAULT-	DIN0-	V_{EE}	V_{EE}	DIN11+	V_{EE}	V_{EE}	DNC
9	DNC	TX_EN	TX_DIS	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	DNC
10	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC

TOP VIEW (PCB LAYOUT)
(10 x 10 ARRAY)

HFBR-772

D2ポート上位16bit

D2ポート下位16bit



Optical Driverを外した状態で、
LATCH FPGAを実行した際のパターンをオシロで観測する。

CommaWord
b0011111 or b1100000

Transmitter Pad Assignment

	J	I	H	G	F	E	D	C	B	A
1	DNC	DNC	DNC	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	DNC
2	DNC	DNC	DNC	V_{EE}	V_{EE}	DIN5+	V_{EE}	V_{EE}	DIN8+	V_{EE}
3	DNC	V_{CCT}	V_{CCT}	V_{EE}	DIN4+	DIN5-	V_{EE}	DIN7+	DIN8-	V_{EE}
4	DNC	V_{CCT}	V_{CCT}	DIN3+	DIN4-	V_{EE}	DIN6+	DIN7-	V_{EE}	DNC
5	DNC	V_{CCT}	V_{CCT}	DIN3-	V_{EE}	DIN2+	DIN6-	V_{EE}	DIN9-	V_{EE}
6	DNC	V_{CCT}	V_{CCT}	V_{EE}	DIN1+	DIN2-	V_{EE}	DIN10-	DIN9+	V_{EE}
7	DNC	DNC	DNC	DIN0+	DIN1-	V_{EE}	DIN11-	DIN10+	V_{EE}	DNC
8	DNC	RESET-	FAULT-	DIN0-	V_{EE}	V_{EE}	DIN11+	V_{EE}	V_{EE}	DNC
9	DNC	TX_EN	TX_DIS	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	DNC
10	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC

HFBR-772

Table 1. Transmitter Module Pad Description

Symbol	Functional Description
V_{EE}	Transmitter Signal Common. All voltages are referenced to this potential unless otherwise indicated. Directly connect these pads to transmitter signal ground plane.
$V_{CC}T$	Transmitter Power Supply. Use recommended power supply filter circuit in Figure 6.
DIN0+ through DIN11+	Transmitter Data In+ for channels 0 through 11, respectively. Differential termination and self bias are included, see Figure 11.
DIN0– through DIN11–	Transmitter Data In- for channels 0 through 11, respectively. Differential termination and self bias are included; see Figure 11.
TX_EN	TX Enable. Active high. Internal pull-up High = VCSEL array is enabled if TX_DIS is inactive (Low). Low = VCSEL array is off. TX_EN must be taken to a logic low state level (V_{OL}) for 1 ms or longer.
TX_DIS	TX Disable. Active high. Internal pull-down Low = VCSEL array is enabled if TX_EN is active (High). High = VCSEL array is off. TX_DIS must be taken to a logic High state level (V_{OH}) for 1 ms or longer.
RESET-	Transmitter RESET- input. Active low. Internal pull-up. Low = Resets logic function clears FAULT- signal, VCSEL array is off. high = Normal operation. See Figure 14.
FAULT-	Transmitter FAULT- output. Active low. Low (logic "0") results from a VCSEL over-current condition, out of temperature range, or EEPROM calibration data corruption condition detected for any VCSEL. An asserted (logic "0") FAULT- disables the VCSEL array and is cleared by RESET- or power cycling $V_{CC}T$ FAULT- is a single ended LVTTL compatible output.
DNC	Do not connect to any electrical potential.

電源はそれぞれのファイバーに共通で、ファイバー１本だけ不具合を起こす要素はあまりなさそう。

CommaDetectについて

8.3.12 Comma Detect and 8-Bit/10-Bit Decoding

The TLK2711-SP has two parallel 8-bit/10-bit decode circuits. Each 8-bit/10-bit decoder converts 10-bit encoded data (half of the 20-bit received word) back into 8 bits. The comma-detect circuit is designed to provide for byte synchronization to an 8-bit/10-bit transmission code. When parallel data is clocked into a parallel-to-serial converter, the byte boundary that was associated with the parallel data is now lost in the serialization of the data. When the serial data is received and converted to parallel format again, a method is needed to recognize the byte boundary. Typically, this is accomplished through the use of a synchronization pattern. This is typically a unique pattern of 1s and 0s that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. The 8-bit/10-bit encoding contains a character called the comma (b0011111 or b1100000), which is used by the comma-detect circuit on the TLK2711-SP to align the received serial data back to its original byte boundary. The decoder detects the comma, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding; the comma is mapped into the LSB. The decoder then converts the data back into 8-bit data. The output from the two decoders is latched into the 16-bit register synchronized to the recovered parallel data clock (RXCLK) and output valid on the rising edge of the RXCLK.

NOTE

The TLK2711-SP only achieves byte alignment on the 0011111 comma.

Decoding provides two additional status signals, RKLSB and RKMSB. When RKLSB is asserted, an 8-bit/10-bit K code is received and the specific K code is presented on the data bits RXD0 to RXD7; otherwise, an 8-bit/10-bit D code is received. When RKMSB is asserted, an 8-bit/10-bit K code is received and the specific K-code is presented on data bits RXD8 to RXD15; otherwise, an 8-bit/10-bit D code is received (see Table 3). The valid K codes the TLK2711-SP; decodes are provided in Table 4. An error detected on either byte, including K codes not in Table 4, causes that byte only to indicate a K0.0 code on the RKxSB and associated data pins, where K0.0 is known to be an invalid 8-bit/10-bit code. A loss of input signal causes a K31.7 code to be presented on both bytes, where K31.7 is also known to be an invalid 8-bit/10-bit code.

To do

- A0ポートでデバッグする。