

マイクロ同軸ケーブル試作2 号機のチャンネルマップ確認

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1.チャンネルマップの導線確認

2.HARNESSE CHECKER(CN50機)を用いた導通測定

チャンネルマップの導線確認

1. マイクロ同軸ケーブルROC側とBEX側のそれぞれのJ1コネクタに写真のDF18拡張基板を取り付ける。
2. 例えば、BDタイプのJ1チャンネル2はBEX側で0_CHIP1_OUT_1Pなので、ROC側のテーブルで同じ名前0_CHIP1_OUT_1Pのチャンネルを探す。
3. 拡張基板上の対応するチャンネルのパッドや半田面にテストのプローブをあて、導通しているか確認する。
4. 対応するチャンネル以外で導通していないか確認する。

BEX側チャンネルマップ

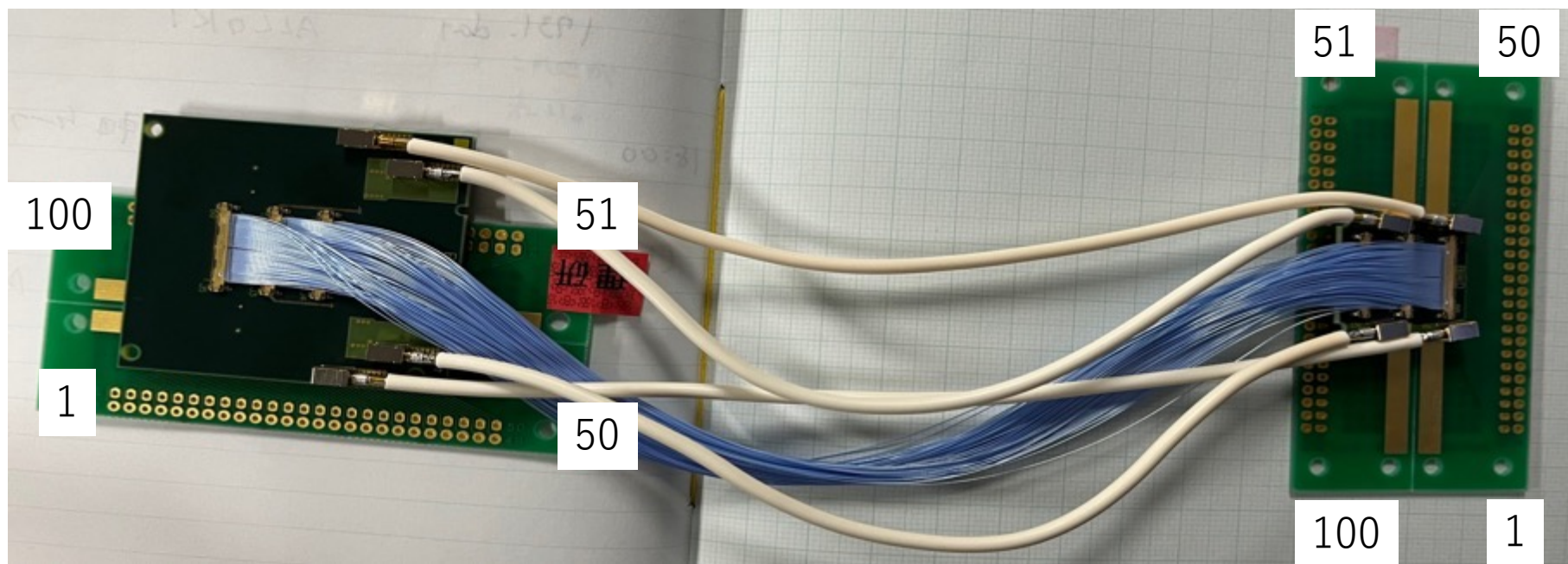
ROC側チャンネルマップ

HDI側							
HEADER (TOP)							
J1 (out side)				J2 (in side)			
#	name (net)	#	name (net)	#	name (net)	#	name (net)
1	DGND	100	AGND	1	AGND	100	DGND
2	0_CHIP1_OUT 1P	99	0_CHIP1_OUT 0P	2	1_CHIP1_OUT 1P	99	1_CHIP1_OUT 0P
3	0_CHIP1_OUT 1N	98	0_CHIP1_OUT 0N	3	1_CHIP1_OUT 1N	98	1_CHIP1_OUT 0N
4	0_CHIP2_OUT 1P	97	0_CHIP2_OUT 0P	4	1_CHIP2_OUT 1P	97	1_CHIP2_OUT 0P
5	0_CHIP2_OUT 1N	96	0_CHIP2_OUT 0N	5	1_CHIP2_OUT 1N	96	1_CHIP2_OUT 0N
6	0_CHIP3_OUT 1P	95	0_CHIP3_OUT 0P	6	1_CHIP3_OUT 1P	95	1_CHIP3_OUT 0P
7	0_CHIP3_OUT 1N	94	0_CHIP3_OUT 0N	7	1_CHIP3_OUT 1N	94	1_CHIP3_OUT 0N
8	0_CHIP4_OUT 1P	93	0_CHIP4_OUT 0P	8	1_CHIP4_OUT 1P	93	1_CHIP4_OUT 0P
9	0_CHIP4_OUT 1N	92	0_CHIP4_OUT 0N	9	1_CHIP4_OUT 1N	92	1_CHIP4_OUT 0N
10	DGND	91	0_CAL_INJECT0	10	1_CAL_INJECT1	91	DGND
11	DGND	90	AGND	11	AGND	90	DGND
12	0_CHIP5_OUT 1P	89	0_CHIP5_OUT 0P	12	1_CHIP5_OUT 1P	89	1_CHIP5_OUT 0P
13	0_CHIP5_OUT 1N	88	0_CHIP5_OUT 0N	13	1_CHIP5_OUT 1N	88	1_CHIP5_OUT 0N
14	0_CHIP7_OUT 1P	87	0_CHIP7_OUT 0P	14	1_CHIP7_OUT 1P	87	1_CHIP7_OUT 0P
15	0_CHIP7_OUT 1N	86	0_CHIP7_OUT 0N	15	1_CHIP7_OUT 1N	86	1_CHIP7_OUT 0N
16	0_CHIP9_OUT 1P	85	0_CHIP9_OUT 0P	16	1_CHIP9_OUT 1P	85	1_CHIP9_OUT 0P
17	0_CHIP9_OUT 1N	84	0_CHIP9_OUT 0N	17	1_CHIP9_OUT 1N	84	1_CHIP9_OUT 0N
18	0_CHIP11_OUT 1P	83	0_CHIP11_OUT 0P	18	1_CHIP11_OUT 1P	83	1_CHIP11_OUT 0P
19	0_CHIP11_OUT 1N	82	0_CHIP11_OUT 0N	19	1_CHIP11_OUT 1N	82	1_CHIP11_OUT 0N
20	0_CHIP13_OUT 1P	81	0_CHIP13_OUT 0P	20	1_CHIP13_OUT 1P	81	1_CHIP13_OUT 0P
21	0_CHIP13_OUT 1N	80	0_CHIP13_OUT 0N	21	1_CHIP13_OUT 1N	80	1_CHIP13_OUT 0N
22	DGND	79	AGND	22	AGND	79	DGND
23	DGND	78	AGND	23	AGND	78	DGND
24	0_CHIP6_OUT 1P	77	0_CHIP6_OUT 0P	24	1_CHIP6_OUT 1P	77	1_CHIP6_OUT 0P
25	0_CHIP6_OUT 1N	76	0_CHIP6_OUT 0N	25	1_CHIP6_OUT 1N	76	1_CHIP6_OUT 0N
26	0_CHIP8_OUT 1P	75	0_CHIP8_OUT 0P	26	1_CHIP8_OUT 1P	75	1_CHIP8_OUT 0P
27	0_CHIP8_OUT 1N	74	0_CHIP8_OUT 0N	27	1_CHIP8_OUT 1N	74	1_CHIP8_OUT 0N
28	0_CHIP10_OUT 1P	73	0_CHIP10_OUT 0P	28	1_CHIP10_OUT 1P	73	1_CHIP10_OUT 0P
29	0_CHIP10_OUT 1N	72	0_CHIP10_OUT 0N	29	1_CHIP10_OUT 1N	72	1_CHIP10_OUT 0N
30	0_CHIP12_OUT 1P	71	0_CHIP12_OUT 0P	30	1_CHIP12_OUT 1P	71	1_CHIP12_OUT 0P
31	0_CHIP12_OUT 1N	70	0_CHIP12_OUT 0N	31	1_CHIP12_OUT 1N	70	1_CHIP12_OUT 0N
32	DGND	69	AGND	32	AGND	69	DGND
33	DGND	68	AGND	33	AGND	68	DGND
34	0_SC_OUT0n	67	0_OUT_CLK0n	34	1_OUT_CLK1n	67	1_SC_OUT1p
35	0_SC_OUT0p	66	0_OUT_CLK0p	35	1_OUT_CLK1p	66	1_SC_OUT1p
36	DGND	65	0_BCO_CLK0n	36	1_BCO_CLK1n	65	DGND
37	DGND	64	0_BCO_CLK0p	37	1_BCO_CLK1p	64	DGND
38	DGND	63	0_SC_IN0n	38	1_SC_IN1n	63	DGND
39	DGND	62	0_SC_IN0p	39	1_SC_IN1p	62	DGND
40	DGND	61	0_RESET0n	40	1_RESET1n	61	DGND
41	DGND	60	0_RESET0p	41	1_RESET1p	60	DGND
42	DGND	59	AGND	42	AGND	59	DGND
43	DGND	58	AGND	43	AGND	58	DGND
44	+2.5VA	57	AGND	44	+2.5VD	57	+2.5VD
45	+2.5VA	56	AGND	45	+2.5VD	56	+2.5VD
46	+2.5VA	55	+2.5VA	46	+2.5VD	55	+2.5VD
47	+2.5VA	54	+2.5VA	47	+2.5VD	54	+2.5VD
48	+2.5VA	53	+2.5VA	48	+2.5VD	53	+2.5VD
49	+2.5VA	52	+2.5VA	49	+2.5VD	52	+2.5VD
50	+2.5VA	51	+2.5VA	50	+2.5VD	51	+2.5VD

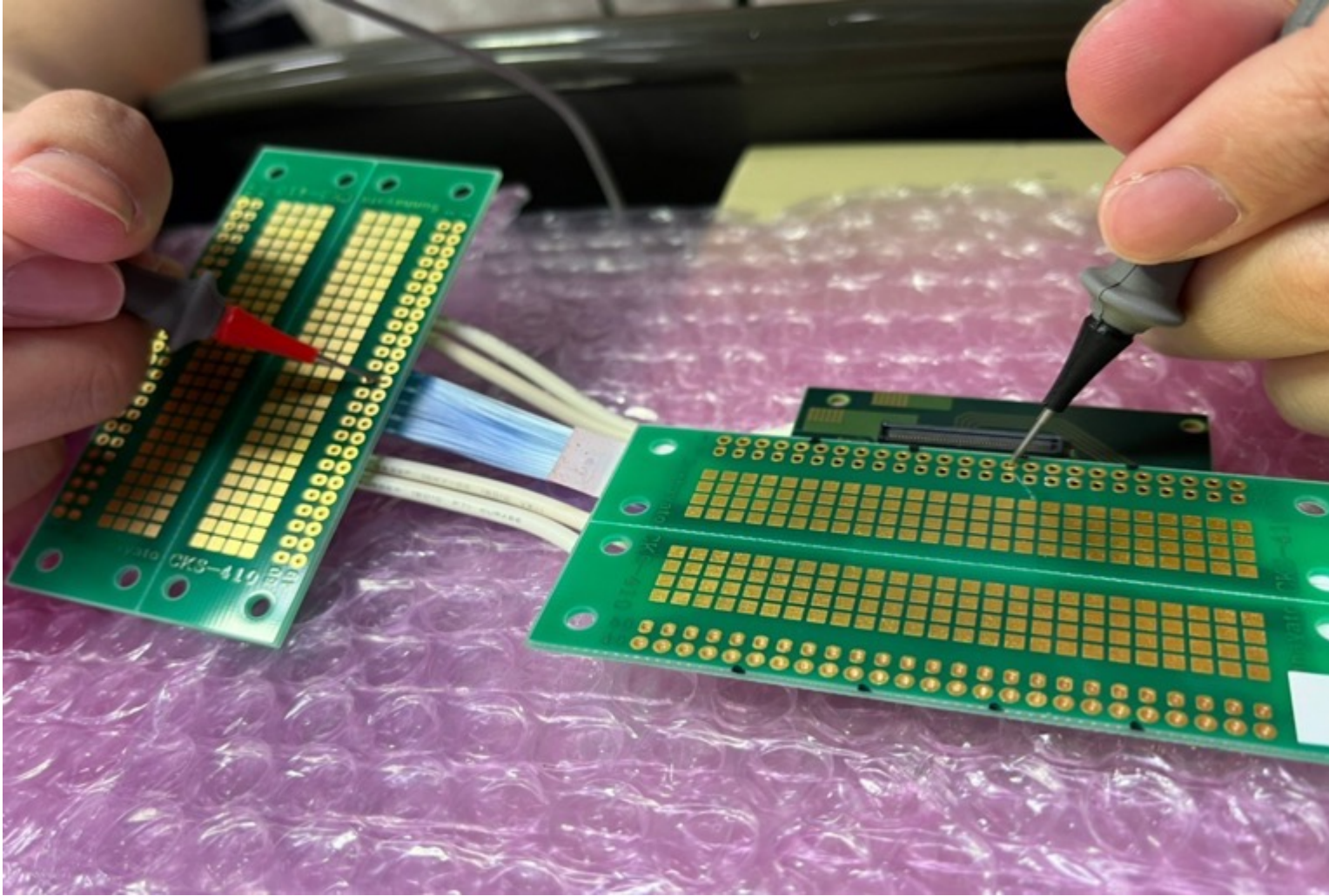
ROC側							
RECEPTACLE (TOP)							
J1 (out side)				J2 (in side)			
#	name (net)	#	name (net)	#	name (net)	#	name (net)
1	AGND	100	DGND	1	AGND	100	DGND
2	1_CHIP1_OUT 1P	99	1_CHIP1_OUT 0P	2	SC_IN1p	99	RESET1p
3	1_CHIP1_OUT 1N	98	1_CHIP1_OUT 0N	3	SC_IN1n	98	RESET1n
4	1_CHIP2_OUT 1P	97	1_CHIP2_OUT 0P	4	DGND	97	BCO_CLK1p
5	1_CHIP2_OUT 1N	96	1_CHIP2_OUT 0N	5	DGND	96	BCO_CLK1n
6	1_CHIP3_OUT 1P	95	1_CHIP3_OUT 0P	6	OUT_CLK1p	95	SC_OUT1p
7	1_CHIP3_OUT 1N	94	1_CHIP3_OUT 0N	7	OUT_CLK1n	94	SC_OUT1n
8	1_CHIP4_OUT 1P	93	1_CHIP4_OUT 0P	8	DGND	93	DGND
9	1_CHIP4_OUT 1N	92	1_CHIP4_OUT 0N	9	DGND	92	DGND
10	DGND	91	DGND	10	DGND	91	DGND
11	DGND	90	DGND	11	DGND	90	DGND
12	DGND	89	DGND	12	DGND	89	DGND
13	DGND	88	DGND	13	DGND	88	DGND
14	DGND	87	DGND	14	DGND	87	DGND
15	DGND	86	DGND	15	DGND	86	DGND
16	DGND	85	DGND	16	DGND	85	DGND
17	DGND	84	DGND	17	DGND	84	DGND
18	DGND	83	DGND	18	DGND	83	DGND
19	DGND	82	DGND	19	DGND	82	DGND
20	DGND	81	DGND	20	DGND	81	DGND
21	DGND	80	DGND	21	DGND	80	DGND
22	DGND	79	DGND	22	DGND	79	DGND
23	DGND	78	DGND	23	DGND	78	DGND
24	DGND	77	DGND	24	DGND	77	DGND
25	DGND	76	DGND	25	DGND	76	DGND
26	DGND	75	DGND	26	DGND	75	DGND
27	DGND	74	DGND	27	DGND	74	DGND
28	DGND	73	DGND	28	DGND	73	DGND
29	DGND	72	DGND	29	DGND	72	DGND
30	DGND	71	DGND	30	DGND	71	DGND
31	DGND	70	DGND	31	DGND	70	DGND
32	DGND	69	DGND	32	DGND	69	DGND
33	DGND	68	DGND	33	DGND	68	DGND
34	DGND	67	DGND	34	DGND	67	DGND
35	0_CHIP9_OUT 0P	66	0_CHIP9_OUT 1P	35	0_CHIP12_OUT 0P	66	0_CHIP12_OUT 1P
36	0_CHIP7_OUT 0N	65	0_CHIP7_OUT 1N	36	0_CHIP10_OUT 0N	65	0_CHIP10_OUT 1N
37	0_CHIP7_OUT 0P	64	0_CHIP7_OUT 1P	37	0_CHIP10_OUT 0P	64	0_CHIP10_OUT 1P
38	0_CHIP5_OUT 0N	63	0_CHIP5_OUT 1N	38	0_CHIP8_OUT 0N	63	0_CHIP8_OUT 1N
39	0_CHIP5_OUT 0P	62	0_CHIP5_OUT 1P	39	0_CHIP8_OUT 0P	62	0_CHIP8_OUT 1P
40	AGND	61	DGND	40	0_CHIP6_OUT 0N	61	0_CHIP6_OUT 1N
41	CAL_INJECT0	60	DGND	41	0_CHIP6_OUT 0P	60	0_CHIP6_OUT 1P
42	0_CHIP4_OUT 0N	59	0_CHIP4_OUT 1N	42	DGND	59	DGND
43	0_CHIP4_OUT 0P	58	0_CHIP4_OUT 1P	43	DGND	58	DGND
44	0_CHIP3_OUT 0N	57	0_CHIP3_OUT 1N	44	OUT_CLK0n	57	SC_OUT0p
45	0_CHIP3_OUT 0P	56	0_CHIP3_OUT 1P	45	OUT_CLK0p	56	SC_OUT0n
46	0_CHIP2_OUT 0N	55	0_CHIP2_OUT 1N	46	DGND	55	RESET0p
47	0_CHIP2_OUT 0P	54	0_CHIP2_OUT 1P	47	DGND	54	RESET0n
48	0_CHIP1_OUT 0N	53	0_CHIP1_OUT 1N	48	SC_IN0p	53	BCO_CLK0p
49	0_CHIP1_OUT 0P	52	0_CHIP1_OUT 1P	49	SC_IN0n	52	BCO_CLK0n
50	AGND	51	DGND	50	AGND	51	DGND

0_CHIP1_OUT_1PはラダーのSide-0 (Chip1-13側)、Chip1の読み出しデータライン1番の+側を表す。このチャンネルはBEX側では、J1コネクタのチャンネル2に現れROC側ではJ1コネクタのチャンネル52番に繋がれているはず。拡張基板上でテスターのプローブをこの二つのチャンネルにあてると、導通しているはず。

マイクロ同軸ケーブル試作 2号機



確認方法



BDタイプの変換ケーブル製作は今回が初めてのため、CN50機のリファレンスマップがないので、テスターで信号線一本一本導通確認をした。

結果

HDI側						ROC側							
HEADER (TOP)						RECEPTACLE (TOP)							
J1 (out side)			J2 (in side)			J1 (out side)			J2 (in side)				
#	name (net)	#	name (net)	#	name (net)	#	name (net)	#	name (net)	#	name (net)	#	name (net)
1	DGND	100	AGND	1	AGND	100	DGND	1	AGND	100	DGND	1	AGND
2	0_CHIP1_OUT 1P	99	0_CHIP1_OUT 0P	2	1_CHIP1_OUT 1P	99	1_CHIP1_OUT 0P	2	1_CHIP1_OUT 1P	99	1_CHIP1_OUT 0P	2	SC_IN1p
3	0_CHIP1_OUT 1N	98	0_CHIP1_OUT 0N	3	1_CHIP1_OUT 1N	98	1_CHIP1_OUT 0N	3	1_CHIP1_OUT 1N	98	1_CHIP1_OUT 0N	3	SC_IN1n
4	0_CHIP2_OUT 1P	97	0_CHIP2_OUT 0P	4	1_CHIP2_OUT 1P	97	1_CHIP2_OUT 0P	4	1_CHIP2_OUT 1P	97	1_CHIP2_OUT 0P	4	DGND
5	0_CHIP2_OUT 1N	96	0_CHIP2_OUT 0N	5	1_CHIP2_OUT 1N	96	1_CHIP2_OUT 0N	5	1_CHIP2_OUT 1N	96	1_CHIP2_OUT 0N	5	DGND
6	0_CHIP3_OUT 1P	95	0_CHIP3_OUT 0P	6	1_CHIP3_OUT 1P	95	1_CHIP3_OUT 0P	6	1_CHIP3_OUT 1P	95	1_CHIP3_OUT 0P	6	OUT_CLK1p
7	0_CHIP3_OUT 1N	94	0_CHIP3_OUT 0N	7	1_CHIP3_OUT 1N	94	1_CHIP3_OUT 0N	7	1_CHIP3_OUT 1N	94	1_CHIP3_OUT 0N	7	OUT_CLK1n
8	0_CHIP4_OUT 1P	93	0_CHIP4_OUT 0P	8	1_CHIP4_OUT 1P	93	1_CHIP4_OUT 0P	8	1_CHIP4_OUT 1P	93	1_CHIP4_OUT 0P	8	DGND
9	0_CHIP4_OUT 1N	92	0_CHIP4_OUT 0N	9	1_CHIP4_OUT 1N	92	1_CHIP4_OUT 0N	9	1_CHIP4_OUT 1N	92	1_CHIP4_OUT 0N	9	DGND
10	DGND	91	0_CAL_INJECT0	10	1_CAL_INJECT1	91	DGND	10	CAL_INJECT1	91	DGND	10	1_CHIP6_OUT 1P
11	DGND	90	AGND	11	AGND	90	DGND	11	AGND	90	DGND	11	1_CHIP6_OUT 1N
12	0_CHIP5_OUT 1P	89	0_CHIP5_OUT 0P	12	1_CHIP5_OUT 1P	89	1_CHIP5_OUT 0P	12	1_CHIP5_OUT 1P	89	1_CHIP5_OUT 0P	12	1_CHIP8_OUT 1P
13	0_CHIP5_OUT 1N	88	0_CHIP5_OUT 0N	13	1_CHIP5_OUT 1N	88	1_CHIP5_OUT 0N	13	1_CHIP5_OUT 1N	88	1_CHIP5_OUT 0N	13	1_CHIP8_OUT 1N
14	0_CHIP7_OUT 1P	87	0_CHIP7_OUT 0P	14	1_CHIP7_OUT 1P	87	1_CHIP7_OUT 0P	14	1_CHIP7_OUT 1P	87	1_CHIP7_OUT 0P	14	1_CHIP10_OUT 1P
15	0_CHIP7_OUT 1N	86	0_CHIP7_OUT 0N	15	1_CHIP7_OUT 1N	86	1_CHIP7_OUT 0N	15	1_CHIP7_OUT 1N	86	1_CHIP7_OUT 0N	15	1_CHIP10_OUT 1N
16	0_CHIP9_OUT 1P	85	0_CHIP9_OUT 0P	16	1_CHIP9_OUT 1P	85	1_CHIP9_OUT 0P	16	1_CHIP9_OUT 1P	85	1_CHIP9_OUT 0P	16	1_CHIP12_OUT 1P
17	0_CHIP9_OUT 1N	84	0_CHIP9_OUT 0N	17	1_CHIP9_OUT 1N	84	1_CHIP9_OUT 0N	17	1_CHIP9_OUT 1N	84	1_CHIP9_OUT 0N	17	1_CHIP12_OUT 1N
18	0_CHIP11_OUT 1P	83	0_CHIP11_OUT 0P	18	1_CHIP11_OUT 1P	83	1_CHIP11_OUT 0P	18	1_CHIP11_OUT 1P	83	1_CHIP11_OUT 0P	18	AGND
19	0_CHIP11_OUT 1N	82	0_CHIP11_OUT 0N	19	1_CHIP11_OUT 1N	82	1_CHIP11_OUT 0N	19	1_CHIP11_OUT 1N	82	1_CHIP11_OUT 0N	19	AGND
20	0_CHIP13_OUT 1P	81	0_CHIP13_OUT 0P	20	1_CHIP13_OUT 1P	81	1_CHIP13_OUT 0P	20	1_CHIP13_OUT 1P	81	1_CHIP13_OUT 0P	20	AGND
21	0_CHIP13_OUT 1N	80	0_CHIP13_OUT 0N	21	1_CHIP13_OUT 1N	80	1_CHIP13_OUT 0N	21	1_CHIP13_OUT 1N	80	1_CHIP13_OUT 0N	21	AGND
22	DGND	79	AGND	22	AGND	79	DGND	22	AGND	79	DGND	22	AGND
23	DGND	78	AGND	23	AGND	78	DGND	23	AGND	78	DGND	23	+2.5VA
24	0_CHIP6_OUT 1P	77	0_CHIP6_OUT 0P	24	1_CHIP6_OUT 1P	77	1_CHIP6_OUT 0P	24	+2.5VA	77	+2.5VD	24	+2.5VA
25	0_CHIP6_OUT 1N	76	0_CHIP6_OUT 0N	25	1_CHIP6_OUT 1N	76	1_CHIP6_OUT 0N	25	+2.5VA	76	+2.5VD	25	+2.5VA
26	0_CHIP8_OUT 1P	75	0_CHIP8_OUT 0P	26	1_CHIP8_OUT 1P	75	1_CHIP8_OUT 0P	26	+2.5VA	75	+2.5VD	26	+2.5VA
27	0_CHIP8_OUT 1N	74	0_CHIP8_OUT 0N	27	1_CHIP8_OUT 1N	74	1_CHIP8_OUT 0N	27	+2.5VA	74	+2.5VD	27	+2.5VA
28	0_CHIP10_OUT 1P	73	0_CHIP10_OUT 0P	28	1_CHIP10_OUT 1P	73	1_CHIP10_OUT 0P	28	AGND	73	DGND	28	+2.5VA
29	0_CHIP10_OUT 1N	72	0_CHIP10_OUT 0N	29	1_CHIP10_OUT 1N	72	1_CHIP10_OUT 0N	29	AGND	72	DGND	29	AGND
30	0_CHIP12_OUT 1P	71	0_CHIP12_OUT 0P	30	1_CHIP12_OUT 1P	71	1_CHIP12_OUT 0P	30	0_CHIP13_OUT 0N	71	0_CHIP13_OUT 1N	30	AGND
31	0_CHIP12_OUT 1N	70	0_CHIP12_OUT 0N	31	1_CHIP12_OUT 1N	70	1_CHIP12_OUT 0N	31	0_CHIP13_OUT 0P	70	0_CHIP13_OUT 1P	31	AGND
32	DGND	69	AGND	32	AGND	69	DGND	32	0_CHIP11_OUT 0N	69	0_CHIP11_OUT 1N	32	AGND
33	DGND	68	AGND	33	AGND	68	DGND	33	0_CHIP11_OUT 0P	68	0_CHIP11_OUT 1P	33	AGND
34	0_SC_OUT0n	67	0_OUT_CLK0n	34	1_OUT_CLK1n	67	1_SC_OUT1n	34	0_CHIP9_OUT 0N	67	0_CHIP9_OUT 1N	34	0_CHIP12_OUT 0N
35	0_SC_OUT0p	66	0_OUT_CLK0p	35	1_OUT_CLK1p	66	1_SC_OUT1p	35	0_CHIP9_OUT 0P	66	0_CHIP9_OUT 1P	35	0_CHIP12_OUT 0P
36	DGND	65	0_BCO_CLK0n	36	1_BCO_CLK1n	65	DGND	36	0_CHIP7_OUT 0N	65	0_CHIP7_OUT 1N	36	0_CHIP10_OUT 0N
37	DGND	64	0_BCO_CLK0p	37	1_BCO_CLK1p	64	DGND	37	0_CHIP7_OUT 0P	64	0_CHIP7_OUT 1P	37	0_CHIP10_OUT 0P
38	DGND	63	0_SC_IN0n	38	1_SC_IN1n	63	DGND	38	0_CHIP5_OUT 0N	63	0_CHIP5_OUT 1N	38	0_CHIP8_OUT 0N
39	DGND	62	0_SC_IN0p	39	1_SC_IN1p	62	DGND	39	0_CHIP5_OUT 0P	62	0_CHIP5_OUT 1P	39	0_CHIP8_OUT 0P
40	DGND	61	0_RESET0n	40	1_RESET1n	61	DGND	40	AGND	61	DGND	40	0_CHIP6_OUT 0N
41	DGND	60	0_RESET0p	41	1_RESET1p	60	DGND	41	CAL_INJECT0	60	DGND	41	0_CHIP6_OUT 0P
42	DGND	59	AGND	42	AGND	59	DGND	42	0_CHIP4_OUT 0N	59	0_CHIP4_OUT 1N	42	DGND
43	DGND	58	AGND	43	AGND	58	DGND	43	0_CHIP4_OUT 0P	58	0_CHIP4_OUT 1P	43	DGND
44	+2.5VA	57	AGND	44	+2.5VD	57	+2.5VD	44	0_CHIP3_OUT 0N	57	0_CHIP3_OUT 1N	44	OUT_CLK0n
45	+2.5VA	56	AGND	45	+2.5VD	56	+2.5VD	45	0_CHIP3_OUT 0P	56	0_CHIP3_OUT 1P	45	OUT_CLK0p
46	+2.5VA	55	+2.5VA	46	+2.5VD	55	+2.5VD	46	0_CHIP2_OUT 0N	55	0_CHIP2_OUT 1N	46	DGND
47	+2.5VA	54	+2.5VA	47	+2.5VD	54	+2.5VD	47	0_CHIP2_OUT 0P	54	0_CHIP2_OUT 1P	47	DGND
48	+2.5VA	53	+2.5VA	48	+2.5VD	53	+2.5VD	48	0_CHIP1_OUT 0N	53	0_CHIP1_OUT 1N	48	SC_IN0p
49	+2.5VA	52	+2.5VA	49	+2.5VD	52	+2.5VD	49	0_CHIP1_OUT 0P	52	0_CHIP1_OUT 1P	49	SC_IN0n
50	+2.5VA	51	+2.5VA	50	+2.5VD	51	+2.5VD	50	AGND	51	DGND	50	AGND

信号ライン
問題なし!

CN50を用いた導通測定(AC用)

1. まずACタイプのFPCを使って、HARNES CHECKERのリファレンスファイルを作成し、登録する。
2. マイクロ同軸ケーブルをつなげ、測定する。
→FPCのチャンネルマップ通りに導通していればOKとなる。

測定方法



結果

AC用では、マイクロ同軸ケーブルはFPCと同じチャンネルマップであることがわかった。

また導通チェックをしたBD用マイクロ同軸ケーブルのチャンネルマップをCN50に登録した。今後、BD用はこれをもとに導通チェックを行う。