

# Test Bench LV Rack Configuration

# General Instructions

To be developed

**INTT LV system**

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**Introduction** [edit | edit source]

The INTT LV voltage system is using the Switch distribution board and LV power supply to power up the ROC boards and chips. The Switch distribution board gives the power to ROC board and LV power supply, and then LV power supply gives the power to the chips. There is 13 slots for Switch distribution board in total, and 10 slots for LV power supply in total. Switch distribution board is controlled by the telnet command line, and the LV power supply is controlled by a perl script. Below shows how to use the telnet command line, the perl script to control the LV system, and also the cable connection.

**Bias voltage (HV)**

**Switch distribution board (Including ROC and chip)**

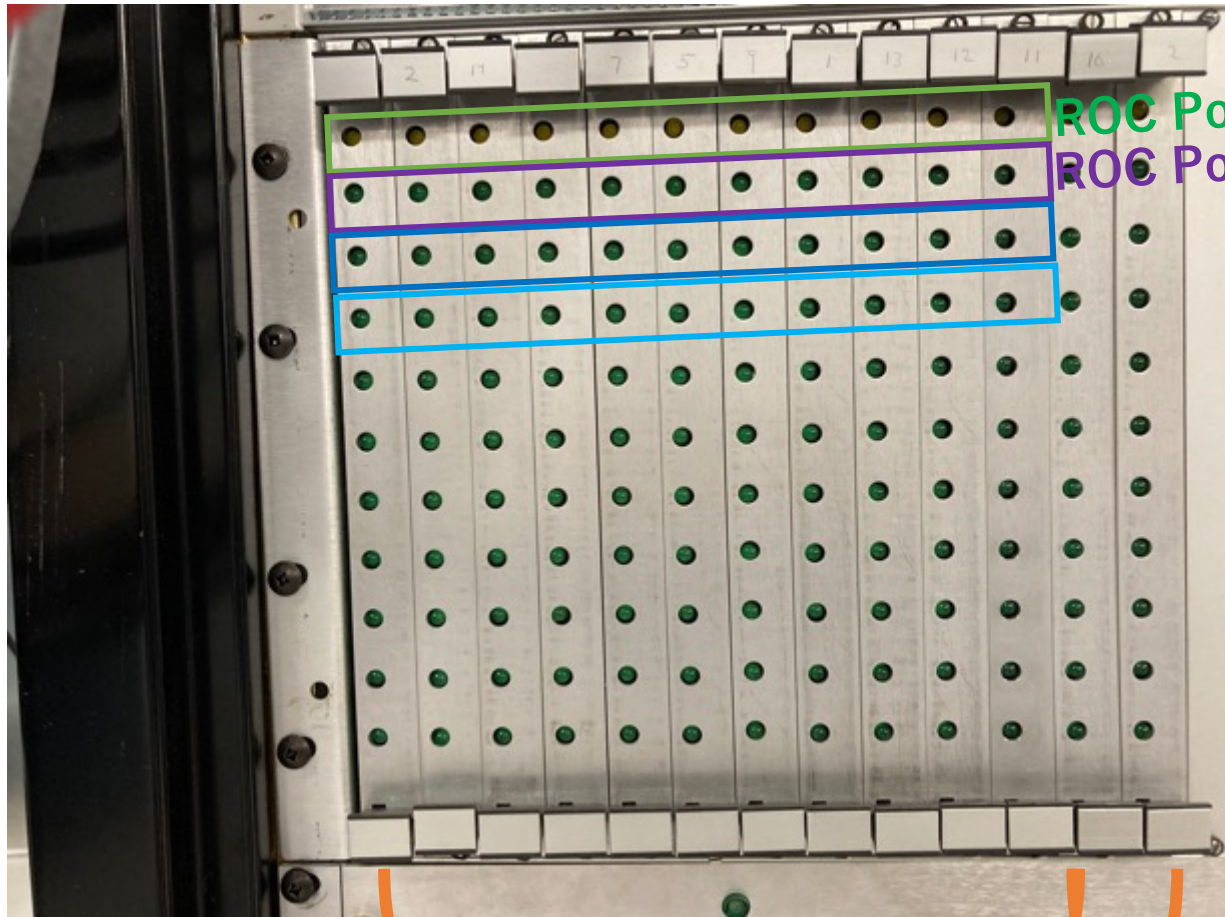
**LV power supply (power up chips)**

**HV filter**

**PC**

[https://wiki.sphenix.bnl.gov/index.php/INTT\\_LV\\_system](https://wiki.sphenix.bnl.gov/index.php/INTT_LV_system)

# 10-Channel LV Switching Module



ROC Power Cable-1  
ROC Power Cable-2

Slot 1~10 : ROC Power  
Slot 12,13 : FPHX Power via LANL boards

ROC Power

FPHX Power

ROC Power

# Test Bench Switching Module Channel Map

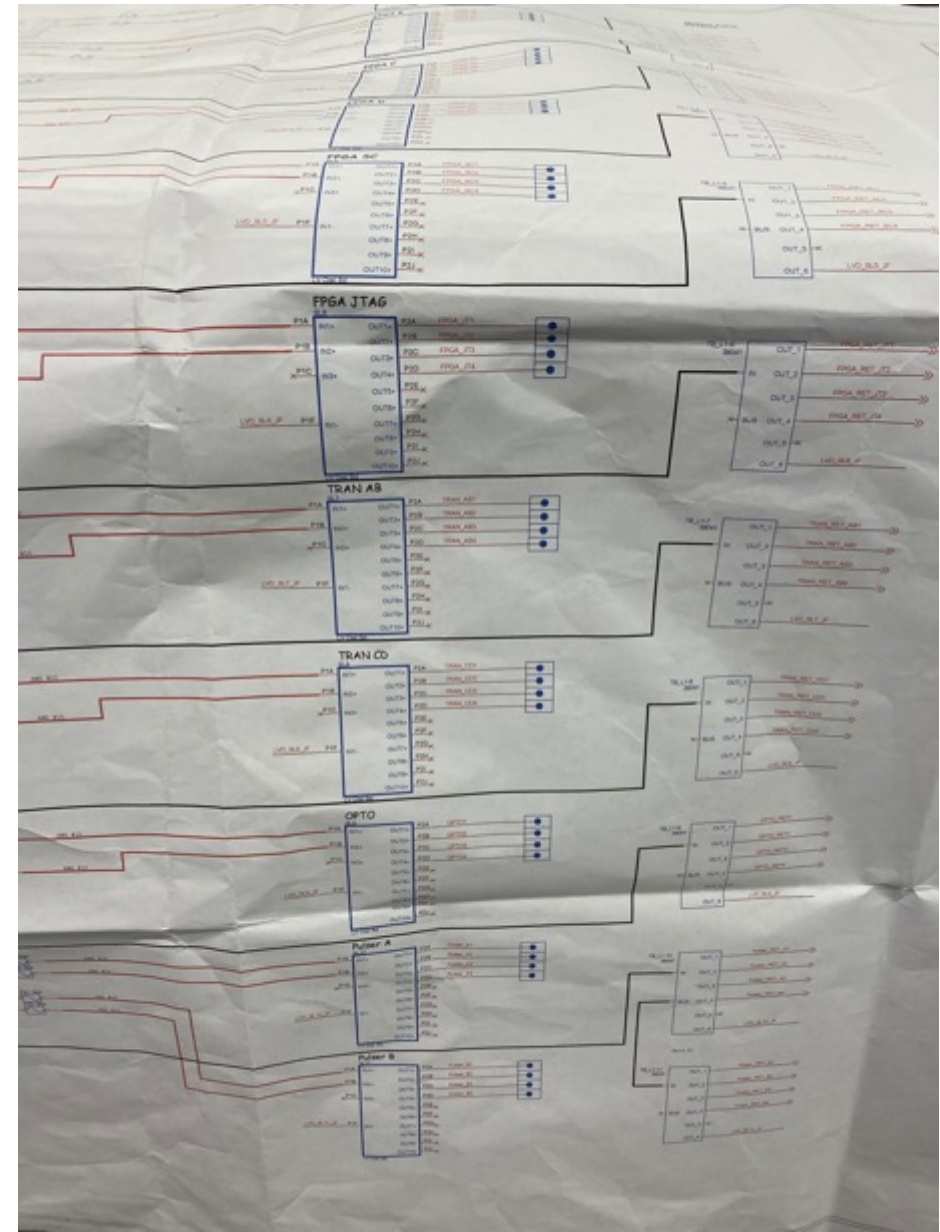
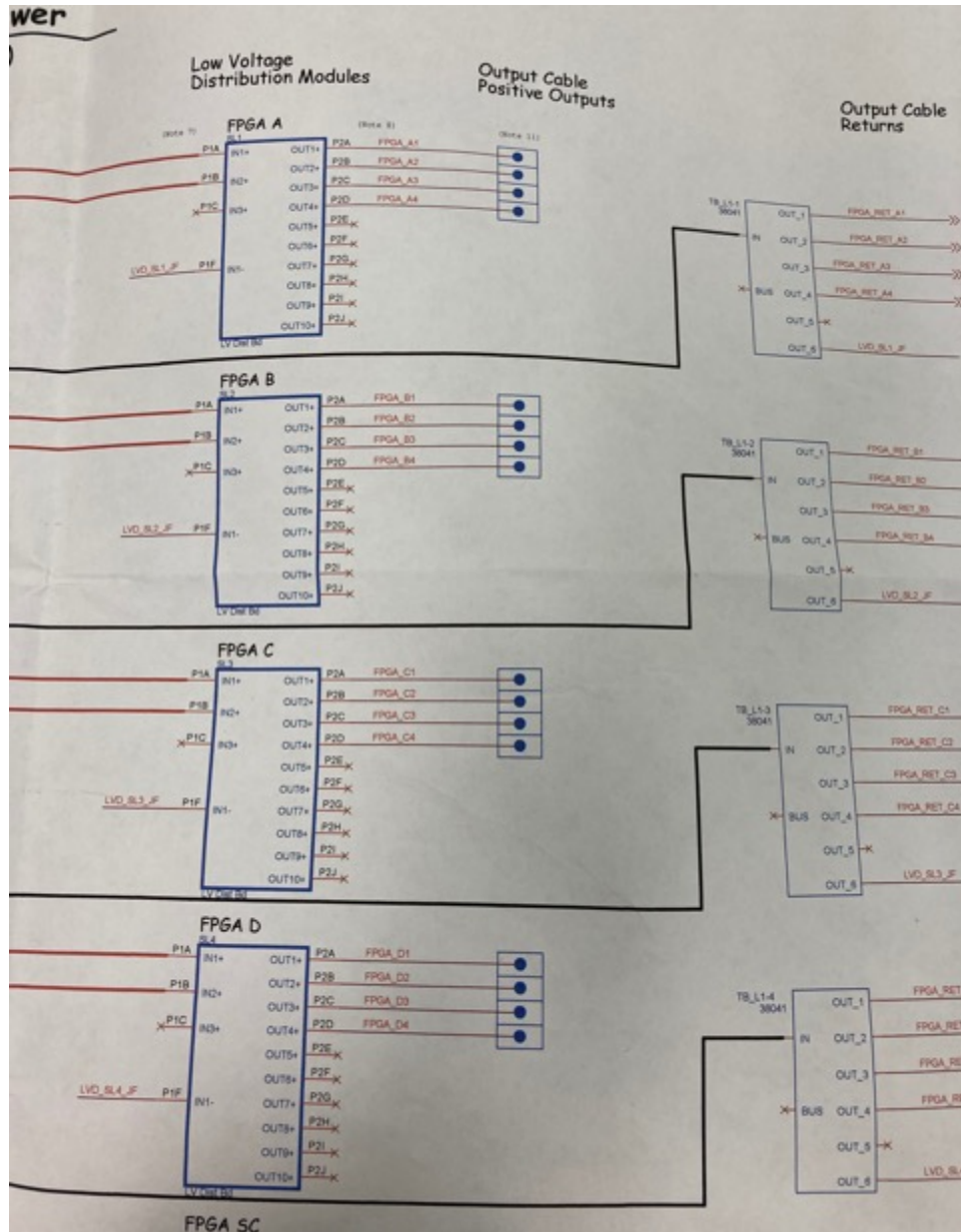
		Channel									
Slot	Destination	1	2	3	4	5	6	7	8	9	10
1	2.5V_FPGA_A	ROC1	ROC2	ROC3	ROC4					N/A	N/A
2	2.5V_FPGA_B	ROC1	ROC2	ROC3	ROC4					N/A	N/A
3	2.5V_FPGA_C	ROC1	ROC2	ROC3	ROC4					N/A	N/A
4	2.5V_FPGA_D	ROC1	ROC2	ROC3	ROC4					N/A	N/A
5	2.5V_FPGA_SC	ROC1	ROC2	ROC3	ROC4					N/A	N/A
6	2.5V_JTAG_FPGA	ROC1	ROC2	ROC3	ROC4					N/A	N/A
7	3.3V_FPGA_A_B_SC	ROC1	ROC2	ROC3	ROC4					N/A	N/A
8	3.3V_FPGA_C_D_BCO	ROC1	ROC2	ROC3	ROC4					N/A	N/A
9	5V_opto_iso	ROC1	ROC2	ROC3	ROC4					N/A	N/A
10	Pulser_5V_A	ROC1	ROC2	ROC3	ROC4					N/A	N/A
11	Pulser_5V_B	ROC1	ROC2	ROC3	ROC4					N/A	N/A
12	FPHX										
13	FPHX										

# LV Distribution Board – ROC power Channel Map

ROC Connector Bundle					10 Channel Switching Module		
Signal	Pin	Pin	Signal		Slot	Channel*	Channel*
gnd_5V	1	2	Pulser_5V_A		10	1	2
gnd_5V	3	4	Pulser_5V_B		11	1	2
	5	6					
gnd_2.5V	7	8	2.5V_FPGA_A		1	1	2
gnd_2.5V	9	10	2.5V_FPGA_B		2	1	2
gnd_2.5V	11	12	2.5V_FPGA_C		3	1	2
gnd_2.5V	13	14	2.5V_FPGA_D		4	1	2
gnd_2.5V	15	16	2.5V_FPGA_SC		5	1	2
gnd_3.3V	17	18	3.3V_FPGA_A_B_SC		7	1	2
gnd_3.3V	19	20	3.3V_FPGA_C_D_BCO		8	1	2
gnd_2.5V	21	22	2.5V_JTAG_FPGA		6	1	2
gnd_5V	23	24	5V_opto_iso		9	1	2
					ROC Power Cable	1	2

# Test Bench Rack Schematics

ROC Power

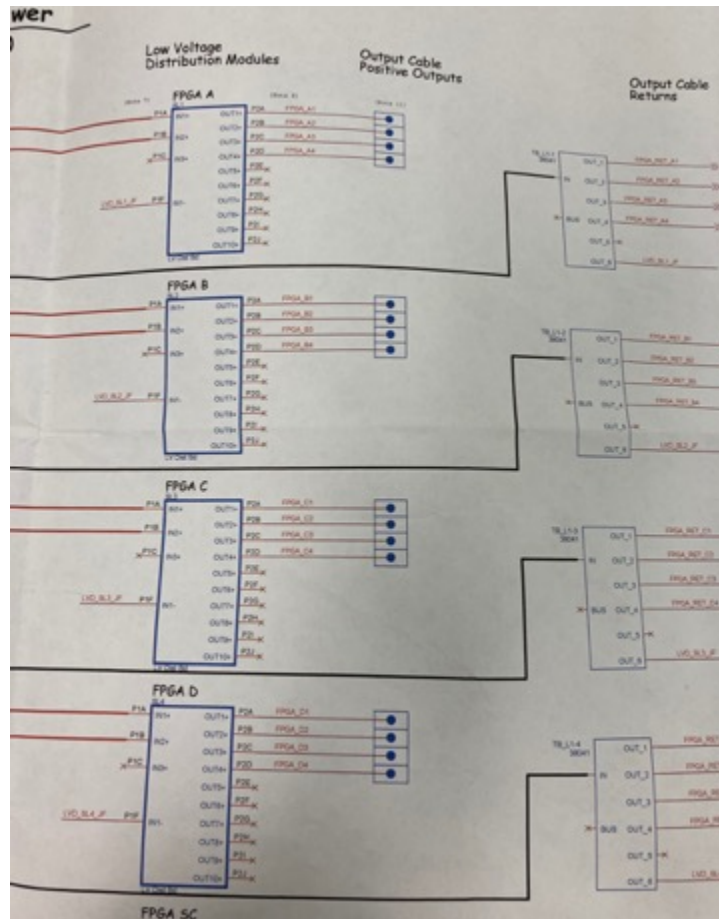




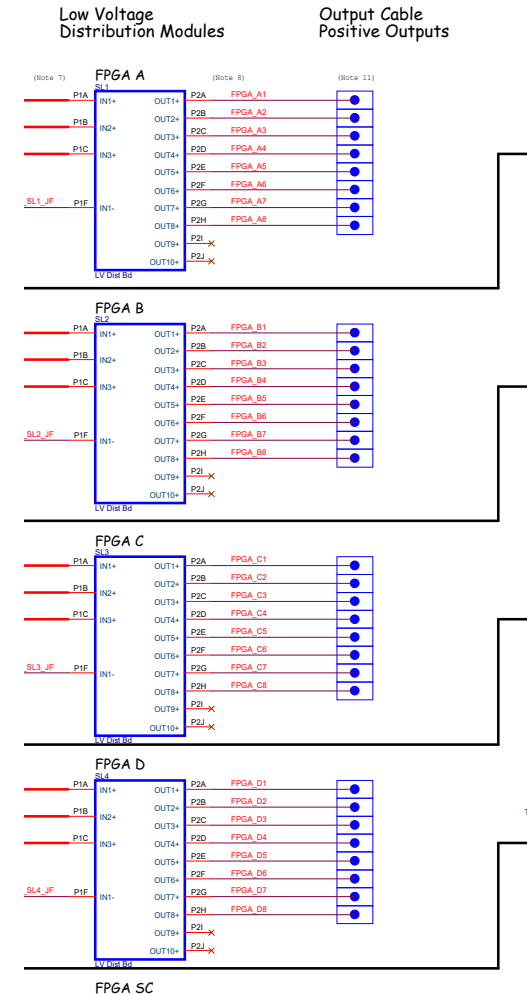




# ROC Power Schematic Drawing



Test Bench Version



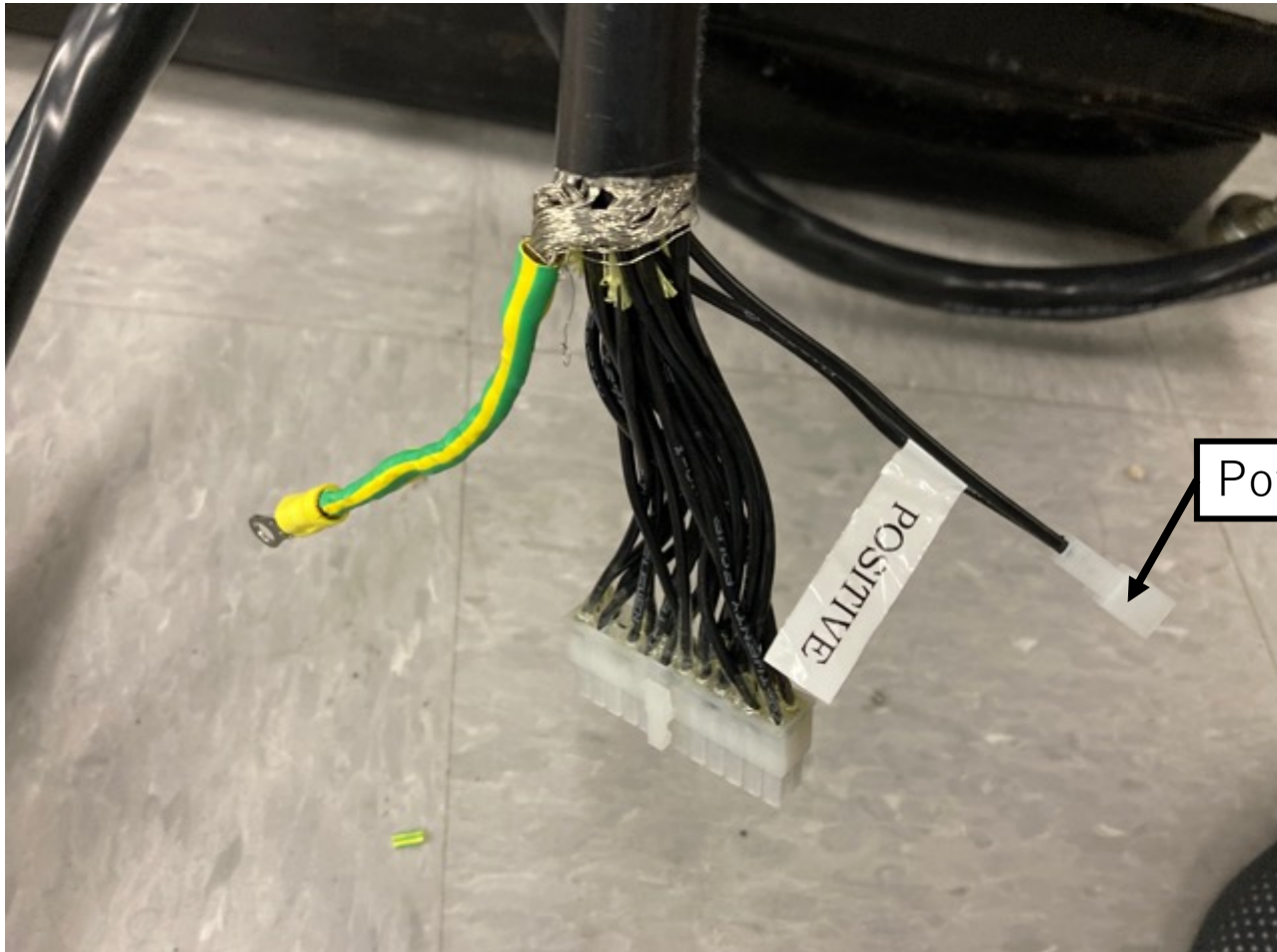
1008 Rack Version

The channel map of the test bench version is fewer channel version of 1008. GUI can be developed and being tested at the test bench rack.

# 1008 Switching Module Channel Map

		Channel									
Slot	Destination	1	2	3	4	5	6	7	8	9	10
1	2.5V_FPGA_A	ROC1	ROC2	ROC3	ROC4	ROC5	ROC6	ROC7	ROC8	N/A	N/A
2	2.5V_FPGA_B	ROC1	ROC2	ROC3	ROC4	ROC5	ROC6	ROC7	ROC8	N/A	N/A
3	2.5V_FPGA_C	ROC1	ROC2	ROC3	ROC4	ROC5	ROC6	ROC7	ROC8	N/A	N/A
4	2.5V_FPGA_D	ROC1	ROC2	ROC3	ROC4	ROC5	ROC6	ROC7	ROC8	N/A	N/A
5	2.5V_FPGA_SC	ROC1	ROC2	ROC3	ROC4	ROC5	ROC6	ROC7	ROC8	N/A	N/A
6	2.5V_JTAG_FPGA	ROC1	ROC2	ROC3	ROC4	ROC5	ROC6	ROC7	ROC8	N/A	N/A
7	3.3V_FPGA_A_B_SC	ROC1	ROC2	ROC3	ROC4	ROC5	ROC6	ROC7	ROC8	N/A	N/A
8	3.3V_FPGA_C_D_BCO	ROC1	ROC2	ROC3	ROC4	ROC5	ROC6	ROC7	ROC8	N/A	N/A
9	5V_opto_iso	ROC1	ROC2	ROC3	ROC4	ROC5	ROC6	ROC7	ROC8	N/A	N/A
10	Pulser_5V_A	ROC1	ROC2	ROC3	ROC4	ROC5	ROC6	ROC7	ROC8	N/A	N/A
11	Pulser_5V_B	ROC1	ROC2	ROC3	ROC4	ROC5	ROC6	ROC7	ROC8	N/A	N/A
12	FPHX										
13	FPHX										

# Power for Beam Clock Cable



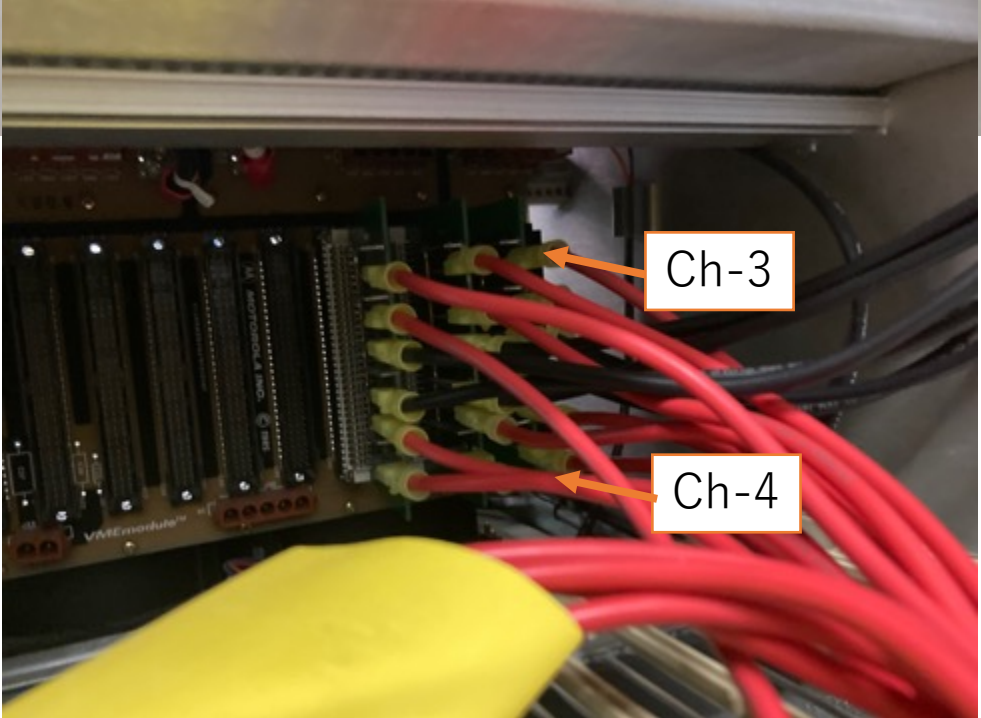
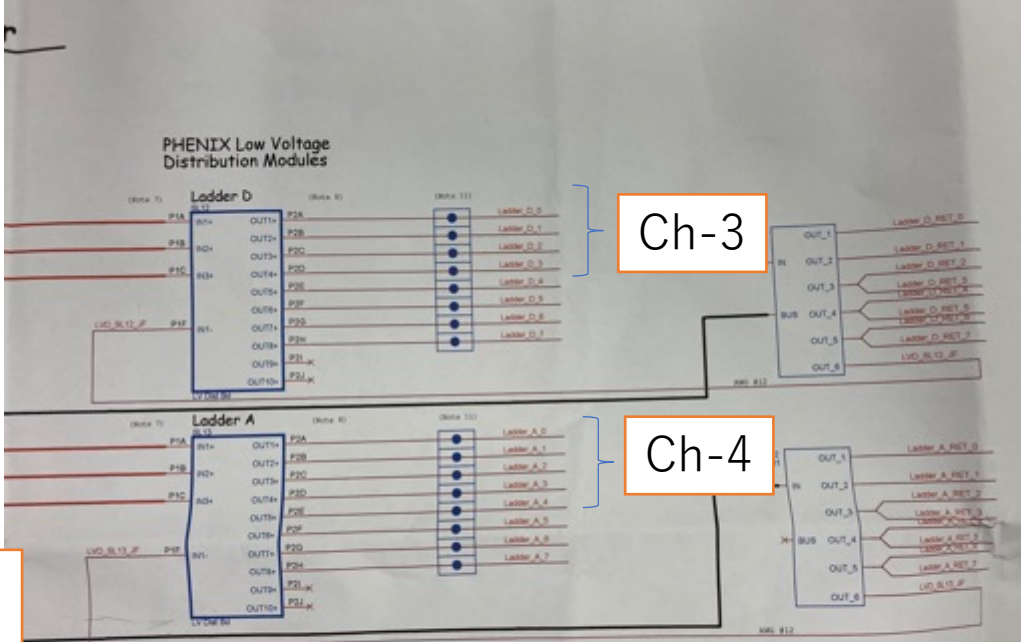
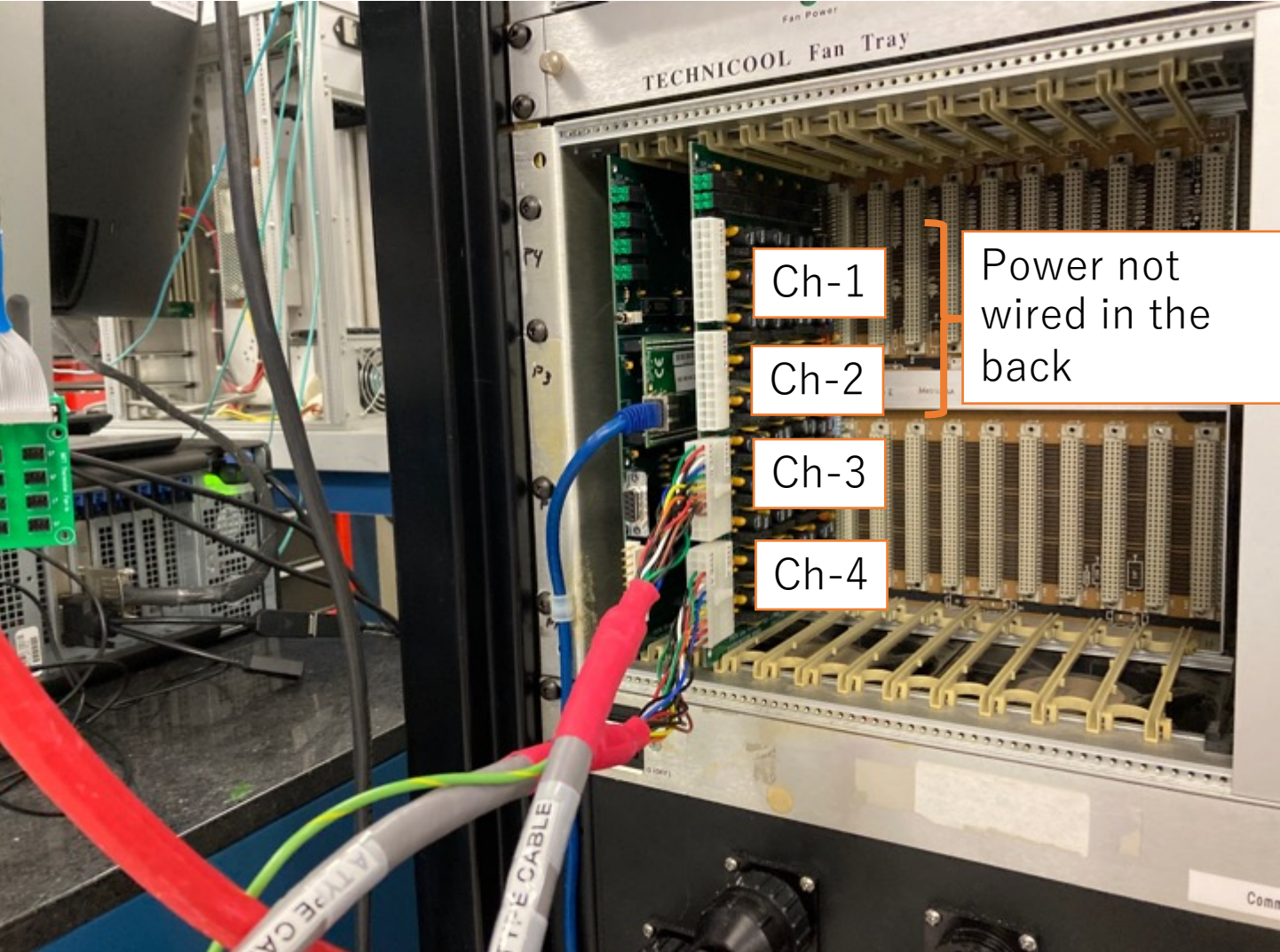
Power Cable for a Beam Clock Board

Not yet sure which channel of switching module from.

FPHX Power

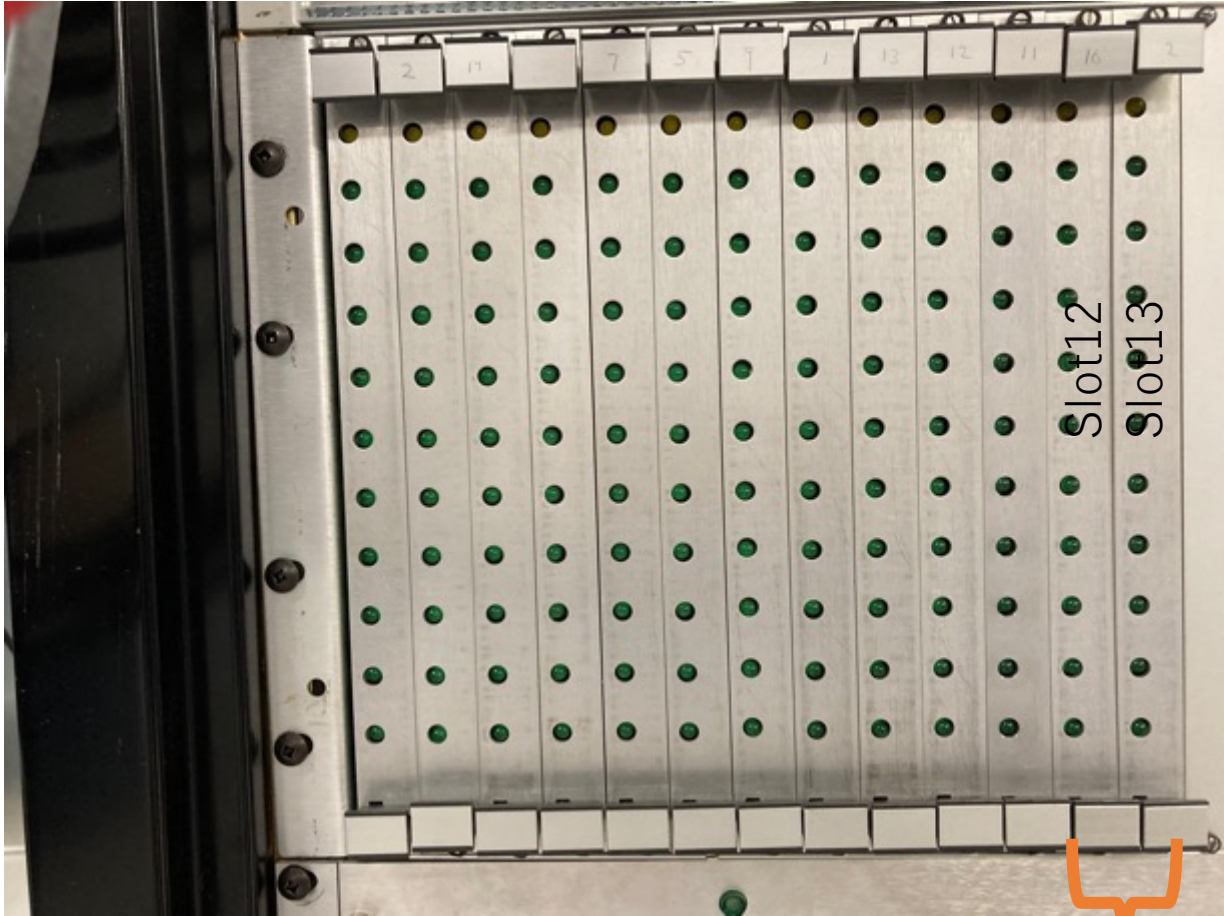


# FPHX Power Crate



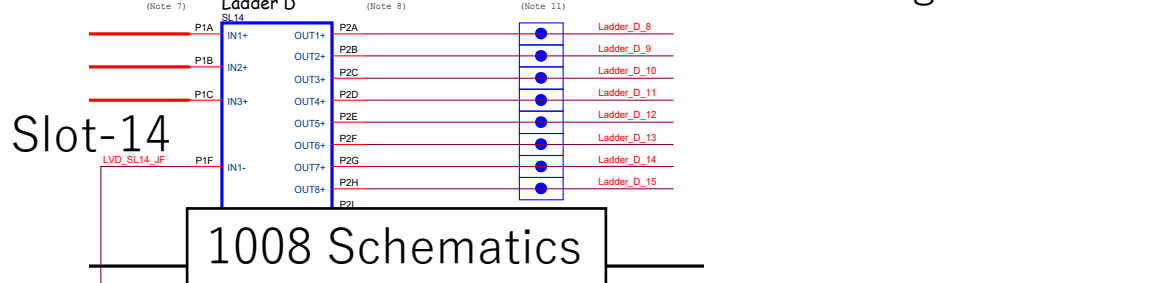
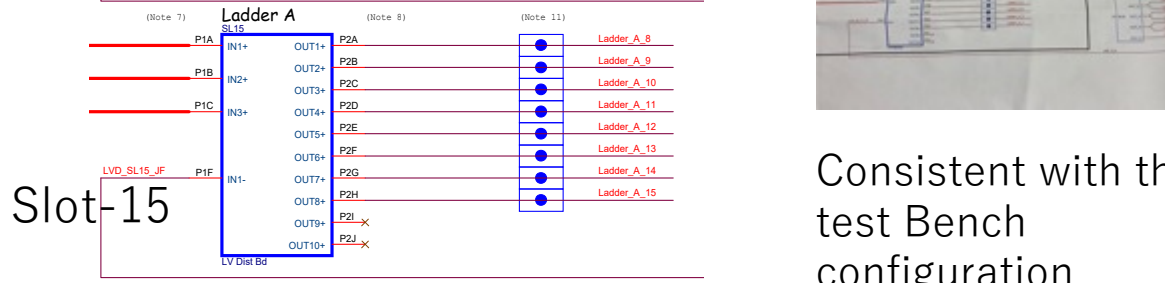
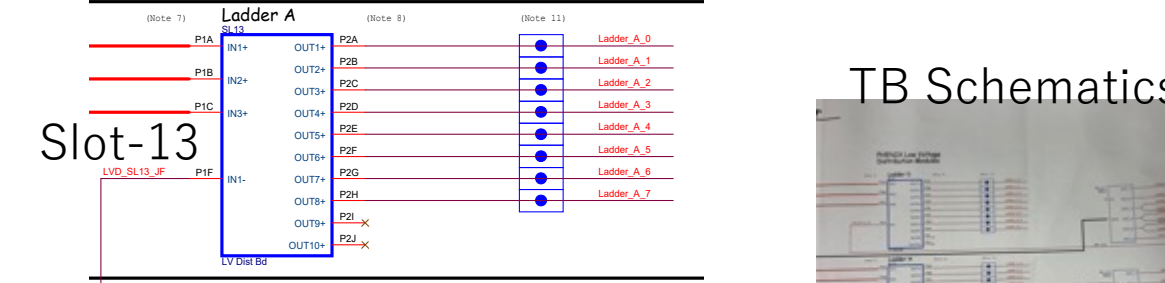
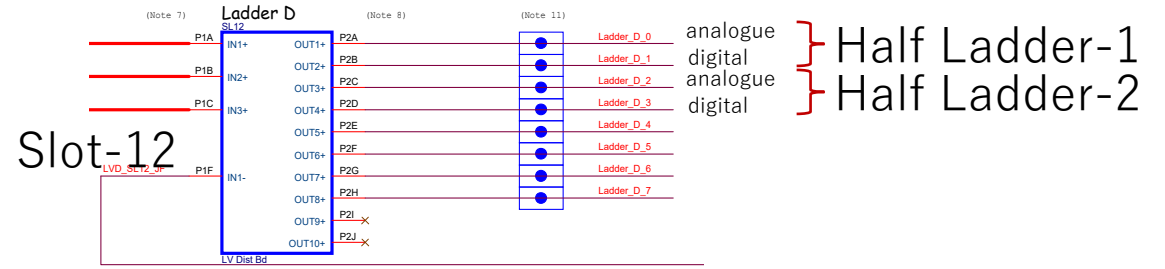
This channel map is assumption. Needs to be confirmed.

# FPHX Power Switching Module Map

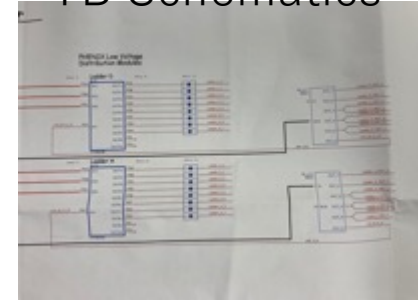


FPHX

PHENIX Low Voltage Distribution Modules



TB Schematics



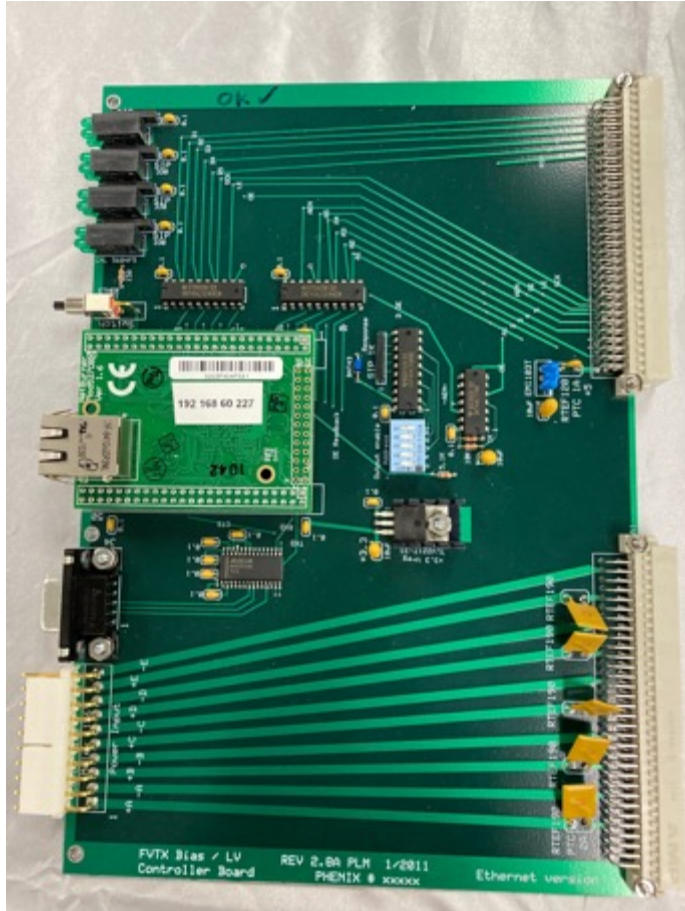
Consistent with the test Bench configuration



# FVTX Bias/LV Controller Boards

TIPs: we can ping these card from the inttpower machine, but not from felix2 server for unknown reason.

## Controller Board-1



**192.168.60.227**

## Controller Board-2

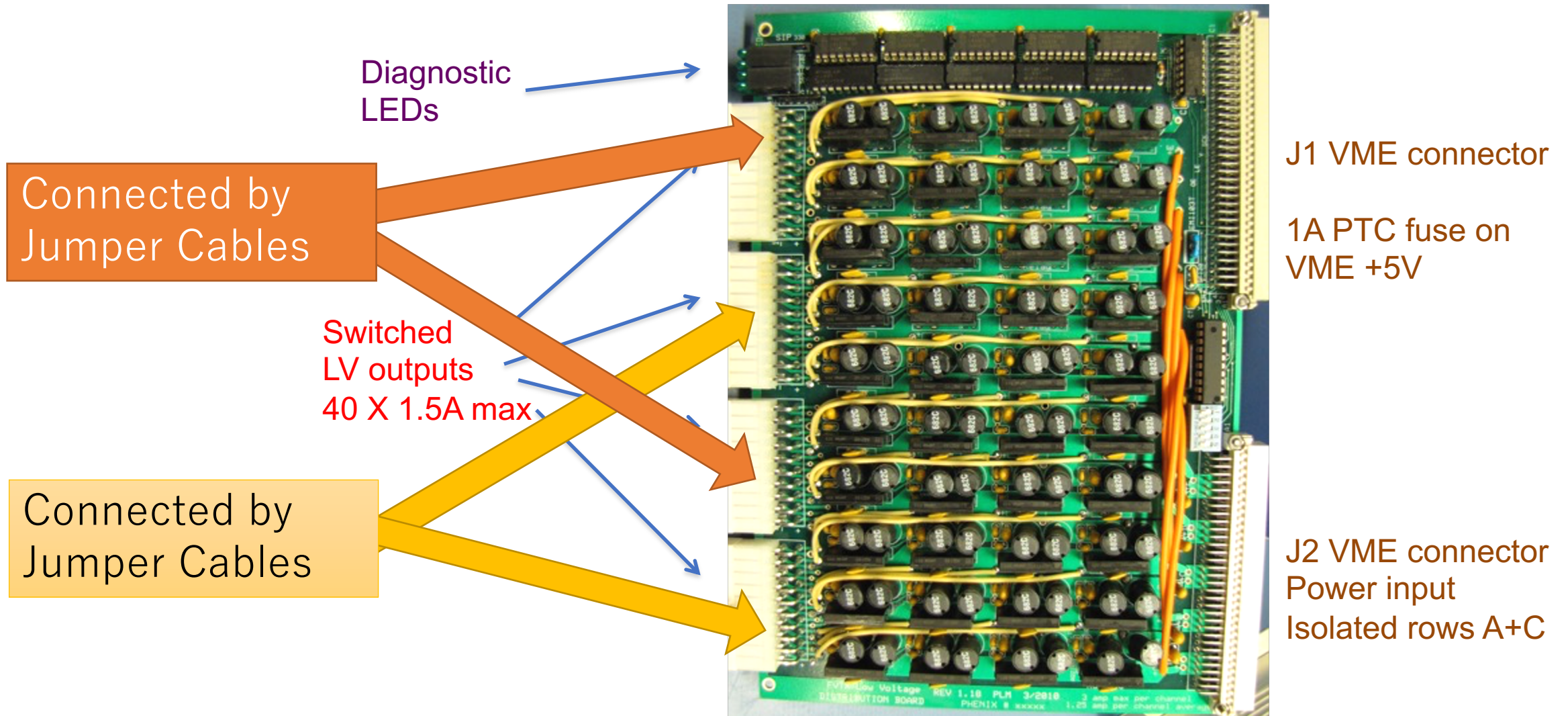


**\*192.168.60.1**

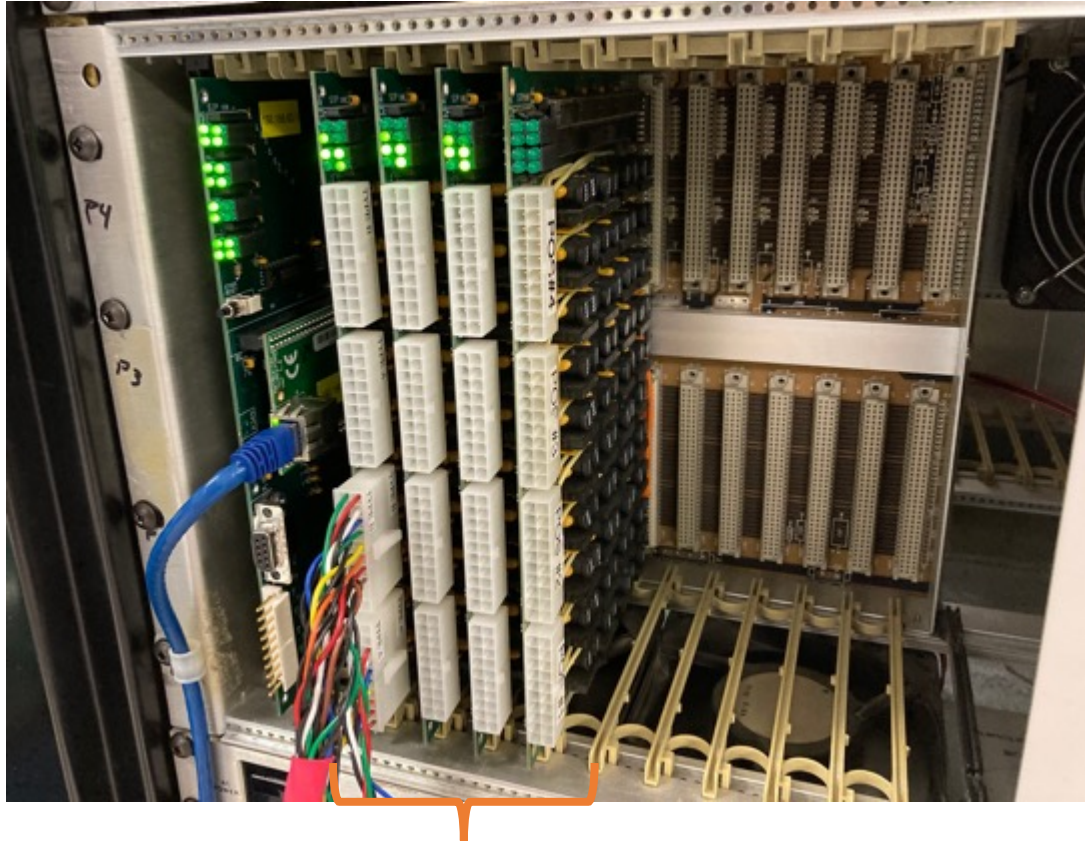
\*This IP address is found by Genki's IP address scan



# 40 Channel LV FPHX Distribution VME Card



# FEM Power Status



40 channel FPHX distribution cards

- The power output is only observed with the controller board-1. The controller board-2 doesn't allow any output voltage from the FPHX distribution boards.

# New Policy for the INTT Power

In order to avoid messy home directory

- Account :
  - intt : for operation
  - inttdev : for developers