Development of LVDS terminator

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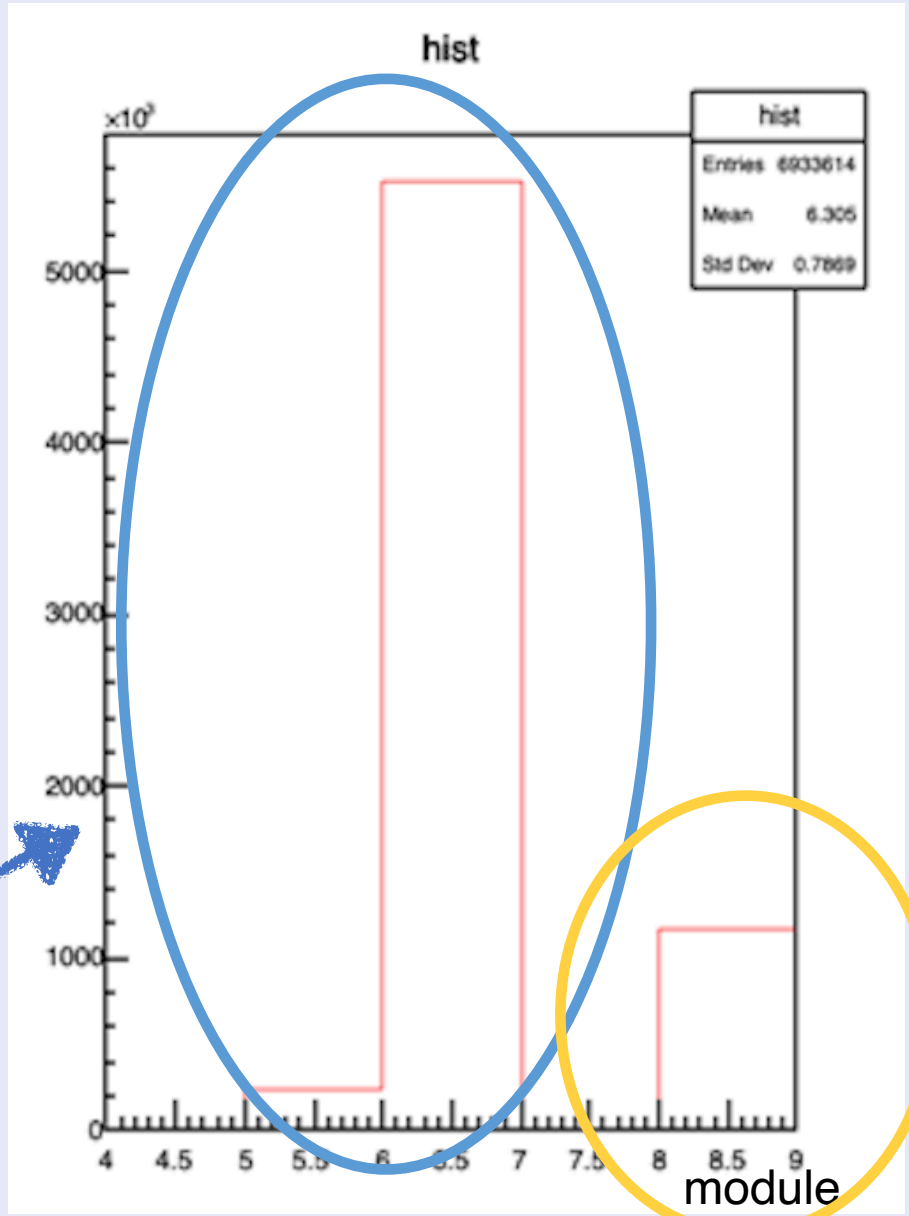
Fake hits Issue

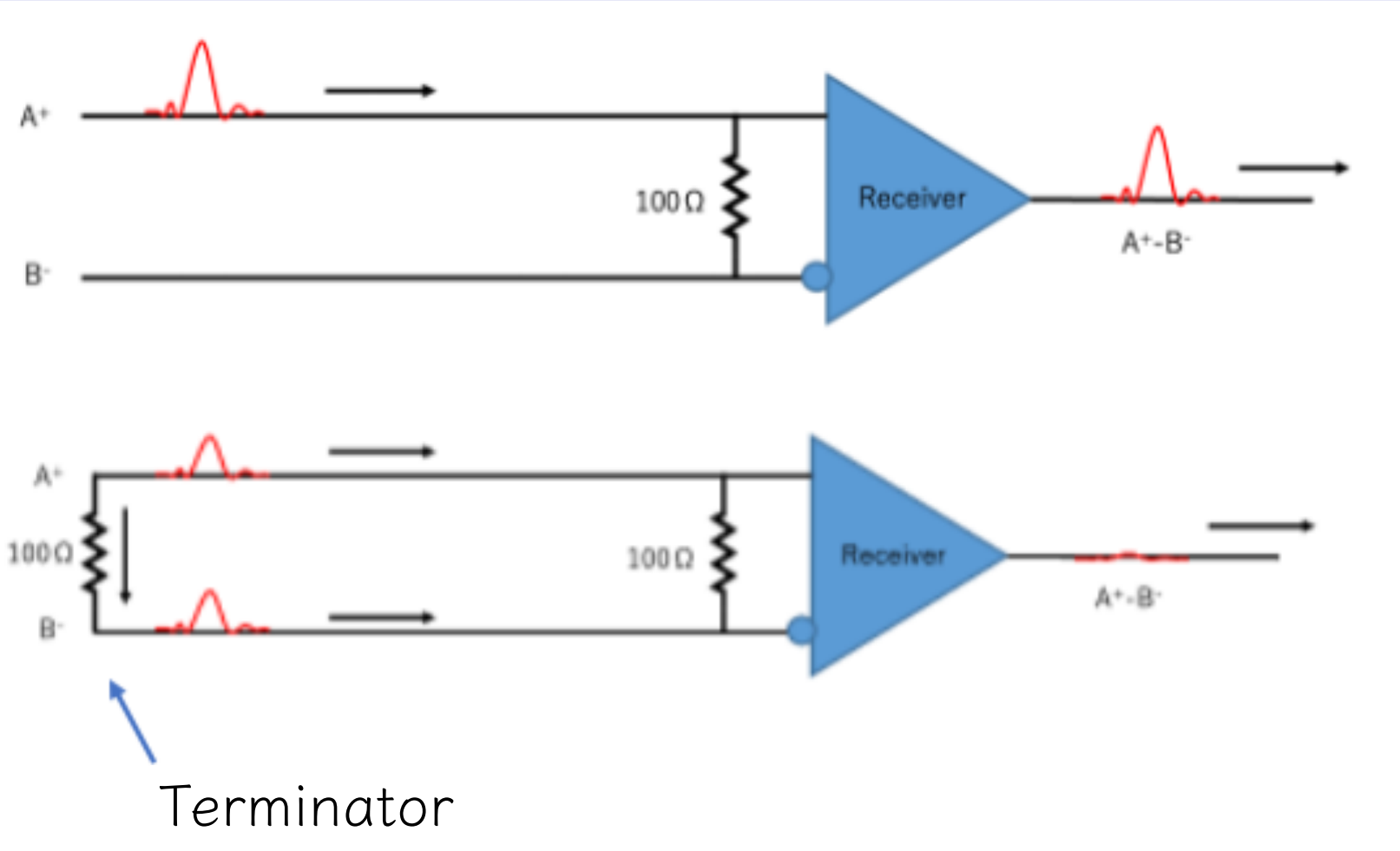


Fake hits are mixed in with the data.

Fake hits

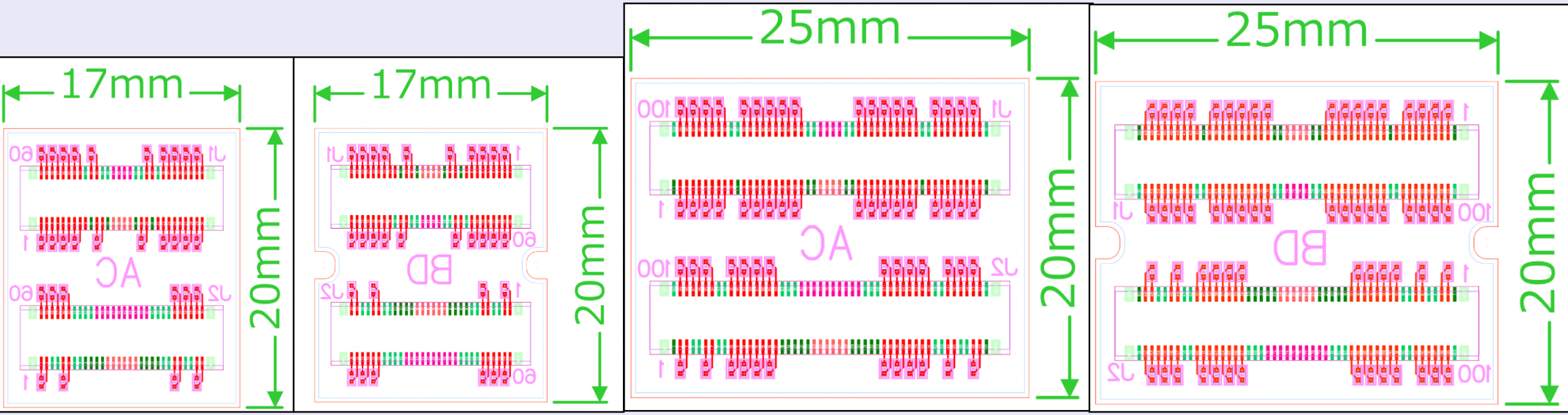
connected to portA1

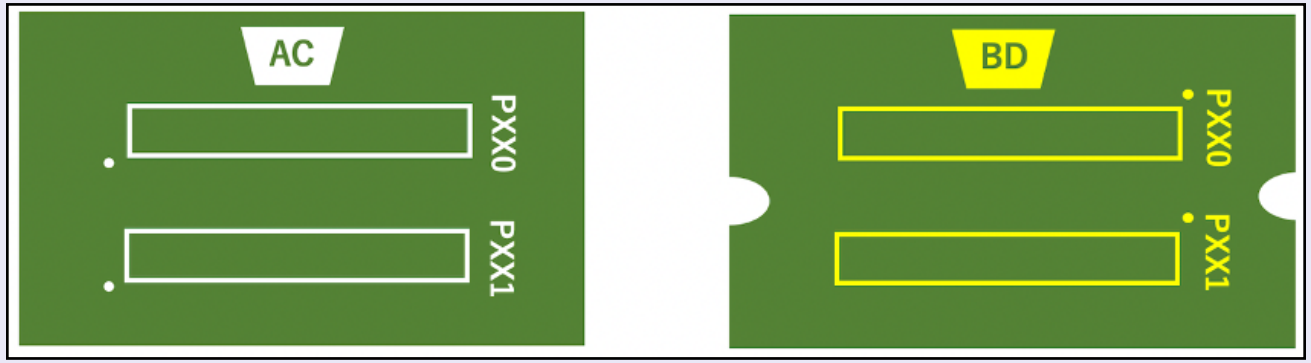
hypothesis



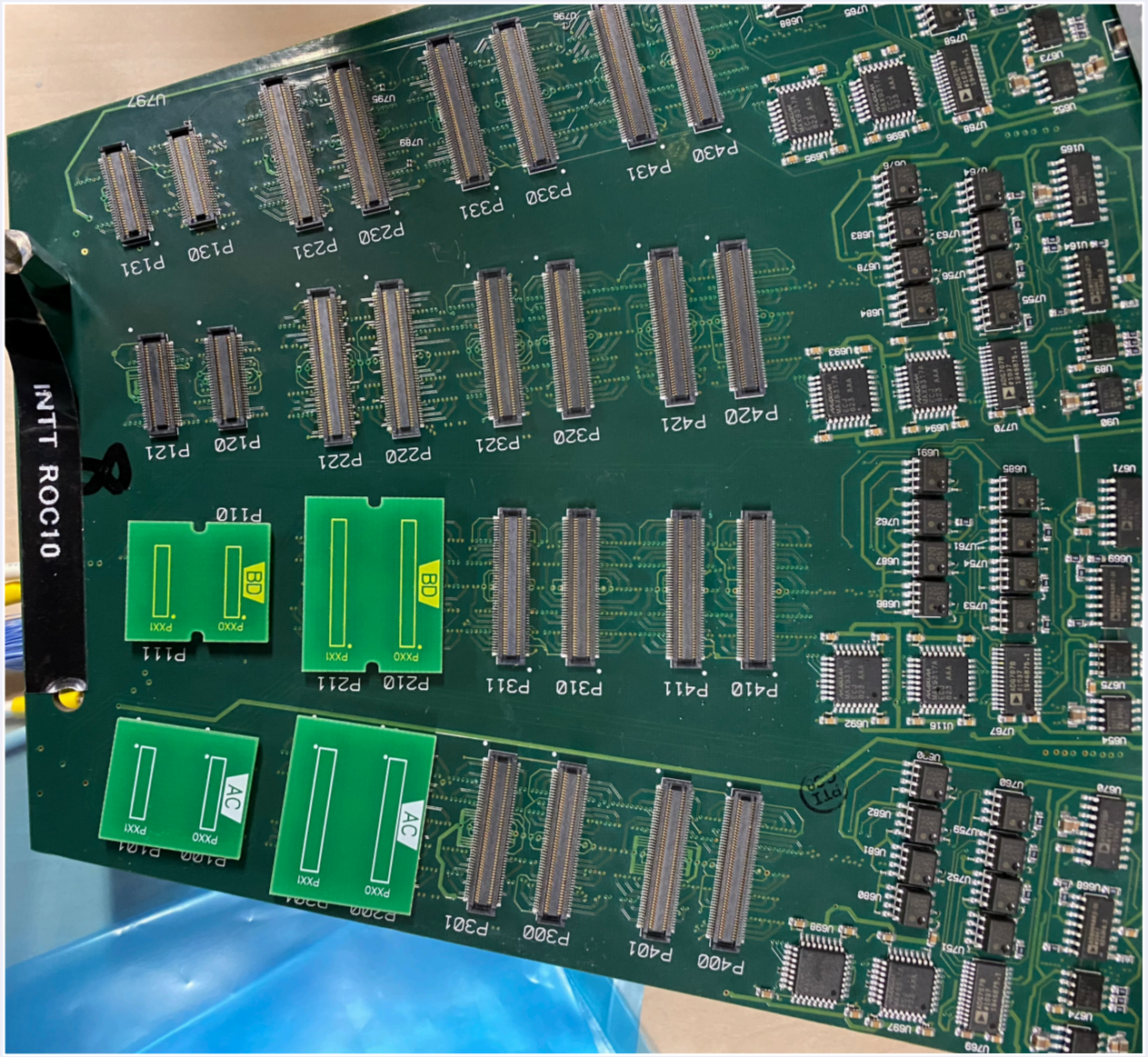
By attaching a terminator at the open end,
we intend to common-mode the noise and cancel it out.

LVDS Terminator prototype





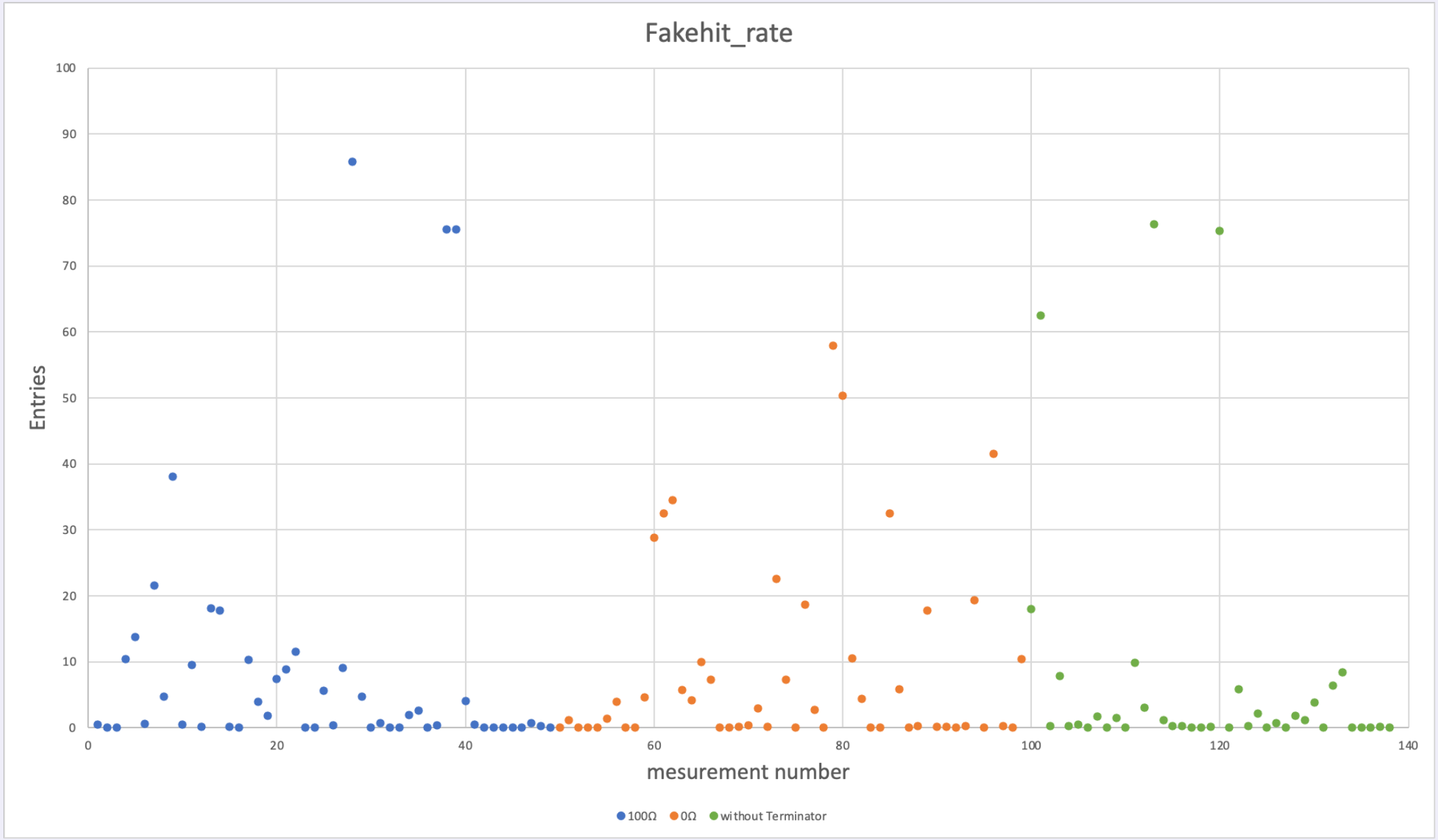
Experiment



Calibration tests were conducted about 50 times each, and data analysis was conducted.

Two types of termination resistors,
100 Ω and 0 Ω were made as prototypes.

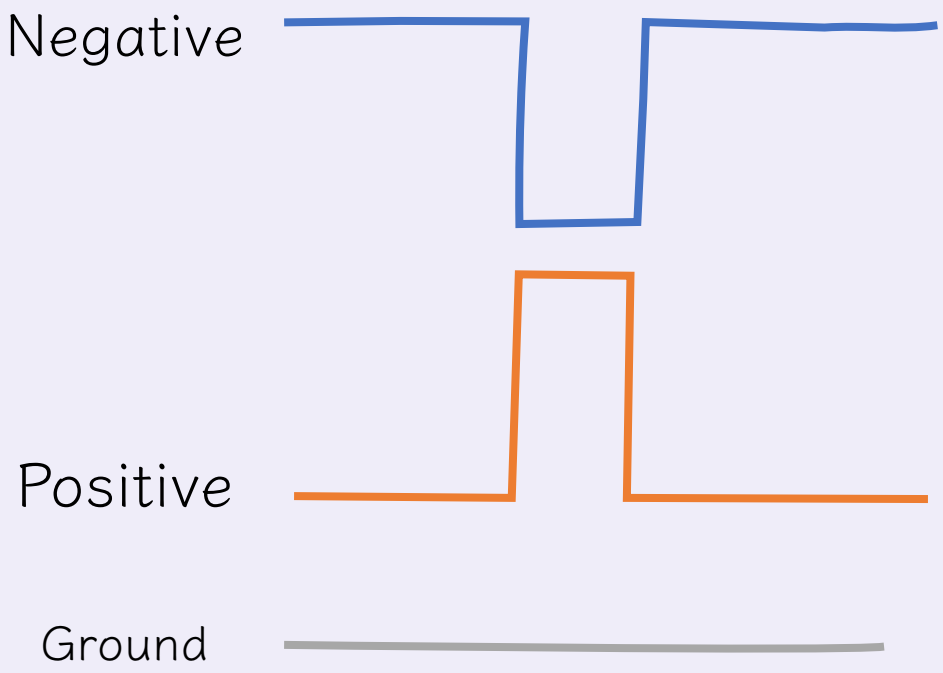
Analysis


Fakehit_rate
Entries
mesurement number
100Ω
0Ω
without Terminator

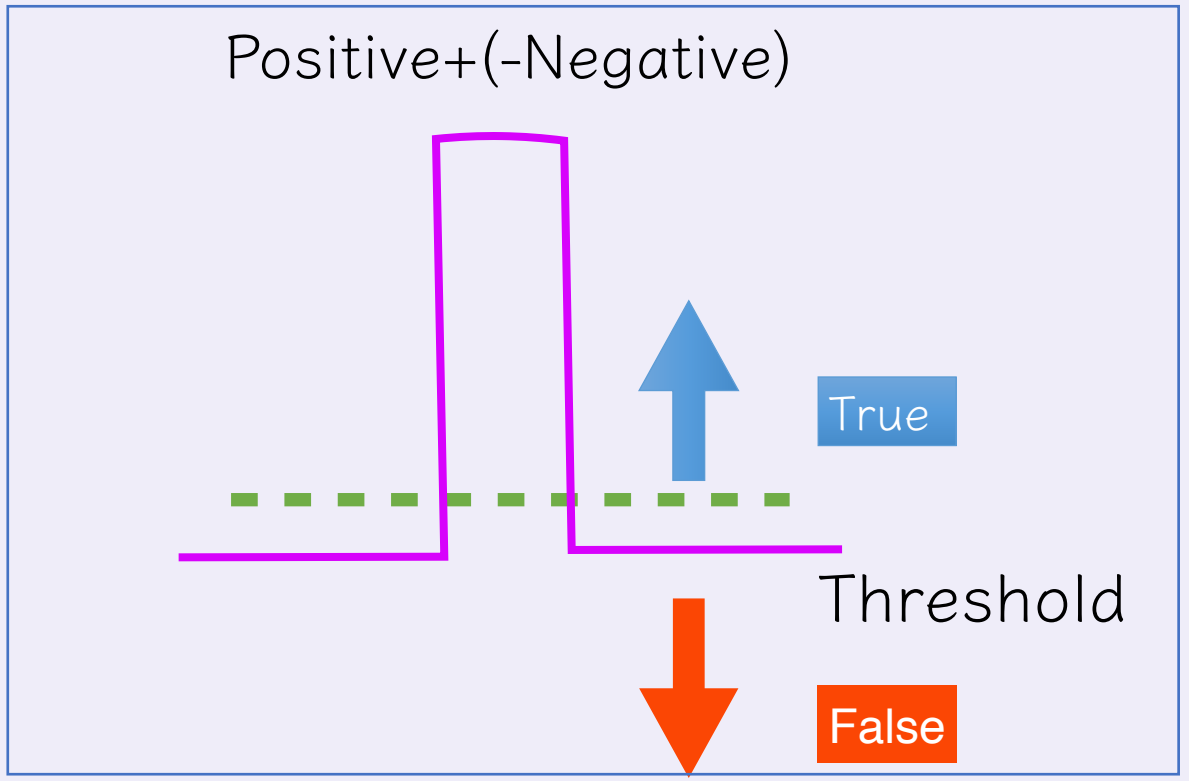
Proposed new terminator

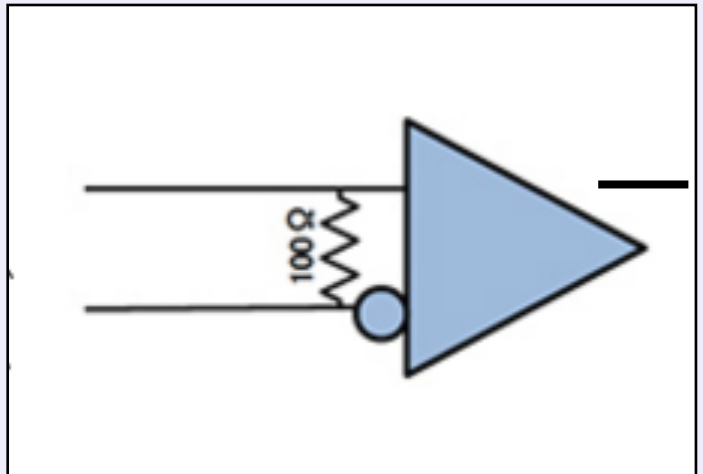
New Hypothesis

Normal(Cable is connected)



Receiver



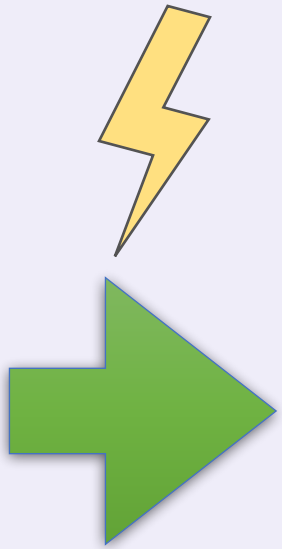


New Hypothesis

Cable is not connected

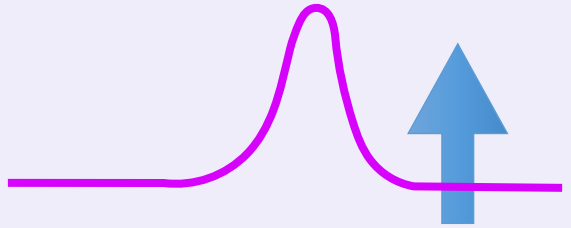
Negative ?V

Positive ?V



Receiver

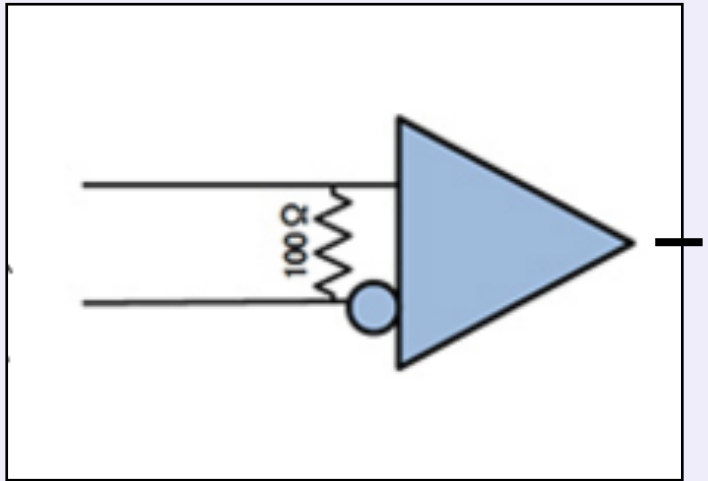
Positive+(-Negative)



True

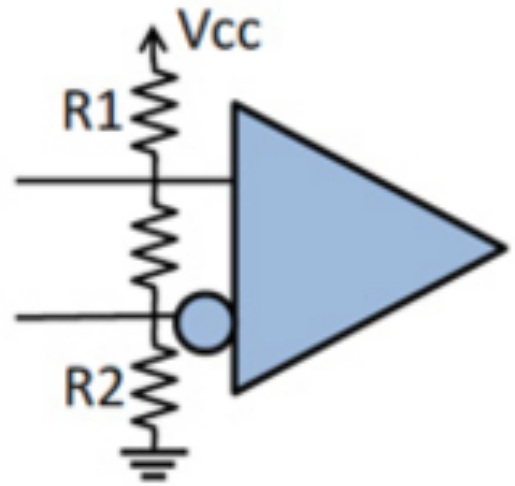
Threshold

False



Voltage is unstable

Proposal



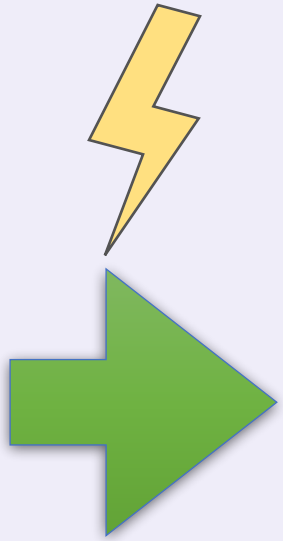
provide potential difference

Connect the positive and negative lines to Vcc and GND via resistors

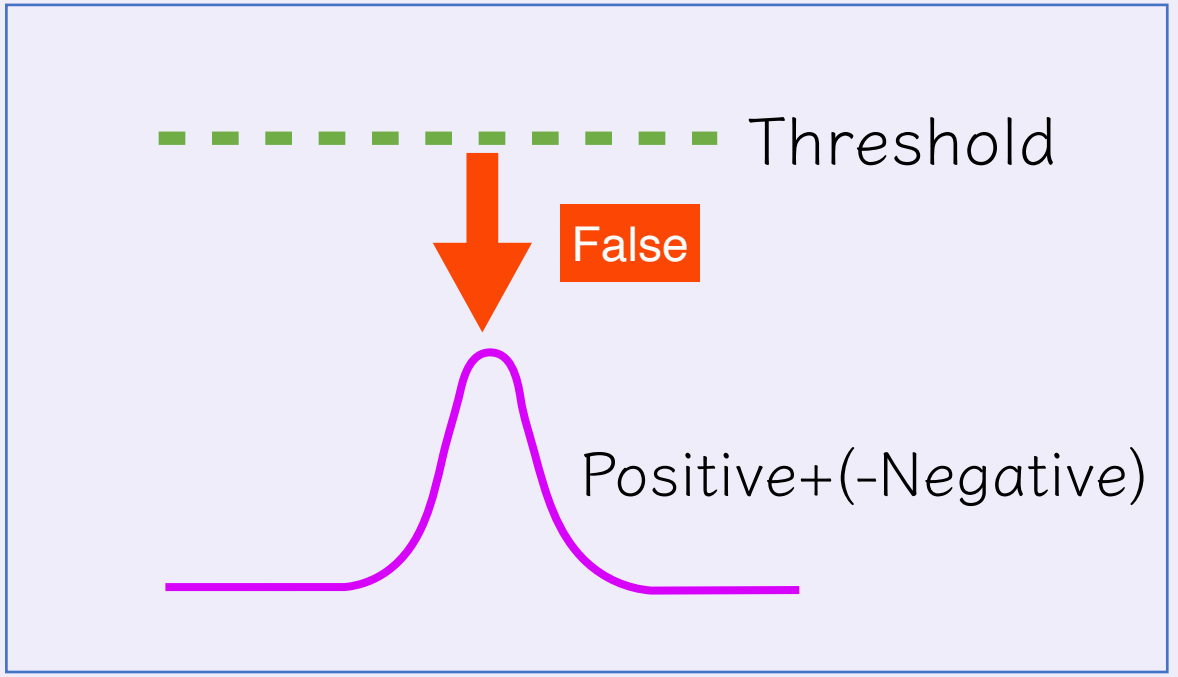
Structure

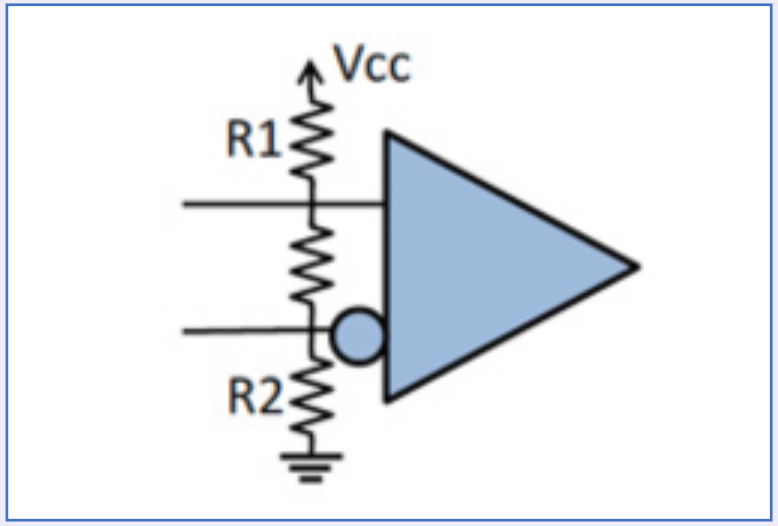
Negative

Positive



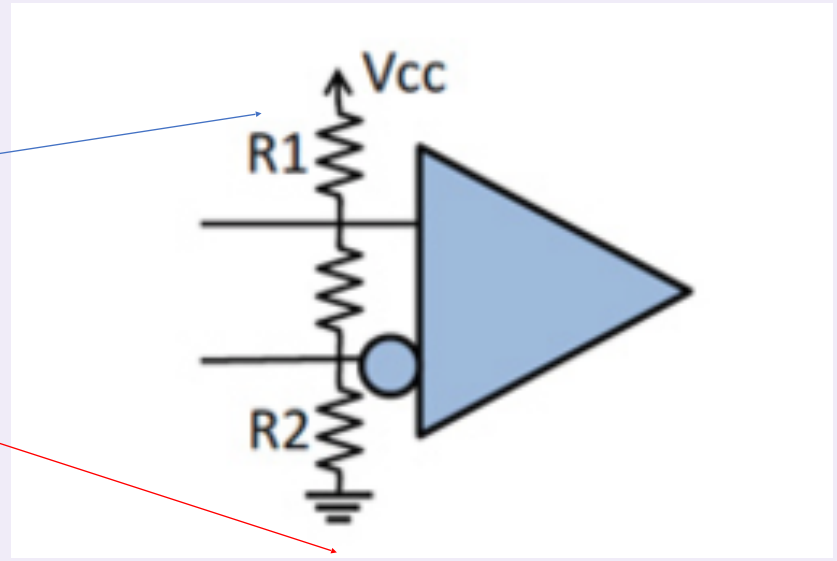
Receiver





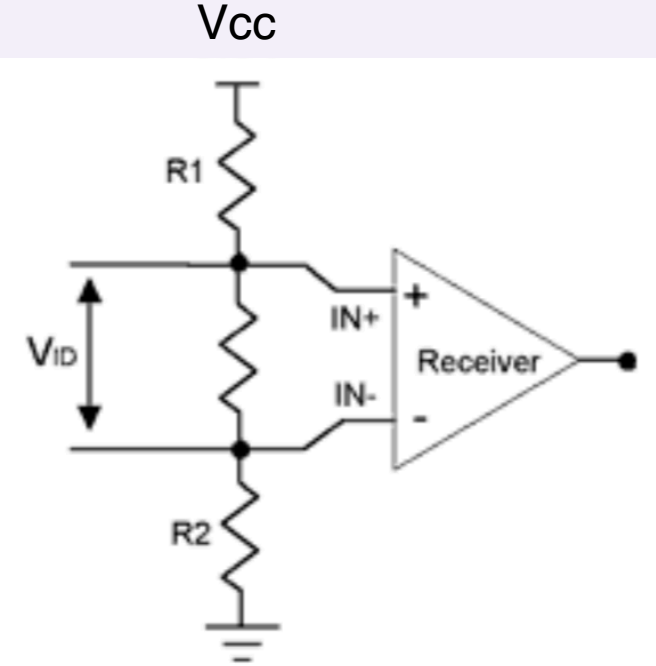
Drop the potential to the false position.

ROC Side							
RECEPTACLE (TOP)							
J1 (out side)				J2 (in side)			
#	name (net)	#	name (net)	#	name (net)	#	name (net)
1	AGND	100	DGND	1	AGND	100	DGND
2	1_CHIP1_OUT 1P	99	1_CHIP1_OUT 0P	2	SC_IN1p	99	RESET1p
3	1_CHIP1_OUT 1N	98	1_CHIP1_OUT 0N	3	SC_IN1n	98	RESET1n
4	1_CHIP2_OUT 1P	97	1_CHIP2_OUT 0P	4	DGND	97	BCO_CLK1p
5	1_CHIP2_OUT 1N	96	1_CHIP2_OUT 0N	5	DGND	96	BCO_CLK1n
6	1_CHIP3_OUT 1P	95	1_CHIP3_OUT 0P	6	OUT_CLK1p	95	SC_OUT1p
7	1_CHIP3_OUT 1N	94	1_CHIP3_OUT 0N	7	OUT_CLK1n	94	SC_OUT1n
8	1_CHIP4_OUT 1P	93	1_CHIP4_OUT 0P	8	DGND	93	DGND
9	1_CHIP4_OUT 1N	92	1_CHIP4_OUT 0N	9	DGND	92	DGND
10	CAL_INJECT1	91	DGND	10	1_CHIP6_OUT 1P	91	1_CHIP6_OUT 0P
11	AGND	90	DGND	11	1_CHIP6_OUT 1N	90	1_CHIP6_OUT 0N
12	1_CHIP5_OUT 1P	89	1_CHIP5_OUT 0P	12	1_CHIP8_OUT 1P	89	1_CHIP8_OUT 0P
13	1_CHIP5_OUT 1N	88	1_CHIP5_OUT 0N	13	1_CHIP8_OUT 1N	88	1_CHIP8_OUT 0N
14	1_CHIP7_OUT 1P	87	1_CHIP7_OUT 0P	14	1_CHIP10_OUT 1P	87	1_CHIP10_OUT 0P
15	1_CHIP7_OUT 1N	86	1_CHIP7_OUT 0N	15	1_CHIP10_OUT 1N	86	1_CHIP10_OUT 0N
16	1_CHIP9_OUT 1P	85	1_CHIP9_OUT 0P	16	1_CHIP12_OUT 1P	85	1_CHIP12_OUT 0P
17	1_CHIP9_OUT 1N	84	1_CHIP9_OUT 0N	17	1_CHIP12_OUT 1N	84	1_CHIP12_OUT 0N
18	1_CHIP11_OUT 1P	83	1_CHIP11_OUT 0P	18	AGND	83	DGND
19	1_CHIP11_OUT 1N	82	1_CHIP11_OUT 0N	19	AGND	82	DGND
20	1_CHIP13_OUT 1P	81	1_CHIP13_OUT 0P	20	AGND	81	DGND
21	1_CHIP13_OUT 1N	80	1_CHIP13_OUT 0N	21	AGND	80	+2.5VD
22	AGND	79	DGND	22	AGND	79	+2.5VD
23	AGND	78	DGND	23	+2.5VA	78	+2.5VD
24	+2.5VA	77	+2.5VD	24	+2.5VA	77	+2.5VD
25	+2.5VA	76	+2.5VD	25	+2.5VA	76	+2.5VD
26	+2.5VA	75	+2.5VD	26	+2.5VA	75	+2.5VD
27	+2.5VA	74	+2.5VD	27	+2.5VA	74	+2.5VD
28	AGND	73	DGND	28	+2.5VA	73	+2.5VD
29	AGND	72	DGND	29	AGND	72	+2.5VD
30	0_CHIP13_OUT 0N	71	0_CHIP13_OUT 1N	30	AGND	71	+2.5VD
31	0_CHIP13_OUT 0P	70	0_CHIP13_OUT 0P	31	AGND	70	DGND
32	0_CHIP11_OUT 0N	69	0_CHIP11_OUT 1N	32	AGND	69	DGND
33	0_CHIP11_OUT 0P	68	0_CHIP11_OUT 1P	33	AGND	68	DGND
34	0_CHIP9_OUT 0N	67	0_CHIP9_OUT 1N	34	0_CHIP12_OUT 0N	67	0_CHIP12_OUT 1N
35	0_CHIP9_OUT 0P	66	0_CHIP9_OUT 1P	35	0_CHIP12_OUT 0P	66	0_CHIP12_OUT 1P
36	0_CHIP7_OUT 0N	65	0_CHIP7_OUT 1N	36	0_CHIP10_OUT 0N	65	0_CHIP10_OUT 1N
37	0_CHIP7_OUT 0P	64	0_CHIP7_OUT 1P	37	0_CHIP10_OUT 0P	64	0_CHIP10_OUT 1P
38	0_CHIP5_OUT 0N	63	0_CHIP5_OUT 1N	38	0_CHIP8_OUT 0N	63	0_CHIP8_OUT 1N
39	0_CHIP5_OUT 0P	62	0_CHIP5_OUT 1P	39	0_CHIP8_OUT 0P	62	0_CHIP8_OUT 1P
40	AGND	61	DGND	40	0_CHIP6_OUT 0N	61	0_CHIP6_OUT 1N
41	CAL_INJECT0	60	DGND	41	0_CHIP6_OUT 0P	60	0_CHIP6_OUT 1P
42	0_CHIP4_OUT 0N	59	0_CHIP4_OUT 1N	42	DGND	59	DGND
43	0_CHIP4_OUT 0P	58	0_CHIP4_OUT 1P	43	DGND	58	DGND
44	0_CHIP3_OUT 0N	57	0_CHIP3_OUT 1N	44	OUT_CLK0n	57	SC_OUT0p
45	0_CHIP3_OUT 0P	56	0_CHIP3_OUT 1P	45	OUT_CLK0p	56	SC_OUT0n
46	0_CHIP2_OUT 0N	55	0_CHIP2_OUT 1N	46	DGND	55	RESET0p
47	0_CHIP2_OUT 0P	54	0_CHIP2_OUT 1P	47	DGND	54	RESET0n
48	0_CHIP1_OUT 0N	53	0_CHIP1_OUT 1N	48	SC_IN0p	53	BCO_CLK0p
49	0_CHIP1_OUT 0P	52	0_CHIP1_OUT 1P	49	SC_IN0n	52	BCO_CLK0n
50	AGND	51	DGND	50	AGND	51	DGND



AC type(large) Channel map

How to find resistance



$$V_{IID(offset)} = \frac{100 \times V_{CC}}{R1 + R2 + 100}$$

V(positive):V(negative)=R1:R2