

# ROC SlowControl FPGAの 書換えの状況

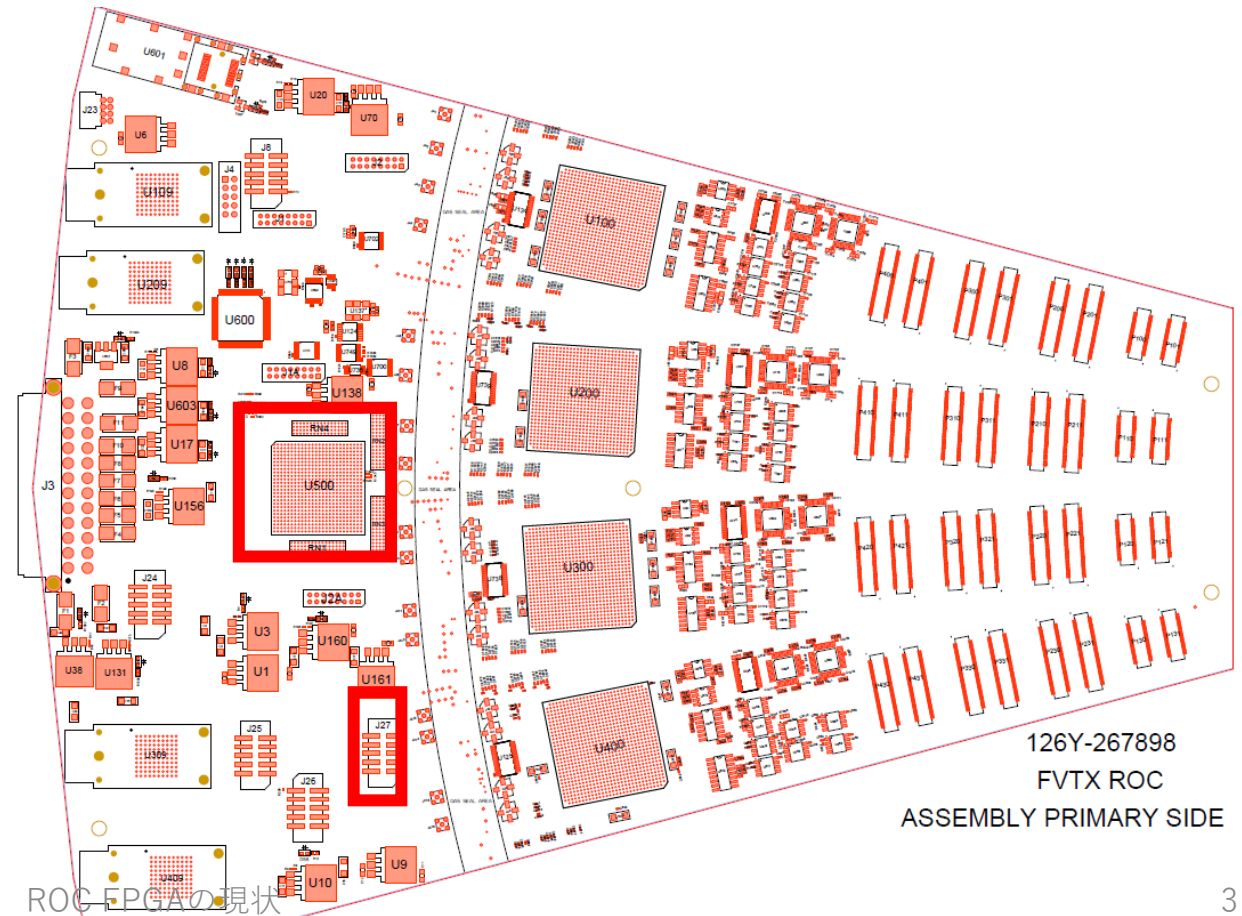
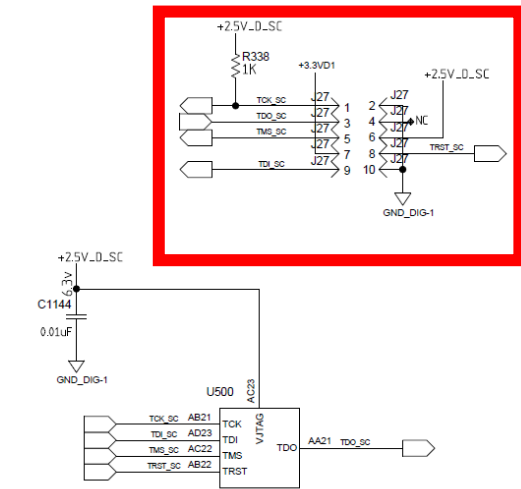
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# Readbackerの現状

- Readbacker :
  - INTTラダー上の読み出しチップ(FPHX)の情報(レジスタ値)を読み出す。
- 現状と課題
  - Bus-Extender(BEX)を接続し、読出し線路が長くなると、読み出したデータが設定値と違う。
  - 問題の症状
    - 設定値と読み出し値が違い、1ビットずれているように見える。
- 改良方針
  - 1ビットずれを補正するようにROC-FPGAを変更する。
- 結論
  - 作業をはじめた。 環境は動いているように見える
  - FPGAコードのコンパイルに失敗
  - FPGAのVerifyに失敗

# ROC-FPGA

- **SlowControl** FPGA:
  - SlowControlコマンドをラダーに送受信する。Readbackerで使用
- DataFPGA
  - ラダーで収集したデータを受信してFEM (FELIX)に送信する
- JTAG-FPGA
  - システム更新用のFPGA。使っていない



126Y-267898  
FVTX ROC  
ASSEMBLY PRIMARY SIDE

REV	CLASS	REVISIONS	DATE	CHANGE BY	CHECK BY
1	ORIGINAL ISSUE				

LOS ALAMOS		CLASSIFICATION OF	DRAWING	U
LOS ALAMOS NATIONAL LABORATORY		PART	U	DRAWING
LOS ALAMOS, NEW MEXICO 87545		TITLE	(P-25)	
			FVTX	
			ROC PROTOTYPE	
			Slow Controls FPGA	
		TOLERANCE (UNLESS OTHERWISE NOTED)		

ITER	NAME	SIGNATURE	DATE	GROUP
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2022/12/7

ROC-FPGAの現状

# セットアップ

- 開発環境
  - LIBERO SOC v11.9 (ProAsic3Eで使える)
    - 論理合成 + 配線ツール(Xilinx ISEに対応)
    - V11.9はProASIC3E用の最終版
    - 最新版(v12)はProASIC3Eが未対応。
    - FVTX開発にはv9.1が使われている
  - Win10
    - FVTXはWin7で開発したと思われる
    - Libero11.9のセットアップはそれなりに手間がかかる
      - ライセンスの入手と設定
      - ライセンスサーバーの登録など。
  - FlashPro(ソフトウェア)
    - FPGA書き込み用ソフトウェア (Xilinx iMPACTに対応)
- PCとの接続関係
  - プログラマー： FlashPro5  
MicroChip社製



# 環境の動作テスト

- カウンタ回路を作成し、論理合成→シミュレーションをしてみた
  - 動いた

```
22 use IEEE.std_logic_unsigned.all;
23
24 entity test is
25 port (
26     --<port_name> : <direction> <type>;
27     CLK          : IN std_logic;
28     Reset        : IN std_logic;
29     port_name1   : IN std_logic; -- example
30     port_name2   : OUT std_logic_vector(1 downto 0); -- example
31     out2        : OUT std_logic_vector(7 downto 0) -- example
32     --<other_ports>;
33 );
34
35 end test;
36
37 architecture architecture_test of test is
38     -- signal, component etc. declarations
39     signal signal_name1 : std_logic; -- example
40     signal signal_name2 : std_logic_vector(7 downto 0); -- example
41
42 begin
43     -- architecture body
44     port_name2(0) <= port_name1;
45     out2 <= signal_name2;
46
47     process (Reset, CLK)
48     begin
49         if (Reset = '1') then
50             signal_name2 <= (others => '0');
51             -- signal_name2 <= "00000000";
52
53         elsif (CLK'event and CLK='1') then
54             signal_name2 <= signal_name2 + "00000001";
55         end if;
56     end process;
57
58 end architecture_test;
```

Signal	Value
/test_tb2/SYSCLK	1
/test_tb2/NSYSRESET	0
/test_tb2/CLK	0
/test_tb2/testin	1
/test_tb2/testout	X
/test_tb2/testout2	(00)

Waveform simulation showing digital signals over time. A yellow vertical cursor is positioned at 981.025 ns. The testout2 signal shows a binary count sequence from 00 to 01.

Message	Message ID	Source Location	Log Location
Implementation			
Synthesis [test] ( 3 Warning(s), 2 Info(s) )			
Signal signal_name1 is undriven. Either assign the signal a value or remove the signal declaration.	CD638	test.vhd(37)	test.srr(25)
Found inferred clock test[CLK which controls 8 sequential elements including signal_name2[7:0]. This clock has no specified timing constraint which may adversely impact design performance.	MT530	test.vhd(47)	test.srr(105)
Found inferred clock test[CLK with period 10.00ns. Please declare a user-defined clock on object "p:CLK"	MT420	-	test.srr(235)
This timing report is an estimate of place and route data. For final timing results, use the FPGA vendor place and route report.	MT320	-	test.srr(251)
Clock constraints include only register-to-register paths associated with each individual clock.	MT322	-	test.srr(253)
Compile [test]			
Please refer to the log file for details about 1 Info(s)			
Place and Route [test]			
Please refer to the log file for details about 1 Info(s)			

# SlowControl FPGAのコンパイル

Libero - C:\FVTX\_VHDL\_code\ROC\_slow\_control\ROC\_slow\_control.prj\*

Project File Edit View Design Tools Help

Design Flow

ROC\_slow\_control\_top

ROC\_slow\_control\_top reports

All 2 Errors 52 Warnings 8 Info

Optimized macros:  
- Dangling net drivers: 0  
- Buffers: 1  
- Inverters: 0  
- Tieoff: 0  
- Logic combining: 10  
Total macros optimized 11

Warning: CMP503: Remapped 8 enable flip-flop(s) to a 2-tile implementation because the CLR/PRE pin on the enable flip-flop is not being driven by a global net.

Info: BLK016: Delete the global instance Inst\_input\_block/RST\_CLKINT because of clock sharing. The driver net will be rerouted.

Info: BLK016: Delete the global instance Inst\_data\_streamer/RST\_CLKINT because of clock sharing. The driver net will be rerouted.

Info: BLK016: Delete the global instance Inst\_sc/Inst\_calibrator/RST\_CLKINT because of clock sharing. The driver net will be rerouted.

Info: BLK016: Delete the global instance Inst\_input\_block/HARD\_RST\_CLKINT because of clock sharing. The driver net will be rerouted.

There were 0 error(s) and 51 warning(s) in this design.

Reading user pdc (Physical Design Constraints) file(s) postcompile

Error: PDC-71: Clock net name 'BCO\_CLK' is not valid

There were 1 error(s) and 0 warning(s) in reading the user pdc.

The Compile command failed ( 00:00:01 )  
Error: Failure when executing Tcl script. [ Line 30 ]

The Execute Script command failed ( 00:00:08 )  
Warning: The database was closed without a save, modifications are lost  
Design closed.

Message

Messages Errors Warnings Info Manage suppressed messages

Message

Please refer to the log file for details about 14 Warning(s)

- Removing instance U\_AND2\_3\_4 because it does not drive other instances. To preserve this instance, use the syn\_noprune synthesis directive.
- Signal SER\_AMPL\_EN\_OUT is floating; a simulation mismatch is possible.
- create\_generated\_clock with both -multiply\_by and -divide\_by not supported for this target technology
- Found inferred clock pll\_main|GLA\_inferred\_clock which controls 201 sequential elements including Inst\_sc.Inst\_command\_decoder.DATA\_FPHX\_OUT. This clock has no specified timing constraint which may adversely impact design performance.
- Found issues with constraints. Please check constraint checker report "C:\FVTX\_VHDL\_code\ROC\_slow\_control\synthesis\ROC\_slow\_control\_top\_cck.rpt".
- Found inferred clock pll\_main|GLA\_inferred\_clock with period 3.33ns. Please declare a user-defined clock on object "n:Inst\_DCM\_MAIN.GLA"
- Source for clock Inst\_DCM\_MAIN/Core:GLA not found in netlist. Run the constraint checker to verify if constraints are applied correctly.

Log Message 2022/12/7

ROC FPGAの現状

Fam: ProASIC3E Part: A3PE1500-2FG676 VHDL

- 失敗
  - 調査を続ける
- Libero v9.1 @ Win7も試してみる？

# FlashProによるFPGAのVerify

- FVTXのWebページにあるFPGAコードを使ってROCのSlowControlFPGAをVerify(同じコードかどうかのチェック)する



## FVTX FPGA Code

Archived VHDL code for test benches can be found [here](#)

Clock Manager Code for Spartan 3: can be found [here for 9.4 MHz code](#) and [here for 10 MHz Code](#). If you want to look at Spartan 3 board pins consult the [user guide](#) (page 49 - ).

LANL ROC, FEM, FEM Interface Card VHDL Codes for **1008**:

- [Home Page](#)
- [Operation/Maintenance/Commissioning](#)
- [Project Management](#)
- [Meetings and Presentations](#)
- [Software](#)
- [Database](#)
- [Wedge Hardware](#)
- [DAQ](#)
  - [Overview](#)
  - [Test Stands](#)
  - [ROC](#)
  - [FEM](#)
  - [FEM Interface](#)
  - [Clock Dist](#)
  - [FPGA Code](#)
  - [Misc](#)
- [BNL Assembly](#)
- [Power and Grounding](#)
- [Mechanics](#)
- [Integration](#)
- [Contact Info](#)

	ROC		FEM				GUIs	
Slow Control	Data	JTAG	Slow Control	Data	FEM_IB	nevis_gui.py	fphxtb.py	Comment
					<a href="#">23-Mar-15 Inverted BCO for NE with Trigger</a>			<b>FEM_IB:</b> Added inverted BCO based Mar13 trigger version of FEM_IB code
			<a href="#">23-Mar-15 FVTX Trigger</a>					<b>SlowControl_FEM:</b> FVTX Trigger Production.
<a href="#">12-Sep-12, fast, and slow version</a>								<b>ROC Slow Control:</b> PLL changed to 9.4 MHz input BCO rather than 10 MHz changed so that there is a 5.1335 ns delay of READ_CLK w.r.t BCO clock when generated by PLL (default used to be 1.335 ns delay). Also send LATCH and SC_EN for FPGA the SC Fiber (11 and 12) so that it can be monitored to debug SW4, column 1 pin
<a href="#">5-Sep-12, fast</a>								<b>ROC Slow Control:</b> PLL changed to 9.4 MHz input BCO rather than 10 MHz changed so that there is no delay of READ_CLK w.r.t BCO clock when generated by PLL (default used to be 1.335 ns delay). This seems to allow all channels to be when collecting calibration data.
<a href="#">22-Aug-12</a>	<a href="#">FPGA-A, fast speed</a> <a href="#">FPGA-B, D, fast speed</a> <a href="#">FPGA-C, fast speed</a>							<b>Production code</b> which should address missing 9-chip chunk problem. All are speed for direct download to FPGA.
								<b>SC FEM:</b> Added DATA_IN and CS_IN

# FPGAとの通信

The screenshot shows the FlashPro software interface. At the top, there is a menu bar (File, Edit, View, Tools, Programmers, Configuration, Customize, Help) and a toolbar. Below the toolbar, a workflow is shown with buttons: 'New Project' and 'Open Project' on the left, 'Configure Device' and 'View Programmers' in the middle, and 'VERIFY' on the right, connected by orange arrows. A 'Device Status Report' window is open in the center, displaying the following information:

Device: A3PE1 500 (A3PE1 500) Programmer: S2001 L82UX (S2001 L82UX)

Device Status:

IDCode (read from the device) (HEX):	1253A1CF
--------------------------------------	----------

User Information:

UROW data (HEX):	935b0352f9c3f739bf7dfee328803dc1
Programming Method:	STAPL
Programmer:	FlashPro4
Programmer Software:	FlashPro vXX
Design Name:	ROC_slow_c
Design Check Sum:	935B
Algorithm Version:	20
Array Prog. Cycle Count:	13

Device State:

IRCapture Register (HEX):	55
FPGA Array Status:	Programmed and enabled

Factory Data:

Factory Serial Number (HEX):	91369c4468
------------------------------	------------

Security:

Device has no security enforced.

- デバイスコードの読出しに成功
- 通信できた

```
Project closed.
Software Version: 11.9.0.4
STAPL file 'C:\FVVTX_VHDL_code\ROC_slow_control\designer\impl1\ROC_slow_control_top.stp' has been loaded successfully.
DESIGN : ROC_slow_control_top; CHECKSUM : 7A8B; ALG_VERSION : 20
programmer 'S2001L82UX' : FlashPro5
Warning: The programmer with id '08756' in the project file cannot be detected and connected.
Opened 'C:\FVVTX_VHDL_code\ROC_slow_control_slow_21May12\designer\impl1\ROC_slow_control_top_fp\ROC_slow_control_top.pro'
Selecting device A3PE1500 for debug
```



# Verifyのテスト

File Edit View Tools Programmers Configuration Customize Help

New Project Open Project Configure Device View Programmers VERIFY

Programmer Name	Programmer Type	Port	Programmer Status	Programmer Enabled
1 S2001L82UX	FlashPro5	usbS2001L82UX	RUN FAILED	<input checked="" type="checkbox"/>

Refresh/Rescan for Programmers

```
programmer 'S2001L82UX' : Executing action VERIFY
programmer 'S2001L82UX' : EXPORT FSN[48] = 9103690c4468
programmer 'S2001L82UX' : Verifying FPGA Array
programmer 'S2001L82UX' : Verify 0 failed at row 5636.
programmer 'S2001L82UX' : EXPORT ERROR_CODE[16] = 805a
programmer 'S2001L82UX' : Finished: Tue Dec 06 17:42:06 2022 (Elapsed time 00:00:00)
Error: programmer 'S2001L82UX' : Executing action VERIFY FAILED, EXIT 11, refer to FlashPro onl
```

Programming file: ROC\_slow\_control\_top.stp

Mode:  Basic  Advanced

Action:  PROGRAM  VERIFY  ERASE

Chain Parameters... Inspect Device

# エラーメッセージの意味

				CHECK_AND_BACKUP_CALIB
0x805A 0x805C	11	Verify 0 failed at row <row number> .  Verify 1 failed at row <row number>	Device is programmed with a different design  Unstable VPUMP voltage level.  Unstable VCC  Unstable VCC_OSC (Fusion only)  Unstable VCC_ROSC voltage level (SmartFusion only)  Signal integrity issues on JTAG pins	Run VERIFY_DEVICE_INFO to verify the device is programmed with the correct data/design.  Monitor related power supplies that cause the issue during programming; check for transients outside of Microsemi specifications. See your <a href="#">device datasheet</a> for more information on transient specifications.  Monitor VJTAG during programming; measure JTAG signals for noise or reflection.

- デザインが違うというエラーに見える
- FVTXのウェブサイトにあるコードを複数試したが失敗した。
  - 試していないものもあるので、もうしばらくテストする予定。

# まとめ

- ROC slowcontrol FPGAの修正作業をはじめた。
  - 開発環境は動いているように見える
  - FPGAコードのコンパイルに失敗
  - FPGAのVerifyに失敗
- 開発に向けての準備
  - ROC用のベンチ(ROC + 電源のみ)を準備する予定
    - 宇宙線測定と分けるため

0x8060	11	Failed to verify FlashROM at row <FlashROM row number>.	<p>Device is programmed with a different design.</p> <p>Unstable VPUMP voltage level.</p> <p>Unstable VCC</p> <p>Unstable VCC_OSC (Fusion only)</p> <p>Unstable VCC_ROSC voltage level (SmartFusion only)</p> <p>Signal integrity issues on JTAG pins.</p>	<p>Run VERIFY_DEVICE_INFO to verify the device is programmed with the correct data/design.</p> <p>Monitor related power supplies that cause the issue during programming; check for transients outside of Microsemi specifications. See your <a href="#">device datasheet</a> for more information on transient specifications.</p> <p>Monitor VJTAG during programming; measure JTAG signals for noise or reflection.</p>
0x8075 0x8076 0x8077	11	Failed to verify Embedded Flash Memory Block (EFMB)	<p>Device is programmed with a different design.</p> <p>Unstable VCC</p> <p>Unstable VCC_NVM/VCC_OSC (Fusion only)</p> <p>Unstable VCC_ENVM/VCC_ROSC voltage level (SmartFusion only)</p> <p>Signal integrity issues on JTAG pins.</p> <p>The EFMB data was modified in your FPGA design after programming. This could have occurred during standalone verify.</p> <p>The target EFMB is locked with FlashLock when running ACTION PROGRAM_NVM_ACTIVE_ARRAY or VERIFY_NVM_ACTIVE_ARRAY.</p>	<p>Verify the device is programmed with the correct data/design.</p> <p>Monitor related power supplies that cause the issue during programming; check for transients outside of Microsemi specifications. See your <a href="#">device datasheet</a> for more information on transient specifications.</p> <p>Measure JTAG pins, and noise or reflection.</p> <p>Run DEVICE_INFO to confirm if the target EFMB block is locked with FlashLock (pass key). If the target EFMB block is locked, then you must unlock it by erasing the security and then reprogramming with the desired security settings. After unlocking the target EFMB block attempt to rerun the target ACTION.</p>