ROC SlowControl FPGAの書換えの状況

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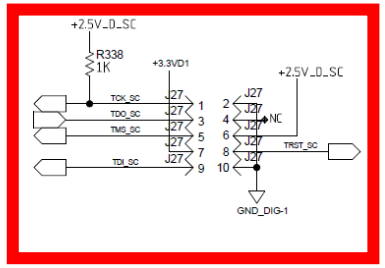
Readbackerの現状

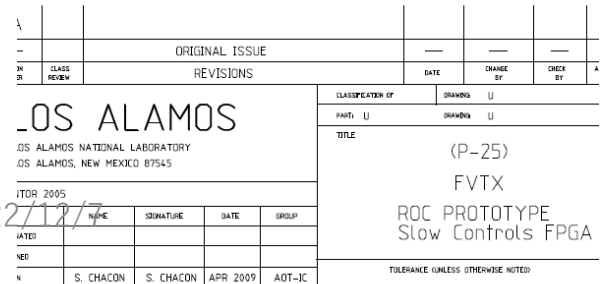
- Readbacker：
  - INTTラダー上の読み出しチップ(FPHX)の情報(レジスタ値)を読み出す。
- 現状と課題
  - Bus-Extender(BEX)を接続し、読出し線路が長くなると、読み出したデータが設定値と違う。
  - 問題の症状
    - 設定値と読み出し値が違い、1ビットずれているように見える。
- 改良方針
  - 1ビットずれを補正するようにROC-FPGAを変更する。

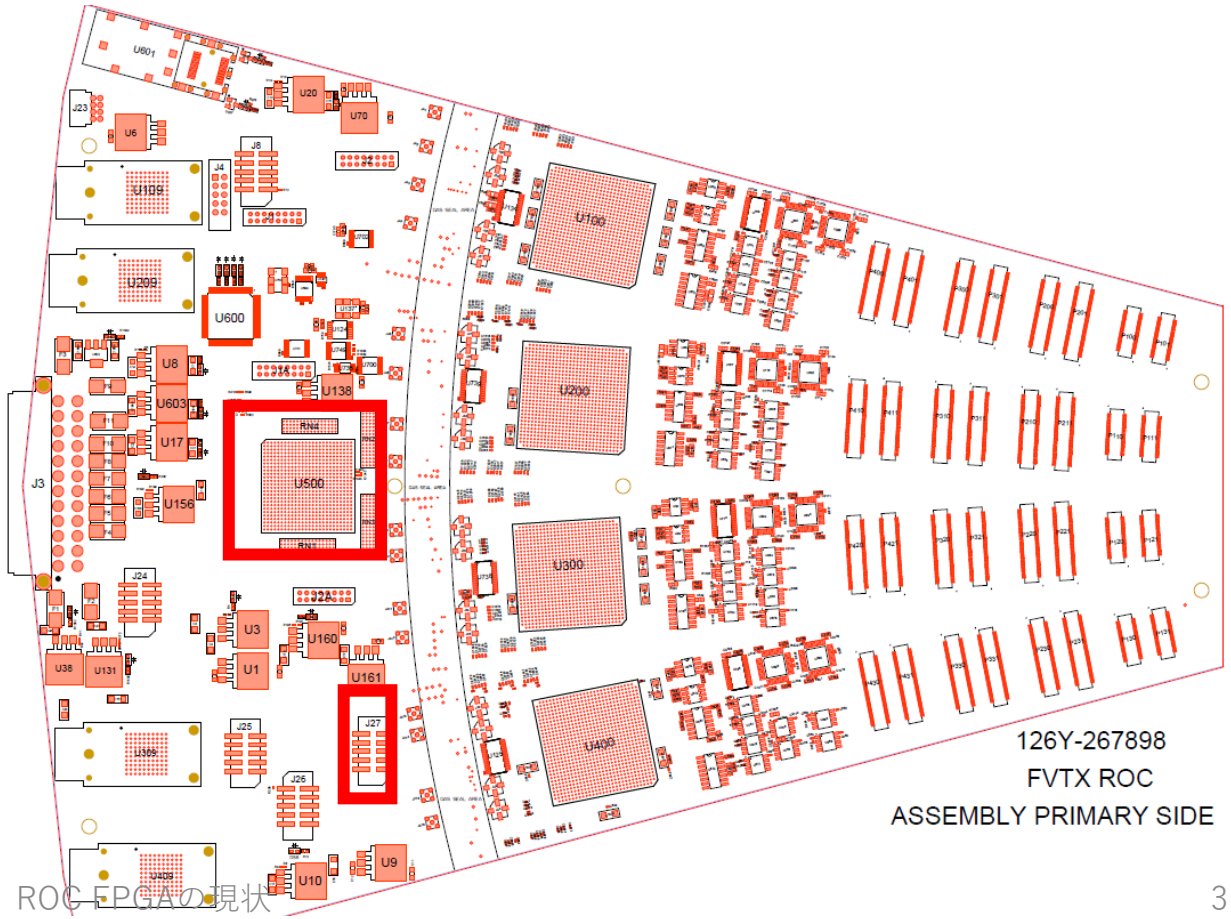
- 結論
  - 作業をはじめた。　環境は動いているように見える
  - FPGAコードのコンパイルに失敗
  - FPGAのVerifyに失敗

ROC-FPGA

- SlowControl FPGA:
  - SlowControlコマンドをラダーに送受信する。Readbackerで使用
- DataFPGA
  - ラダーで収集したデータを受信してFEM (FELIX)に送信する
- JTAG-FPGA
  - システム更新用のFPGA。　使っていない







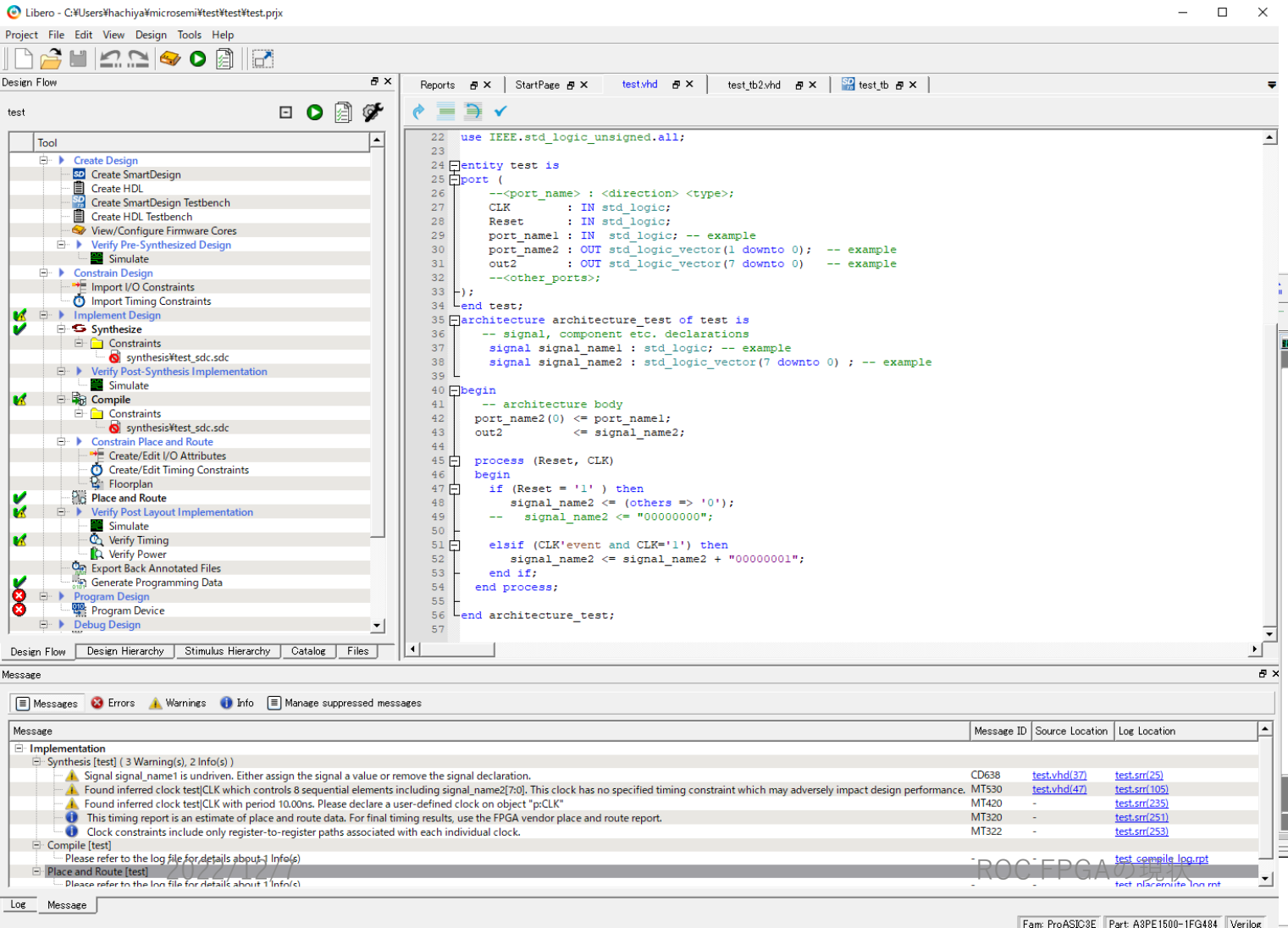
セットアップ

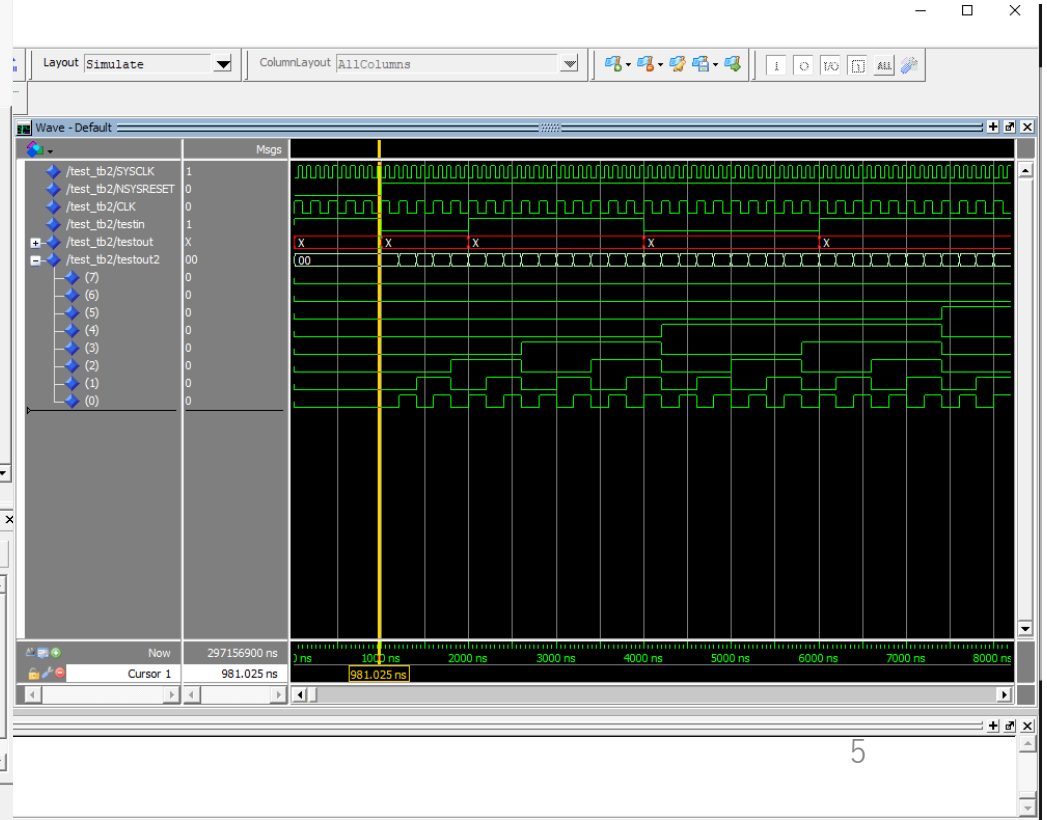
- 開発環境
  - LIBERO SOC v11.9 (ProAsic3Eで使える)
    - 論理合成＋配線ツール(Xilinx ISEに対応)
    - V11.9はProASIC3E用の最終版
    - 最新版(v12)はProASIC3Eが未対応。
    - FVTX開発にはv9.1が使われている
  - Win10
    - FVTXはWin7で開発したと思われる
    - Libero11.9のセットアップはそれなりに手間がかかる
      - ライセンスの入手と設定
      - ライセンスサーバーの登録など。
  - FlashPro(ソフトウェア)
    - FPGA書き込み用ソフトウェア (Xilinx iMPACTに対応)

- PCとの接続関係
  - プログラマー：　FlashPro5
    MicroChip社製

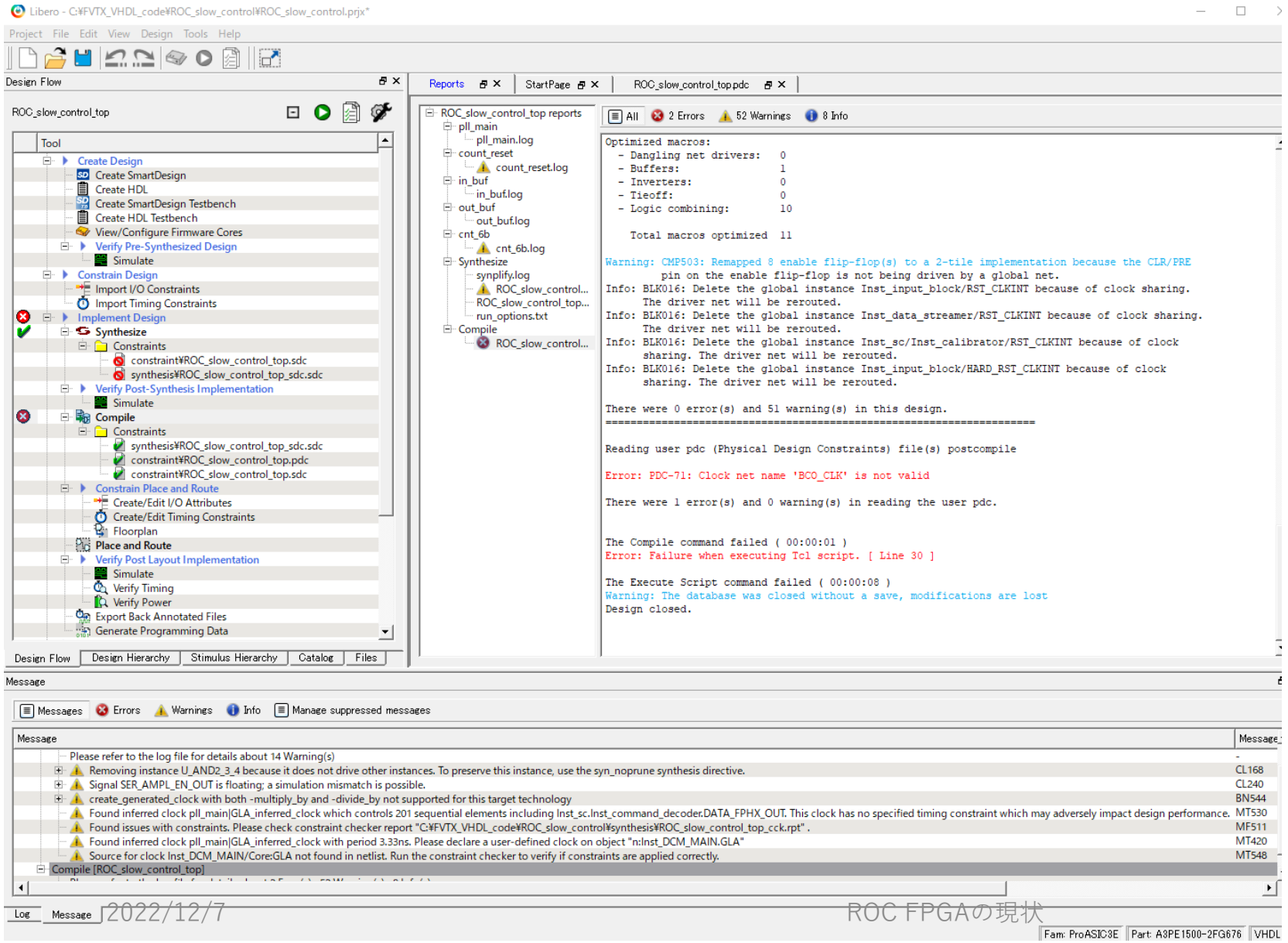
環境の動作テスト

- カウンタ回路を作成し、論理合成→シミュレーションをしてみた
  - 動いた





SlowControl FPGAのコンパイル



- 失敗
  - 調査を続ける
- Libero v9.1 @ Win7も試してみる？

FlashProによるFPGAのVerify

- FVTXのWebページにあるFPGAコードを使ってROCのSlowControlFPGAをVerify(同じコードかどうかのチェック)する

FVTX Group

FVTX

- Home Page
- Operation/Maintenance /Commissioning
- Project Management
- Meetings and Presentations
- Software
- Database
- Wedge Hardware
- DAQ
  - Overview
  - Test Stands
  - ROC
  - FEM
  - FEM Interface
  - Clock Dist
  - FPGA Code
  - Misc
- BNL Assembly
- Power and Grounding
- Mechanics
- Integration
- Contact Info

FVTX FPGA Code

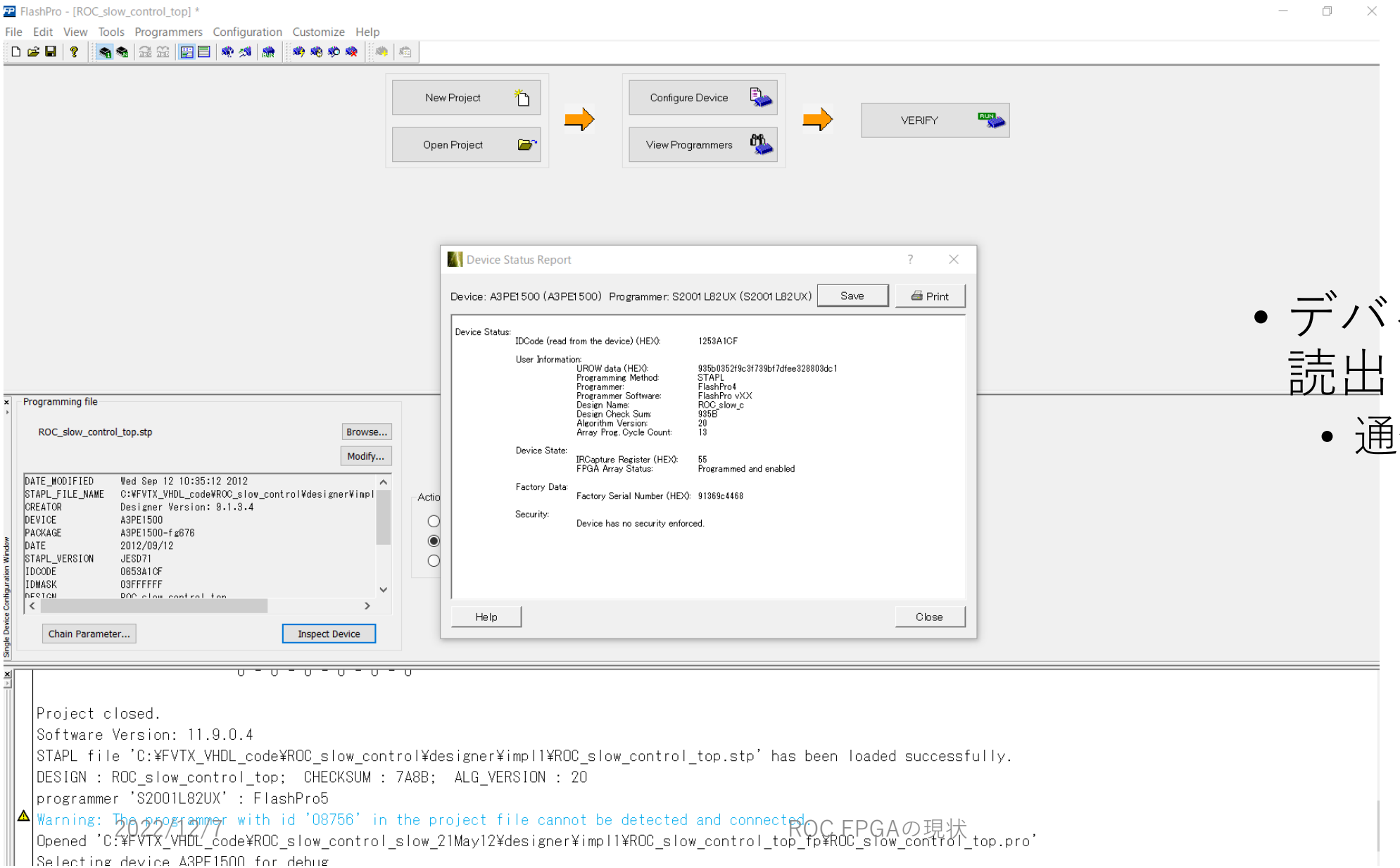
Archived VHDL code for test benches can be found here

Clock Manager Code for Spartan 3: can be found here for 9.4 MHz code and here for 10 MHz Code. If you want to look at Spartan 3 board pin consult the user guide (page 49 -).

LANL ROC, FEM, FEM Interface Card VHDL Codes for 1008:

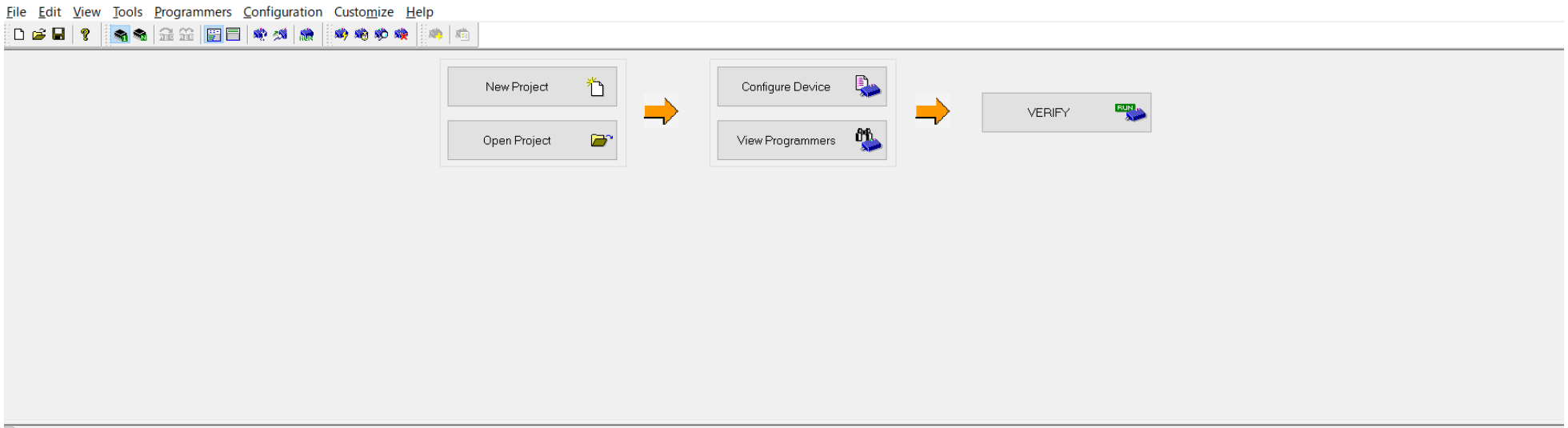
	ROC		FEM				GUIs	
Slow Control	**Data**	**JTAG**	**Slow Control**	**Data**	**FEM_IB**	**nevis_gui.py**	**fphxtb.py**	**Comment**
					23-Mar-15**Inverted BCO for NE with Trigger**			**FEM_IB:** Added inverted BCO based Mar13 trigger version of FEM_IB coc
			23-Mar-15 **FVTX Trigger**					**SlowControl_FEM:** FVTX Trigger Production.
12-Sep-12, fast , and slow version								**ROC Slow Control:** PLL changed to 9.4 MHz input BCO rather than 10 MI changed so that there is a 5.1335 ns c READ_CLK w.r.t BCO clock when gene by PLL (default used to be 1.335 ns de Also send LATCH and SC_EN for FPG the SC Fiber (11 and 12) so that it car monitored to debug SW4, column 1 pr
5-Sep-12, fast								**ROC Slow Control:** PLL changed to 9.4 MHz input BCO rather than 10 MI changed so that there is no delay of READ_CLK w.r.t BCO clock when gene by PLL (default used to be 1.335 ns de This seems to allow all channels to be when collecting calibration data.
22-Aug-12	FPGA-A, fast speed FPGA-B_D, fast speed FPGA-C, fast speed							**Production code** which should addre missing 9-chip chunk problem. All are speed for direct download to FPGA.

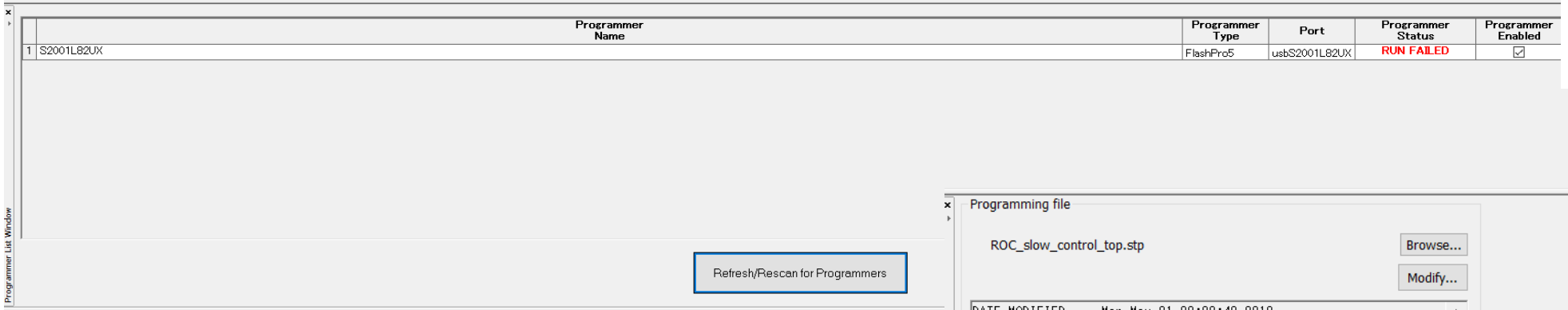
FPGAとの通信

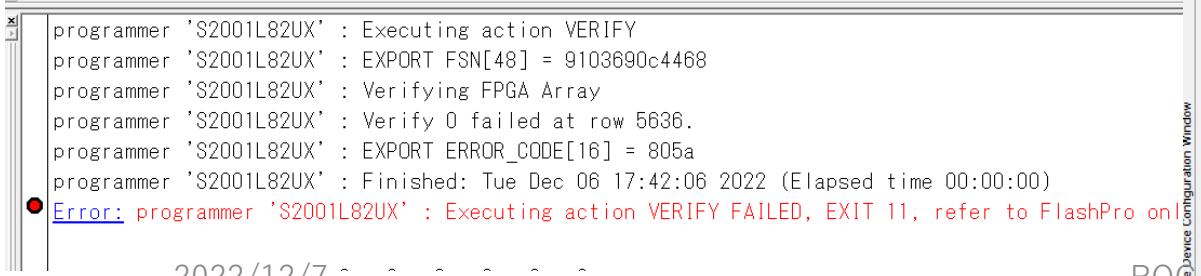


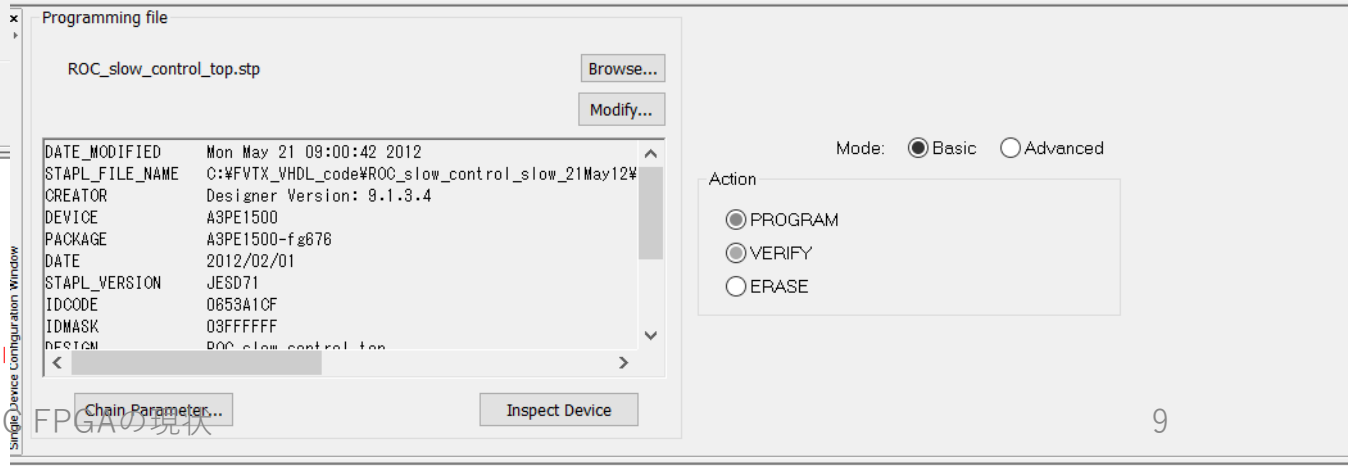
- デバイスコードの読出しに成功
  - 通信できた

Verifyのテスト


File Edit View Tools Programmers Configuration Customize Help
New Project
Open Project
Configure Device
View Programmers
VERIFY


Programmer Name
Programmer Type
Port
Programmer Status
Programmer Enabled
1 S2001L82UX
FlashPro5
usbS2001L82UX
RUN FAILED
Refresh/Rescan for Programmers


programmer 'S2001L82UX' : Executing action VERIFY
programmer 'S2001L82UX' : EXPORT FSN[48] = 9103690c4468
programmer 'S2001L82UX' : Verifying FPGA Array
programmer 'S2001L82UX' : Verify 0 failed at row 5636.
programmer 'S2001L82UX' : EXPORT ERROR_CODE[16] = 805a
programmer 'S2001L82UX' : Finished: Tue Dec 06 17:42:06 2022 (Elapsed time 00:00:00)
Error: programmer 'S2001L82UX' : Executing action VERIFY FAILED, EXIT 11, refer to FlashPro onl


Programming file
ROC_slow_control_top.stp
Browse...
Modify...
DATE_MODIFIED Mon May 21 09:00:42 2012
STAPL_FILE_NAME C:¥FVTX_VHDL_code¥ROC_slow_control_slow_21May12¥
CREATOR Designer Version: 9.1.3.4
DEVICE A3PE1500
PACKAGE A3PE1500-fg676
DATE 2012/02/01
STAPL_VERSION JESD71
IDCODE 0653A1CF
IDMASK 03FFFFFF
Mode: Basic Advanced
Action
PROGRAM
VERIFY
ERASE
Chain Parameter...
Inspect Device

エラーメッセージの意味

				CHECK_AND_BACKUP_CALIB
0x805A 0x805C	11	Verify 0 failed at row <row number> . Verify 1 failed at row <row number>	Device is programmed with a different design Unstable VPUMP voltage level. Unstable VCC Unstable VCC_OSC (Fusion only) Unstable VCC_ROSC voltage level (SmartFusion only) Signal integrity issues on JTAG pins	Run VERIFY_DEVICE_INFO to verify the device is programmed with the correct data/design. Monitor related power supplies that cause the issue during programming; check for transients outside of Microsemi specifications. See your device datasheet for more information on transient specifications. Monitor VJTAG during programming; measure JTAG signals for noise or reflection.
				Monitor related power supplies that cause

- デザインが違うというエラーに見える

- FVTXのウェブサイトにあるコードを複数試したが失敗した。
  - 試していないものもあるので、もうしばらくテストする予定。

まとめ

- ROC slowcontrol FPGAの修正作業をはじめた。
  - 開発環境は動いているように見える
  - FPGAコードのコンパイルに失敗
  - FPGAのVerifyに失敗

- 開発に向けての準備
  - ROC用のベンチ(ROC＋電源のみ)を準備する予定
    - 宇宙線測定と分けるため

0x8060	11	Failed to verify FlashROM at row <FlashROM row number>.	Device is programmed with a different design. Unstable VPUMP voltage level. Unstable VCC Unstable VCC_OSC (Fusion only) Unstable VCC_ROSC voltage level (SmartFusion only) Signal integrity issues on JTAG pins.	Run VERIFY_DEVICE_INFO to verify the device is programmed with the correct data/design. Monitor related power supplies that cause the issue during programming; check for transients outside of Microsemi specifications. See your device datasheet for more information on transient specifications. Monitor VJTAG during programming; measure JTAG signals for noise or reflection.
0x8075 0x8076 0x8077	11	Failed to verify Embedded Flash Memory Block (EFMB)	Device is programmed with a different design. Unstable VCC Unstable VCC_NVM/VCC_OSC (Fusion only) Unstable VCC_ENVM/VCC_ROSC voltage level (SmartFusion only) Signal integrity issues on JTAG pins. The EFMB data was modified in your FPGA design after programming. This could have occurred during standalone verify. The target EFMB is locked with FlashLock when running ACTION PROGRAM_NVM_ACTIVE_ARRAY or VERIFY_NVM_ACTIVE_ARRAY.	Verify the device is programmed with the correct data/design. Monitor related power supplies that cause the issue during programming; check for transients outside of Microsemi specifications. See your device datasheet for more information on transient specifications. Measure JTAG pins, and noise or reflection. Run DEVICE_INFO to confirm if the target EFMB block is locked with FlashLock (pass key). If the target EFMB block is locked, then you must unlock it by erasing the security and then reprogramming with the desired security settings. After unlocking the target EFMB block attempt to rerun the target ACTION.