LGAD R&D in Taiwan

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On behave of TIDC consortium

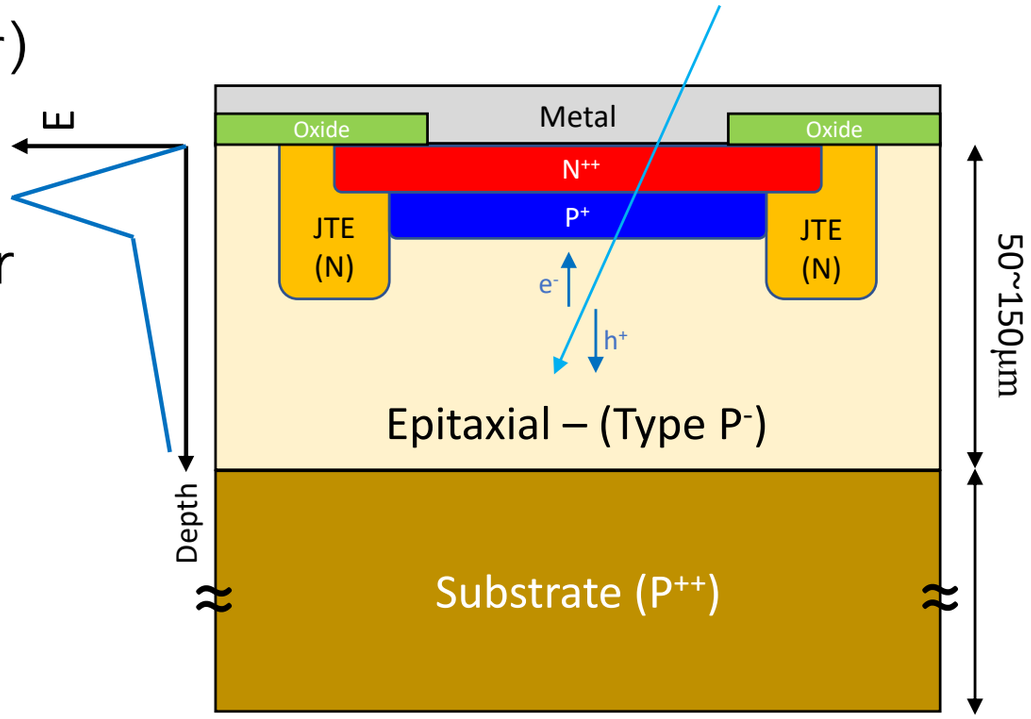
Introduction

- In Taiwan, we started the R&D project following the CMS RTD proposal and sought for developing our own LGAD fabrication line.
- Collaborating with local institutes/companies to produce DC-LGAD sensors. Exploring the fabrication possibility
- Designed various DC-LGAD structures and submitted masks for production at Taiwan Semiconductor Research Institute, TSRI.
- Preserve know-how and evaluate TCAD simulation for future R&D.

TMC - Taiwan Mask Corporation

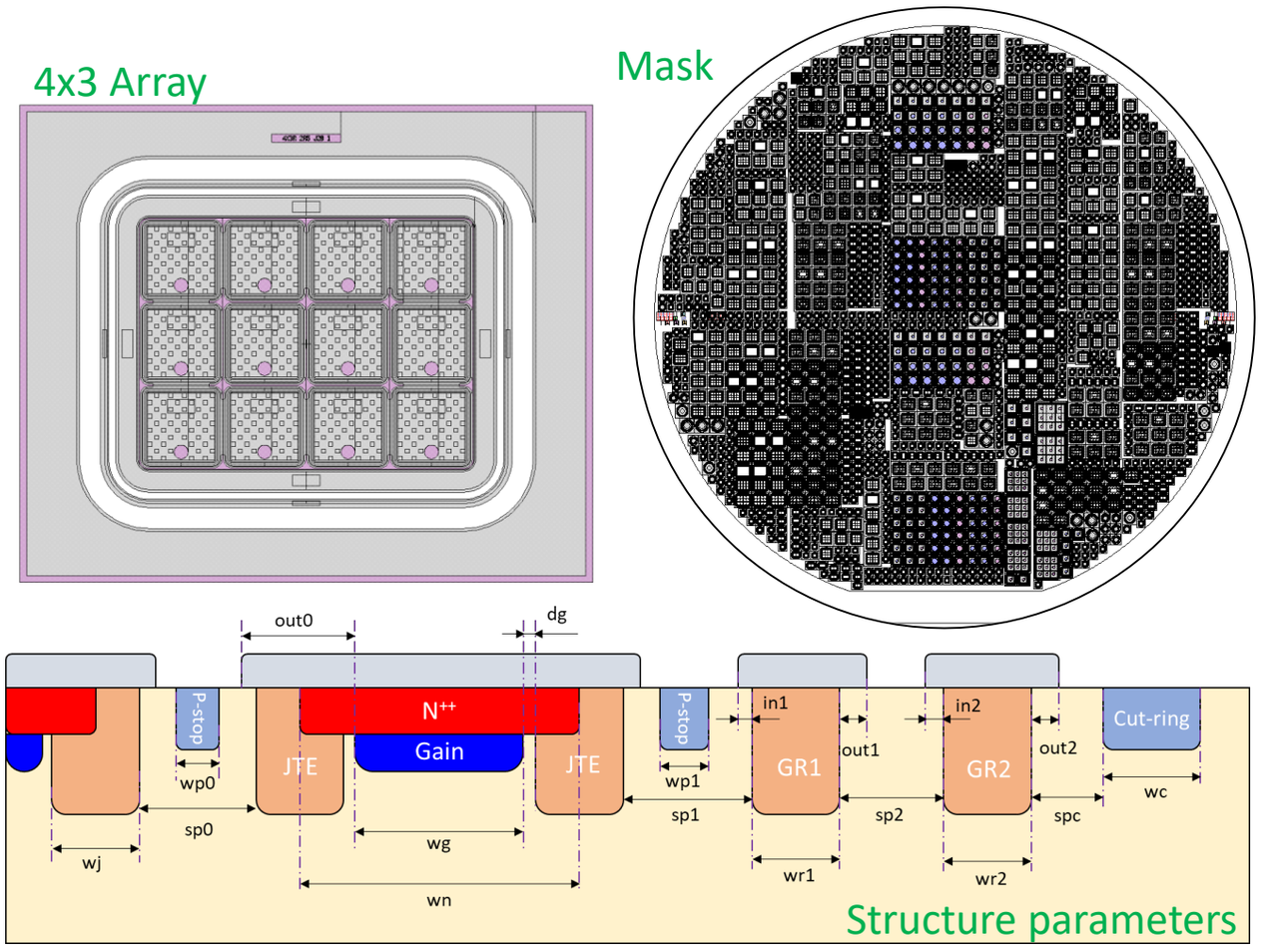
Low Gain Avalanche Detector

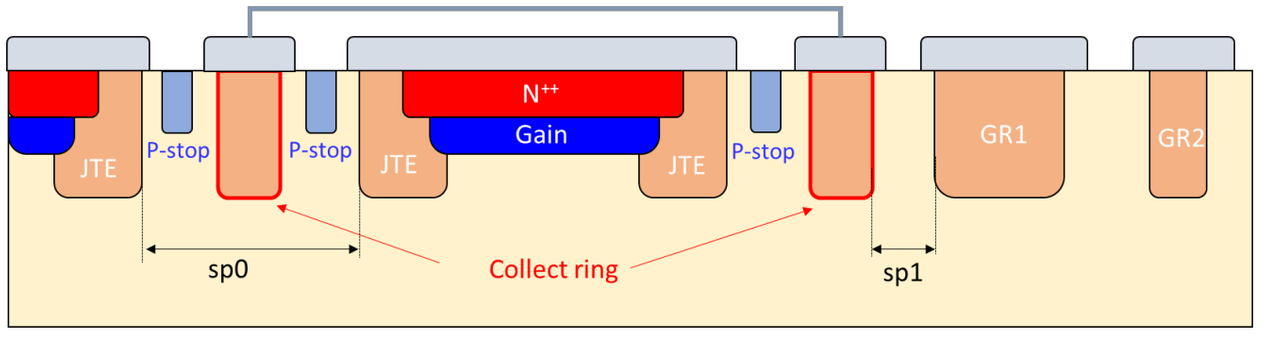
- Characteristic：
  - ✦ High time resolution (~30ps)
  - ✦ Controlled gain produced by gain layer (P^+ layer)
- What we do in Taiwan?
  - ✦ Simulate the LGAD process and electric behavior with TCAD to build a possible process flow and parameters. In the first LGAD manufacture, various configurations were used. We want to verify our TCAD simulation with real product. It can help us to improve the sensor design in the future.
  - ✦ Design masks for DC-LGAD sensor. First set of masks was produced by Taiwan Mask Corporation (TMC).
  - ✦ Produce sensor wafers at Taiwan Semiconductor Research Institute (TSRI). A batch of 12 wafers with 7 configurations was delivered.
  - ✦ Measure IV, CV and gain of LGAD sensor.



Mask Design

- Type: pixel DC-pad structure
- Purpose: Study the structure for breakdown voltage and cross talk.
- There are ~180 different structures in the mask.
- Almost parameters are studied in the small single test keys.
- Parameters:
  - ✦ Area of gain layer: 0.5x0.5 ~ 2x2 mm^2
  - ✦ Array cell size (1x1 ~ 3x4)
  - ✦ Pattern width
  - ✦ Pitch
  - ✦ Guard Ring: numbers, width, and pitch
  - ✦ P-stop
  - ✦ Collect ring

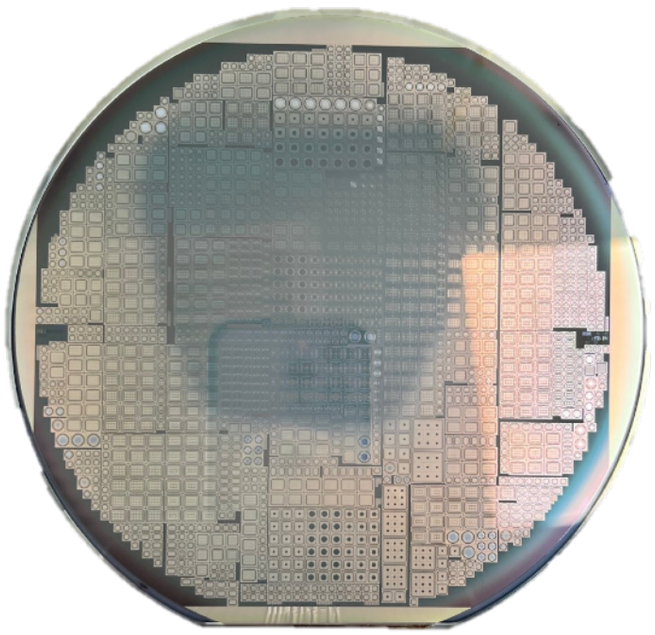


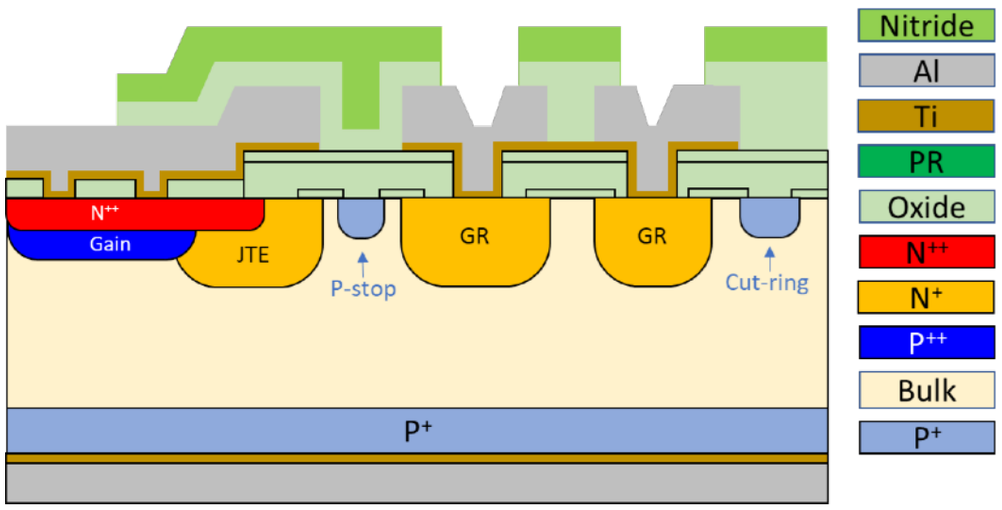


Manufacture in TSRI

- Wafers are 6" FZ〈100〉 with a resistivity of 3000 Ω-cm and a thickness of 625 μm. (Not ideal, should use 50μm epi-wafer)
- 12 wafers with 7 different configurations
- The right table shows the processes.
- Pros: TSRI gives us information during manufacturing. We control the parameters of processing.
- Cons: No standard procedure. We have to try ourselves for production.

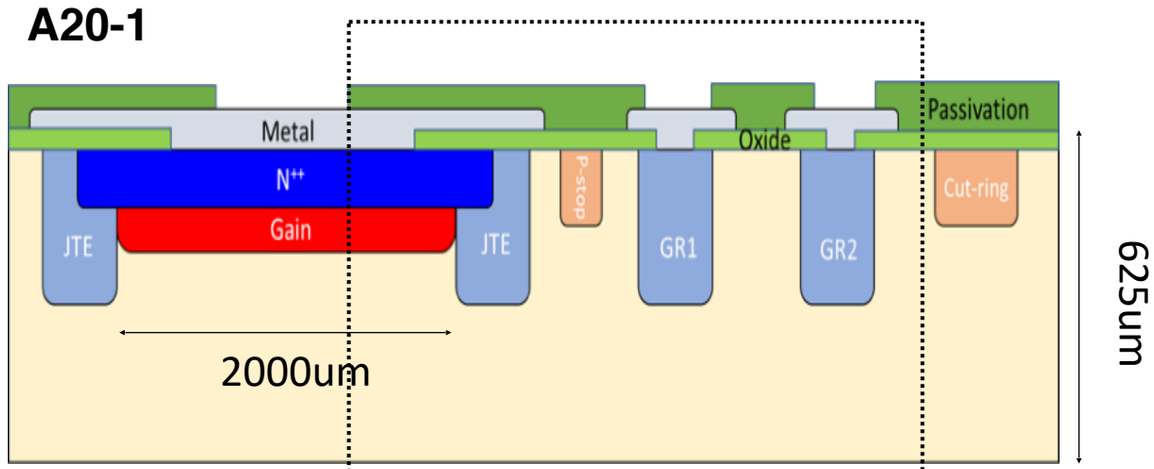
1	Backside imp.
2	JTE&GR imp.
3	P-stop imp.
4	Drive in 1 (Wet Oxide)
5	Gain layer imp.
6	Drive in 2
7	N^{++} imp.
8	Drive in 3
9	PECVD oxide
10	Contact etch
11	Front Metal dep.
12	Front Metal etch
13	alloy
14	Passivation dep.
15	Passivation etch
16	Back Metal dep.
17	alloy



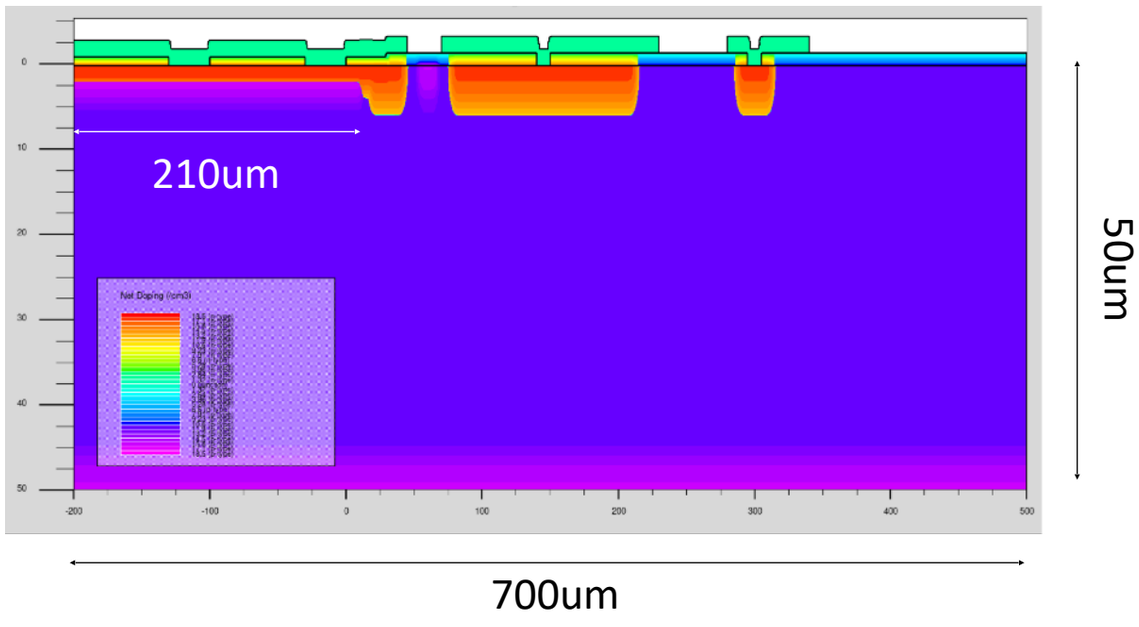


TCAD Simulation

- Simulate with the realistic structure of various configurations.
- Only 210μm into gain region.
- 50μm thickness in simulation

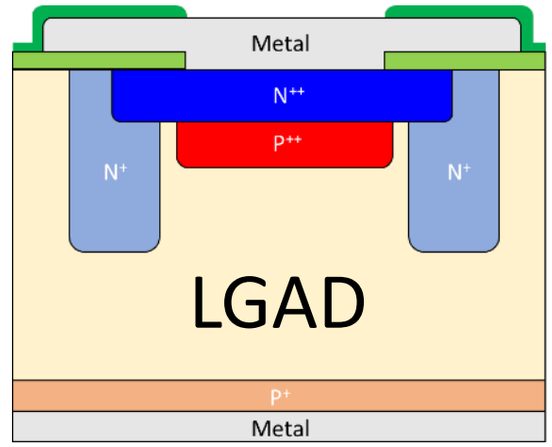


TCAD simulation



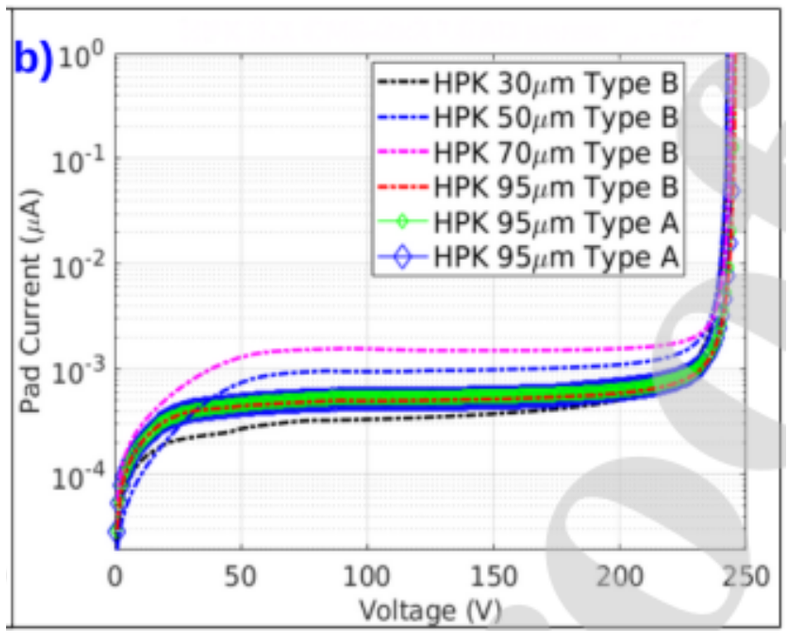
LGAD Property Measurement

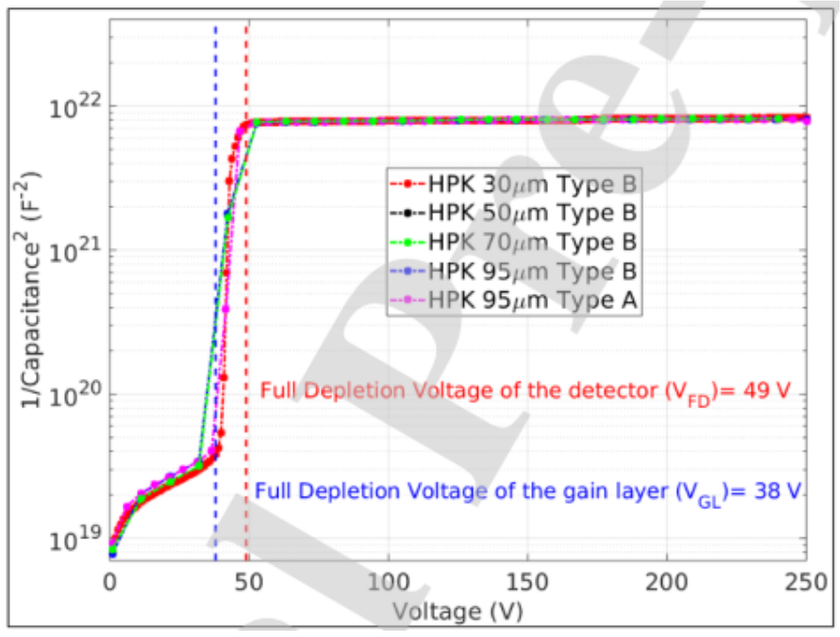
- Measure IV and CV for both LGAD cell and PIN diode with same structure on the same wafer
- LGAD cell will have two-step response due to the gain layer
- The first step show the depletion of gain layer where 2nd step shows the depletion of full bulk

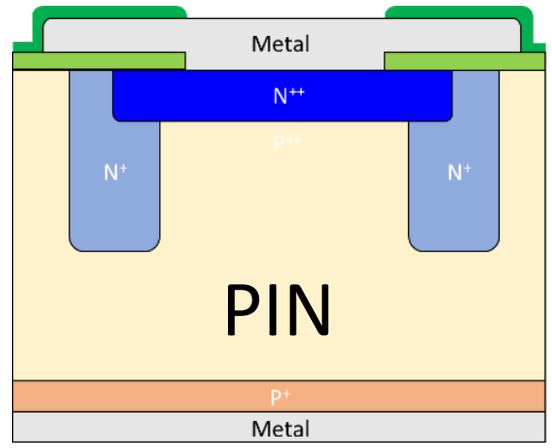


From HPK 3.1 production LGADs

NIMA 979 (2020) 164494

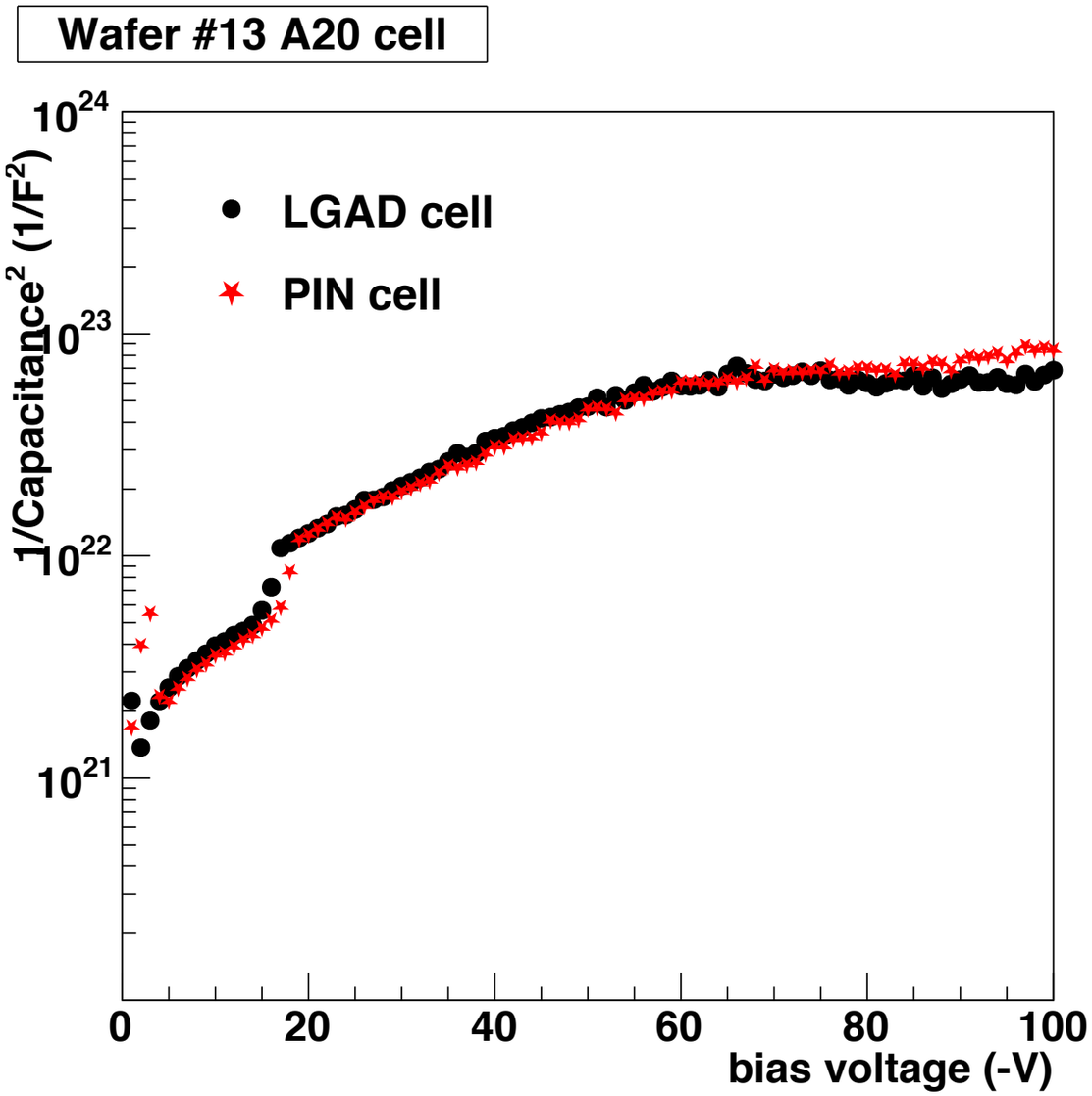






CV Measurement

- CV measurement shows two steps but in both LGAD and PIN diode.
- CMN Sensor also has PIN diode showing two-step response. The reason was not described in literature.



HPK

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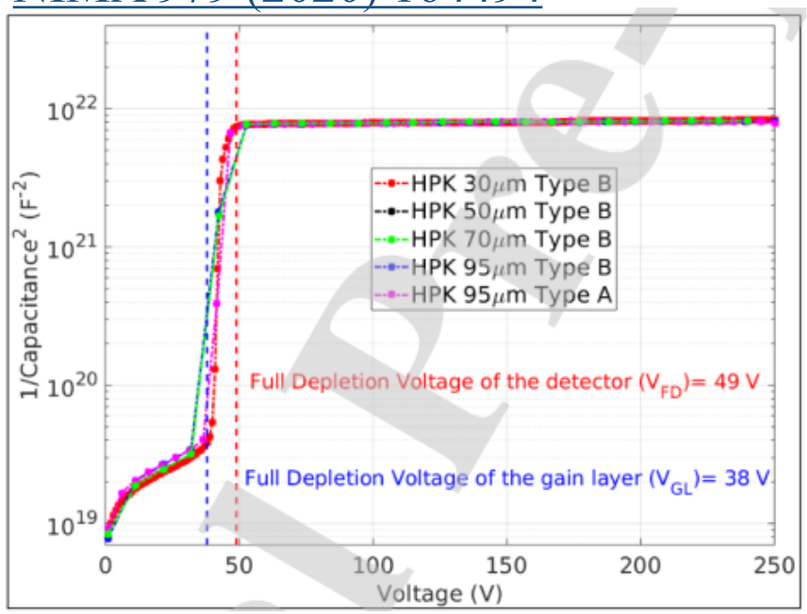
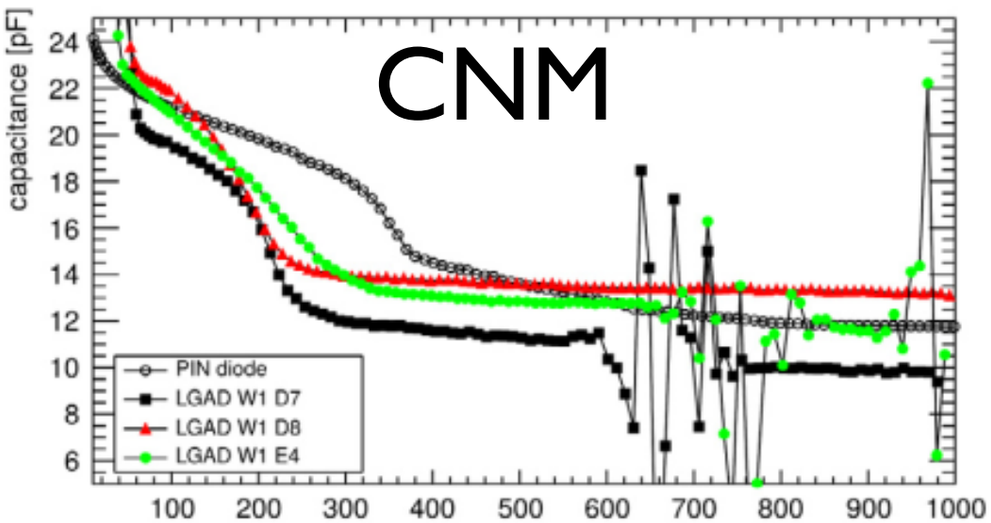


CNM

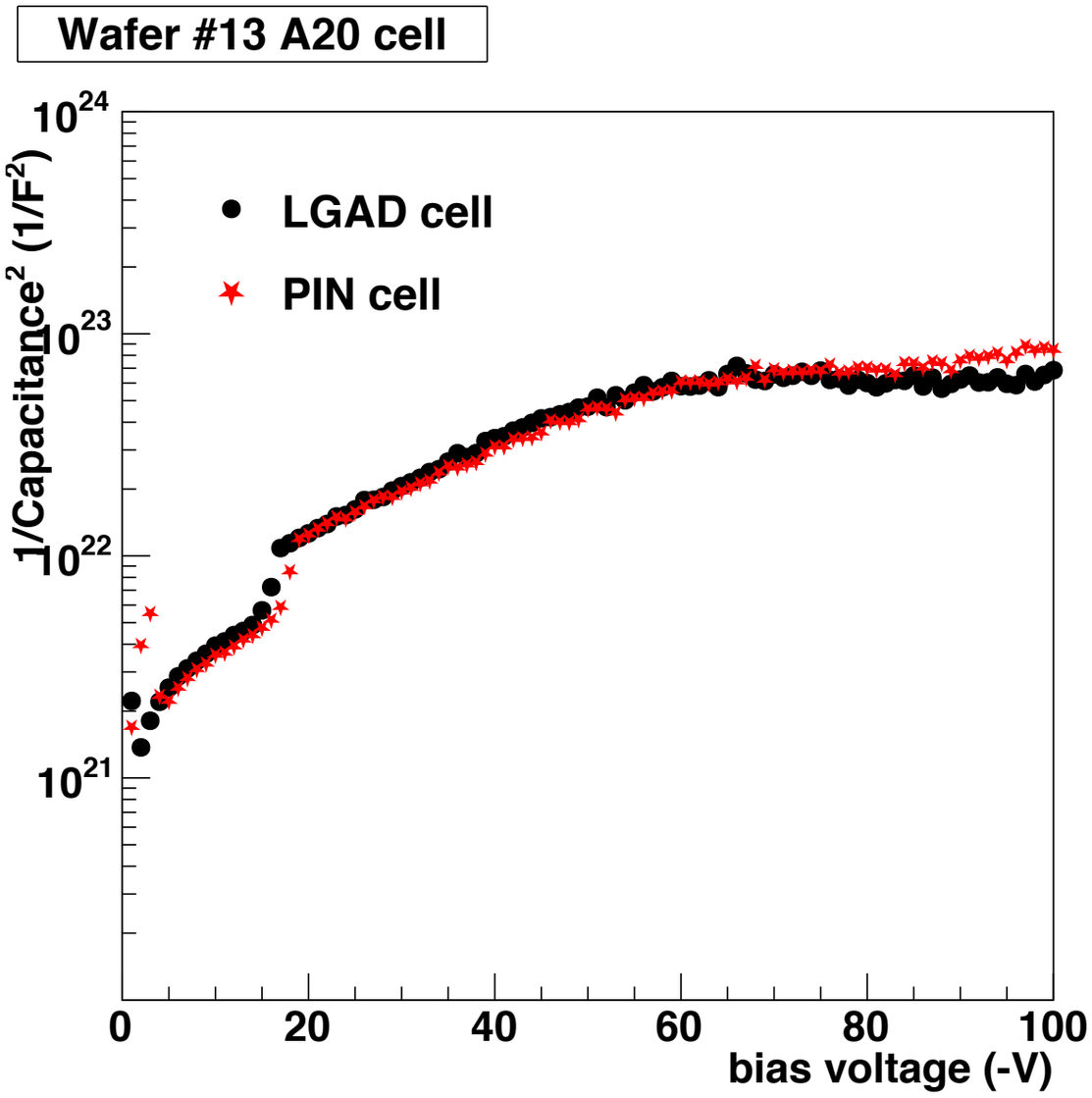


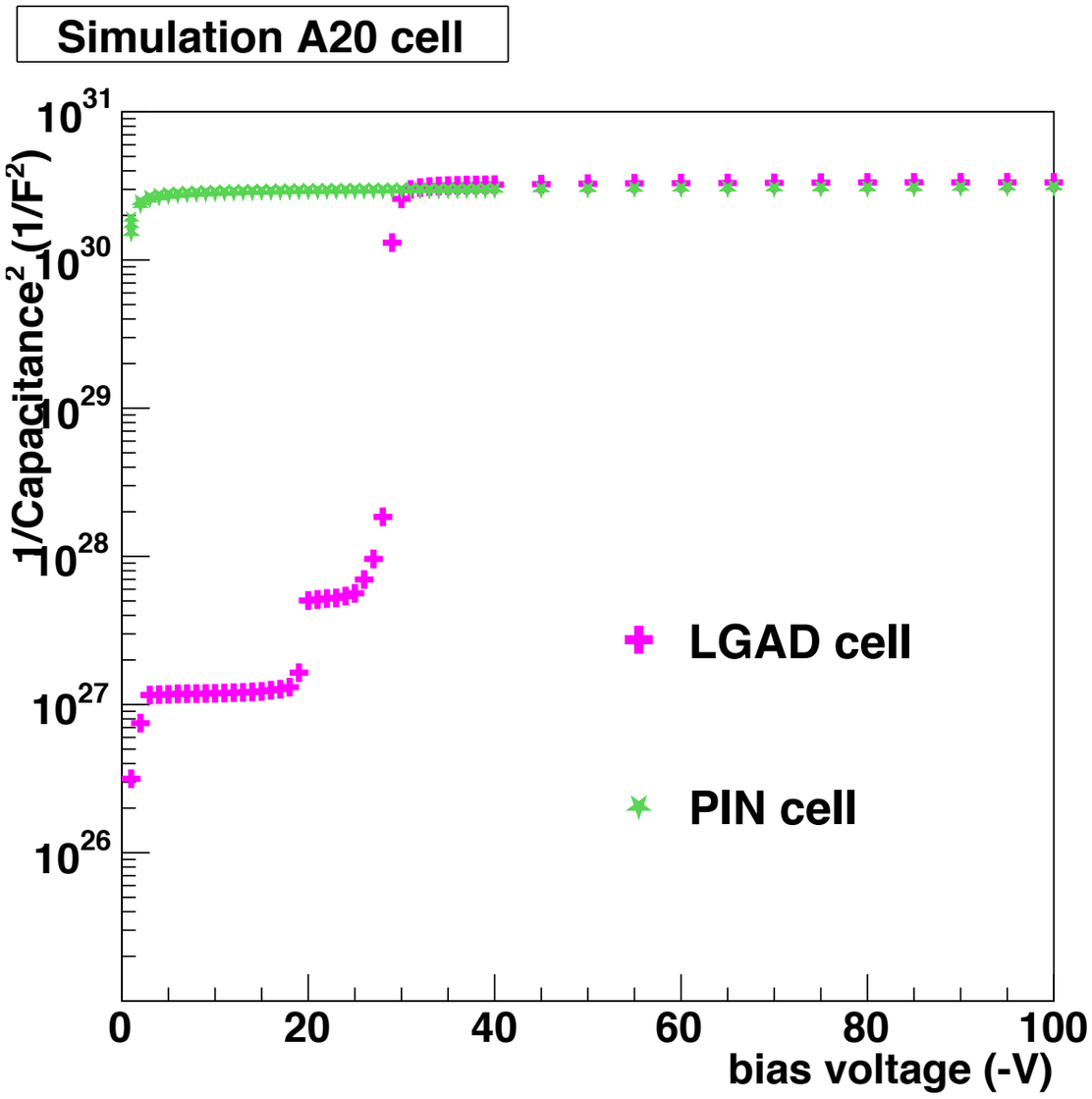
NIMA 875 (2017) 27–34

(b) CV measurement.

CV Measurement

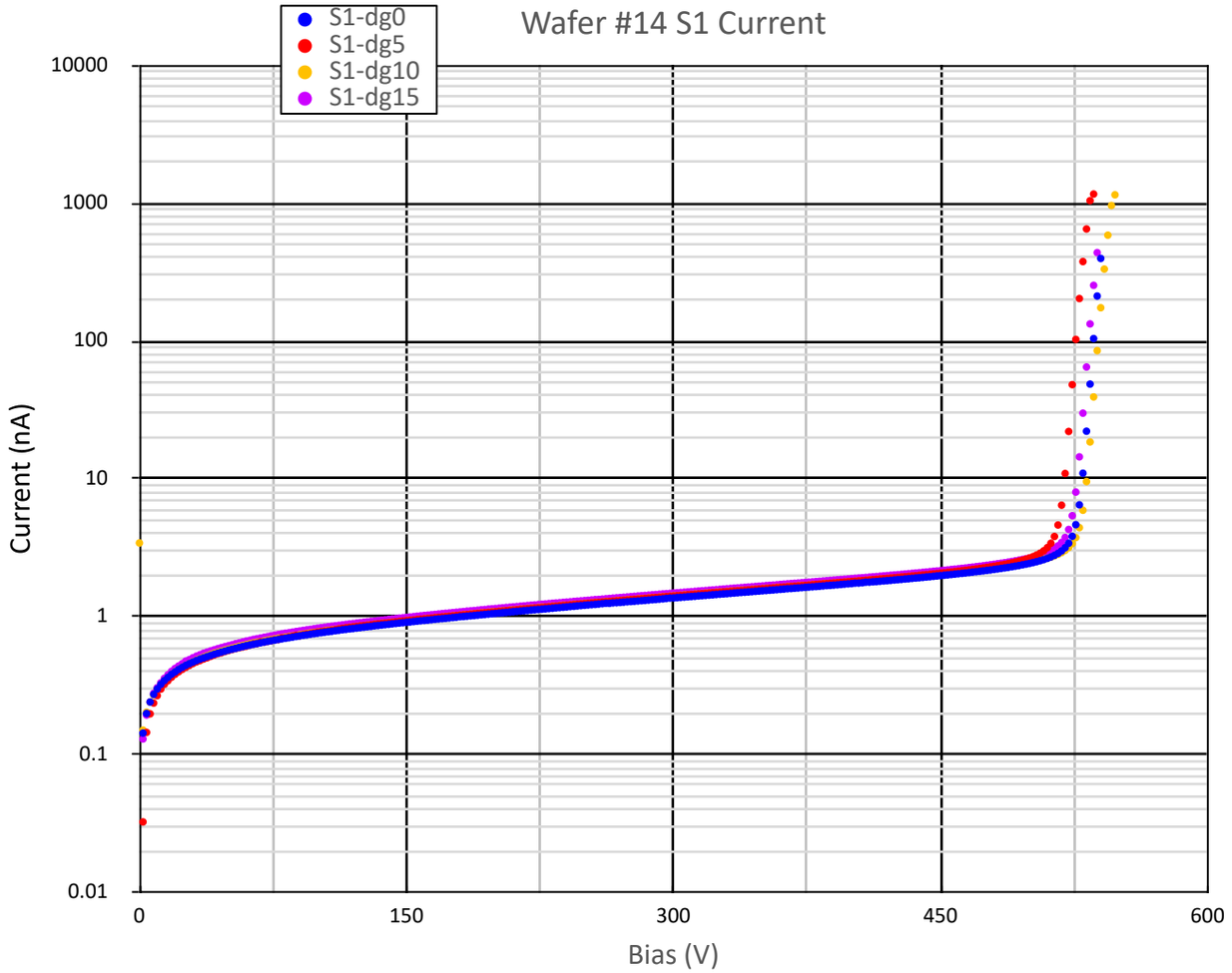
- CV measurement shows two steps but in both LGAD and PIN diode.
- A step @20V is also seen in the simulation, though not on the PIN diode.

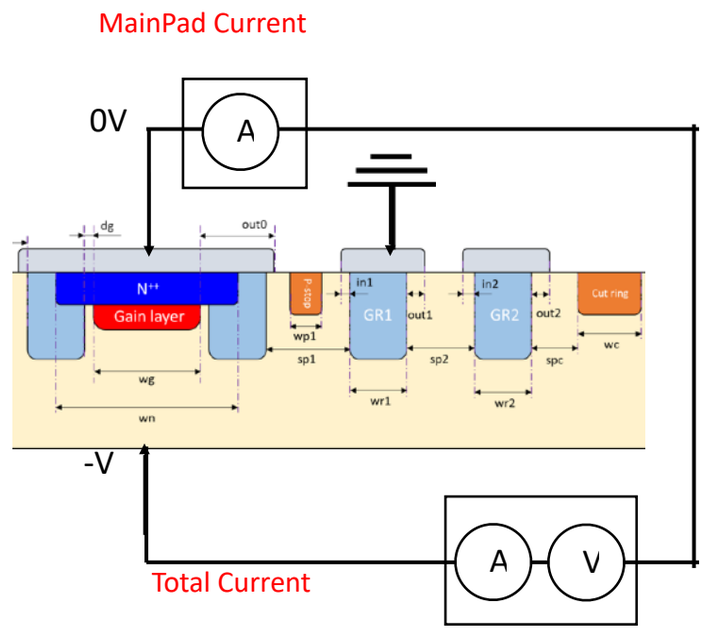




IV Measurement

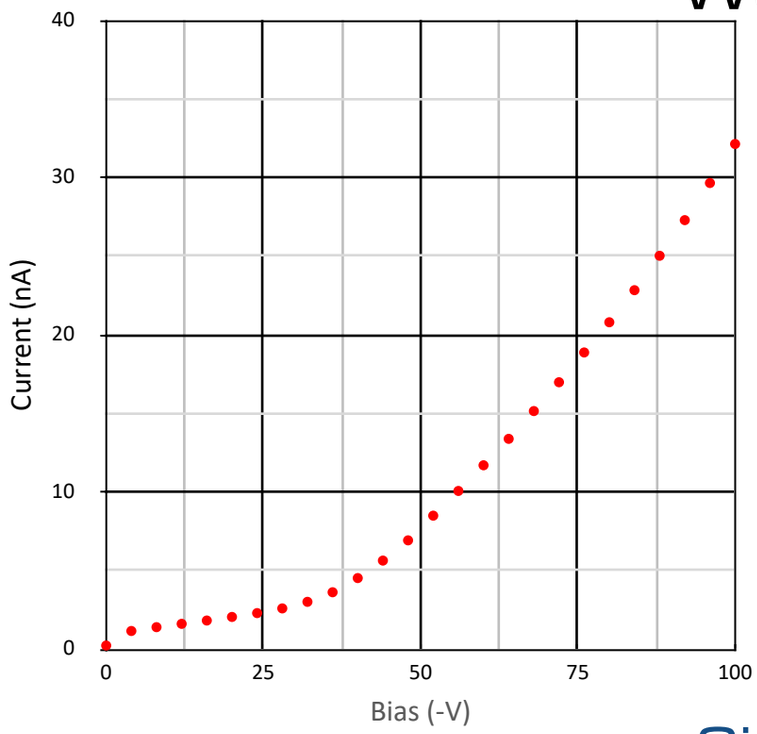
- Measure the IV for individual cells and total current.
- The breakdown voltage is low for a 625μm bulk.
- Wafers and cells have uniformity issues. The breakdown voltages and leakage currents varies among wafers and position on wafers.

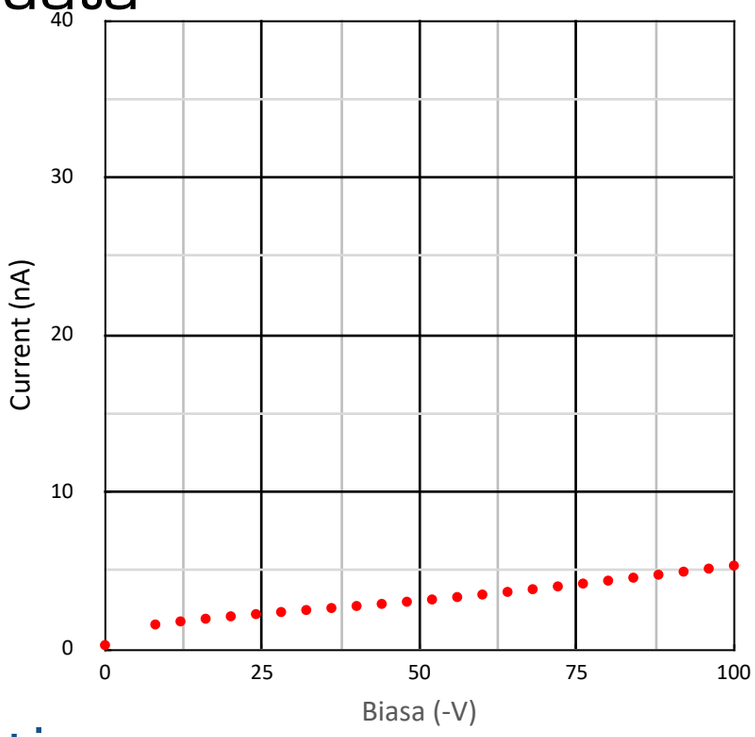




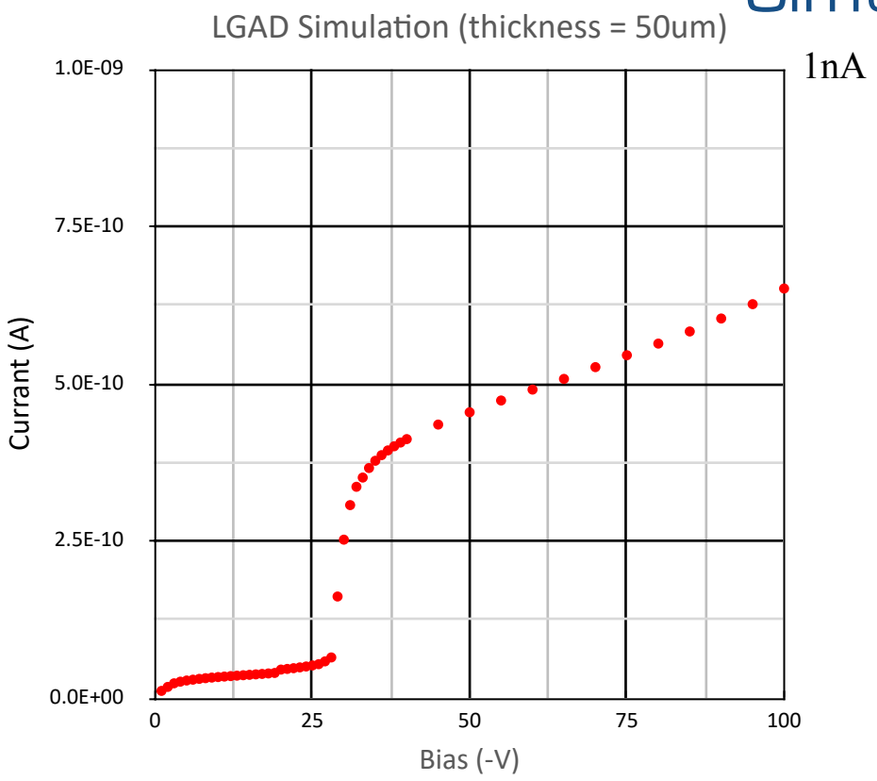
IV Comparison with Simulation

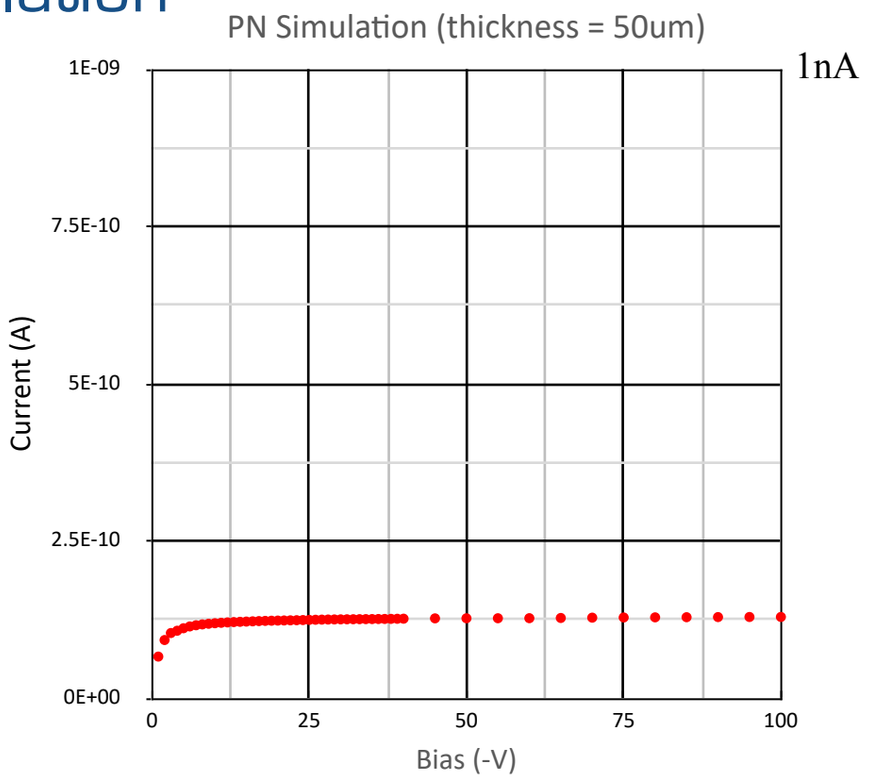
Wafer data





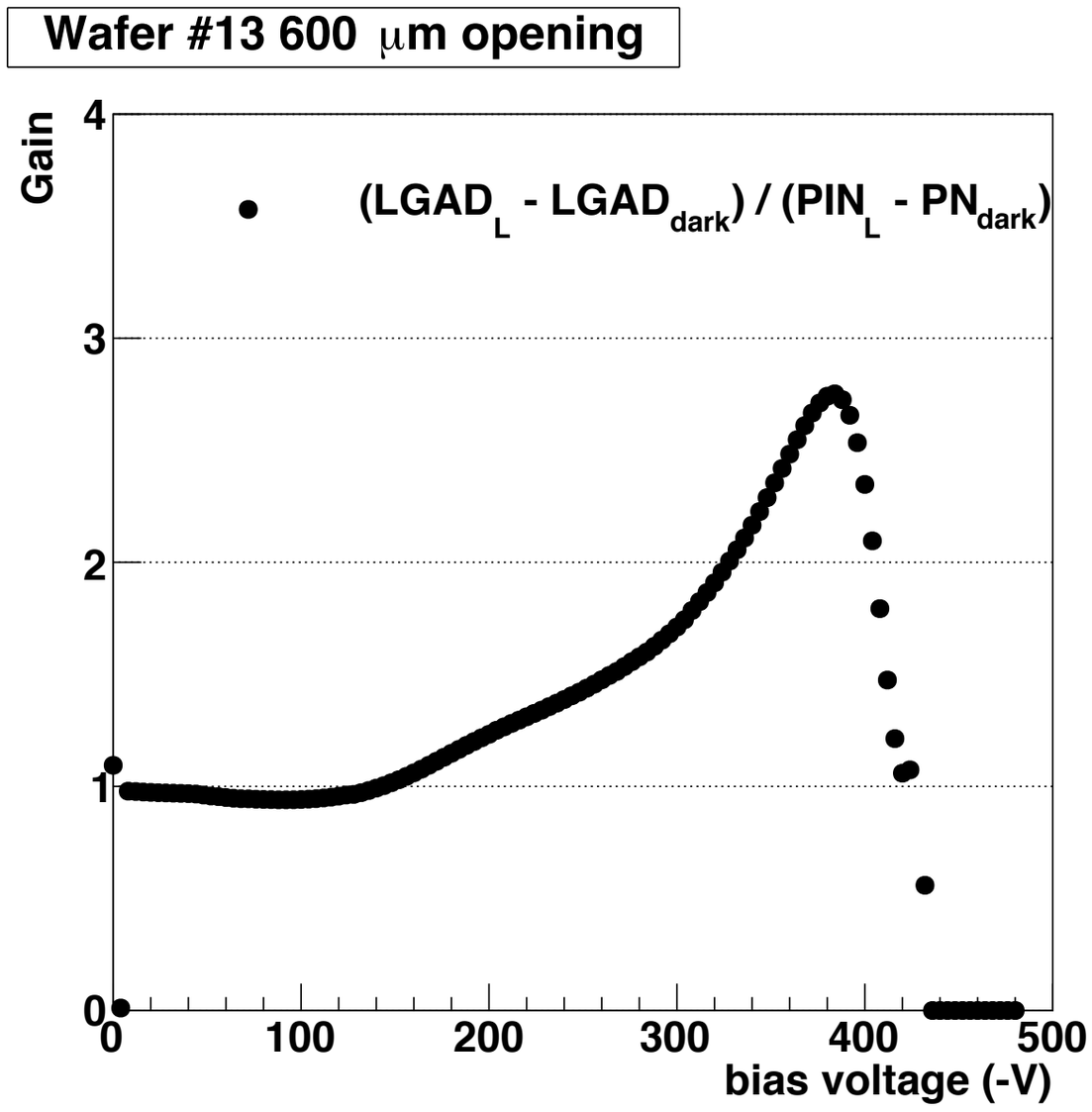
Simulation

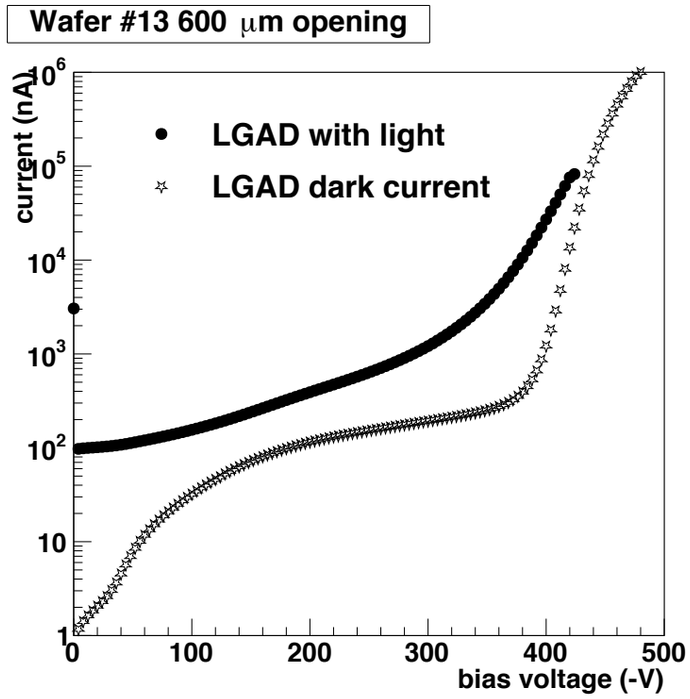


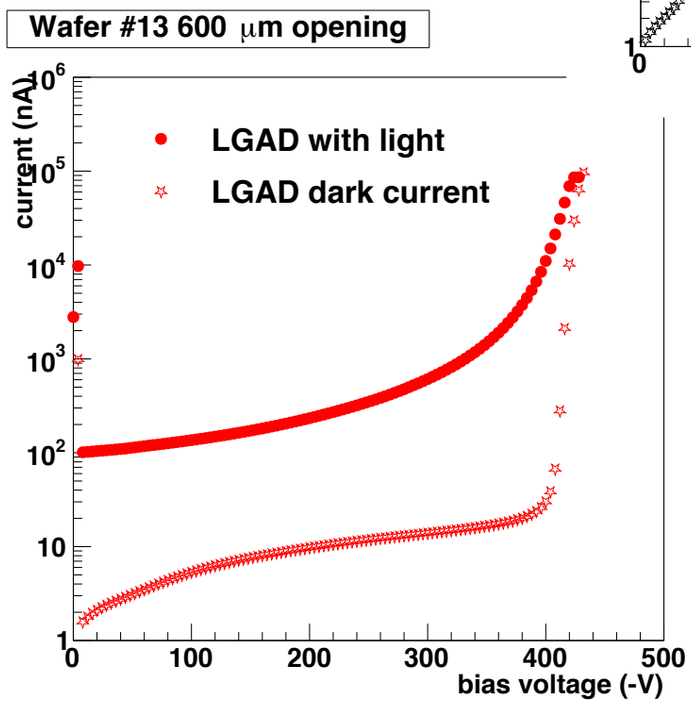


Gain Measurement

- Measure IV for LGAD and PIN with and without LED light exposure.
- Compare the dark-current-subtracted response between LGAD and PIN
- Observed enhancement of current from LGAD, though the gain is smaller than expected and later in voltage.
- Will use fluorescent light tubes and laser for gain meausrement



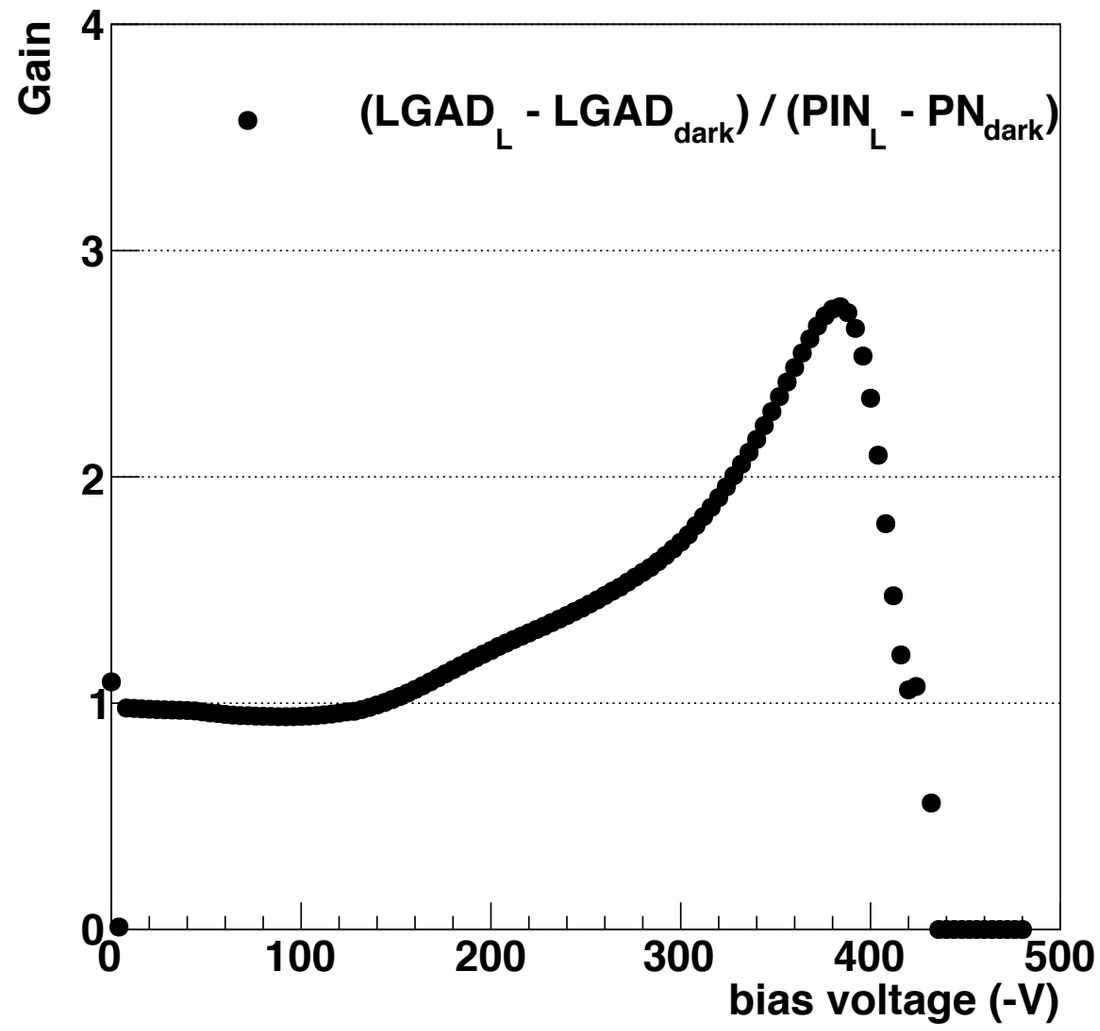




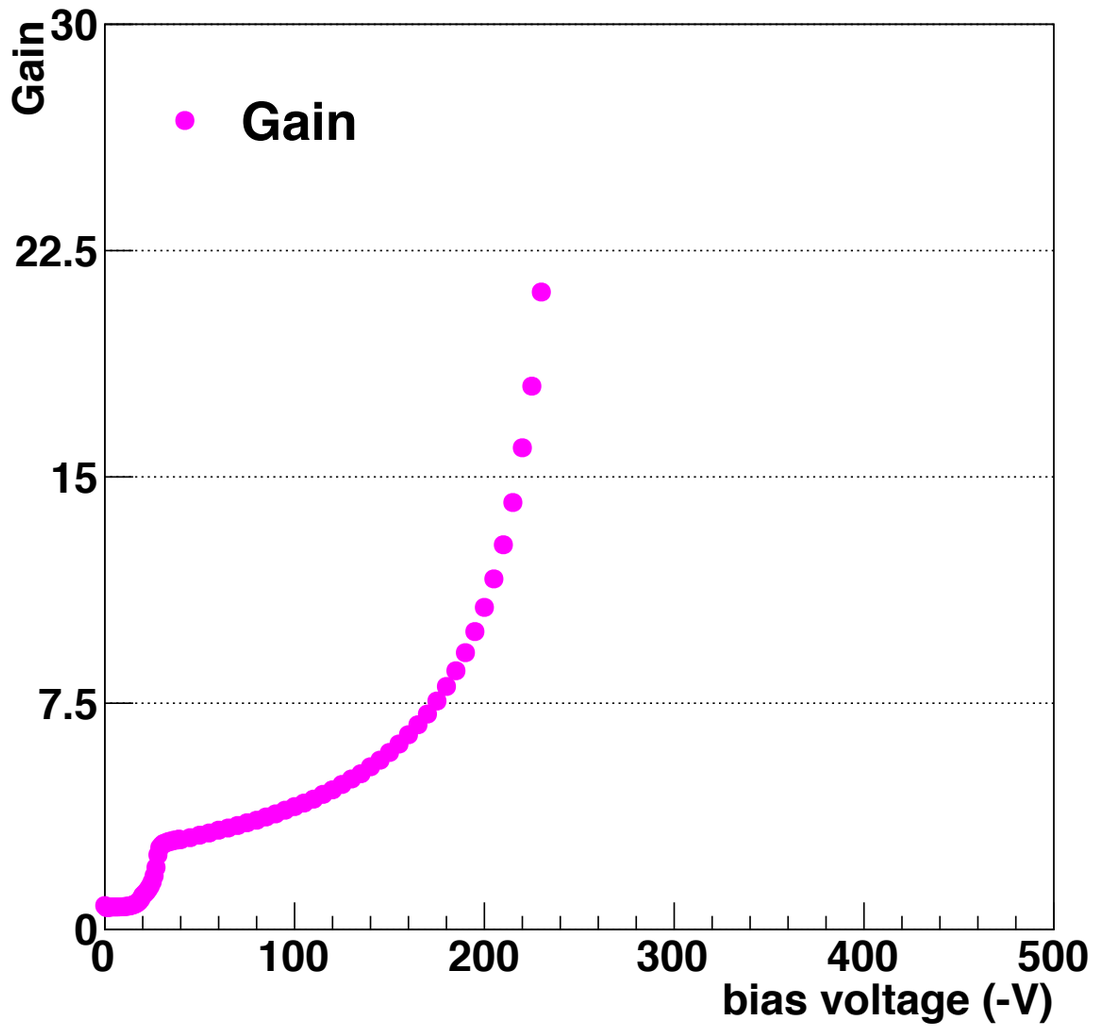
Gain Measurement

- The simulation takes 1W laser ($\lambda = 625\text{nm}$) to produce photoelectric current
- In SIM, the gain started ~30V.
- Question on the depletion depth and E-field distribution. Needs to be verified on actual wafers.

Wafer #13 600 μm opening



Simulation 600 μm opening

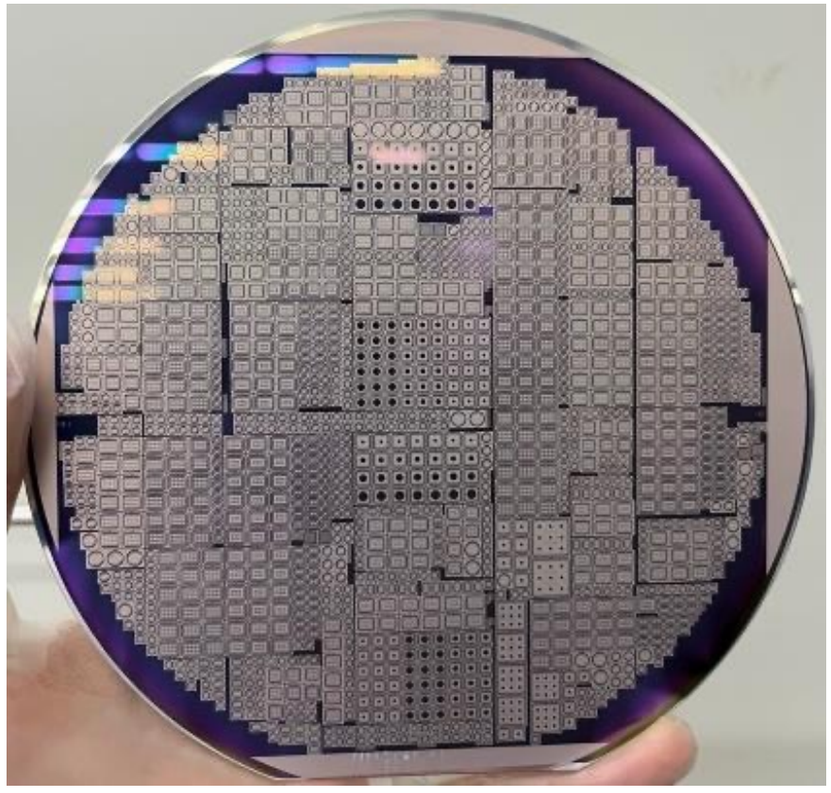


Summary

- 12 DC-LGAD wafers were produced in TSRI
- Various measurements were performed. The characteristic of LGAD cell is not understood and different from expected in Simulation
- Will use infrared laser to measure gain.
- Detail studies of doping concentration and implant structure will be done.
- Uniformity of wafers produced in TSRI is not great. Will also look for mature FAB for production.
- Will produce AC-LGAD sensor as well.

Backup

- The color pattern came from the passivation thickness.
- The metal layer was clear.



- Test wafer (in metal etch)