Contributions to the ePIC DAQ Project

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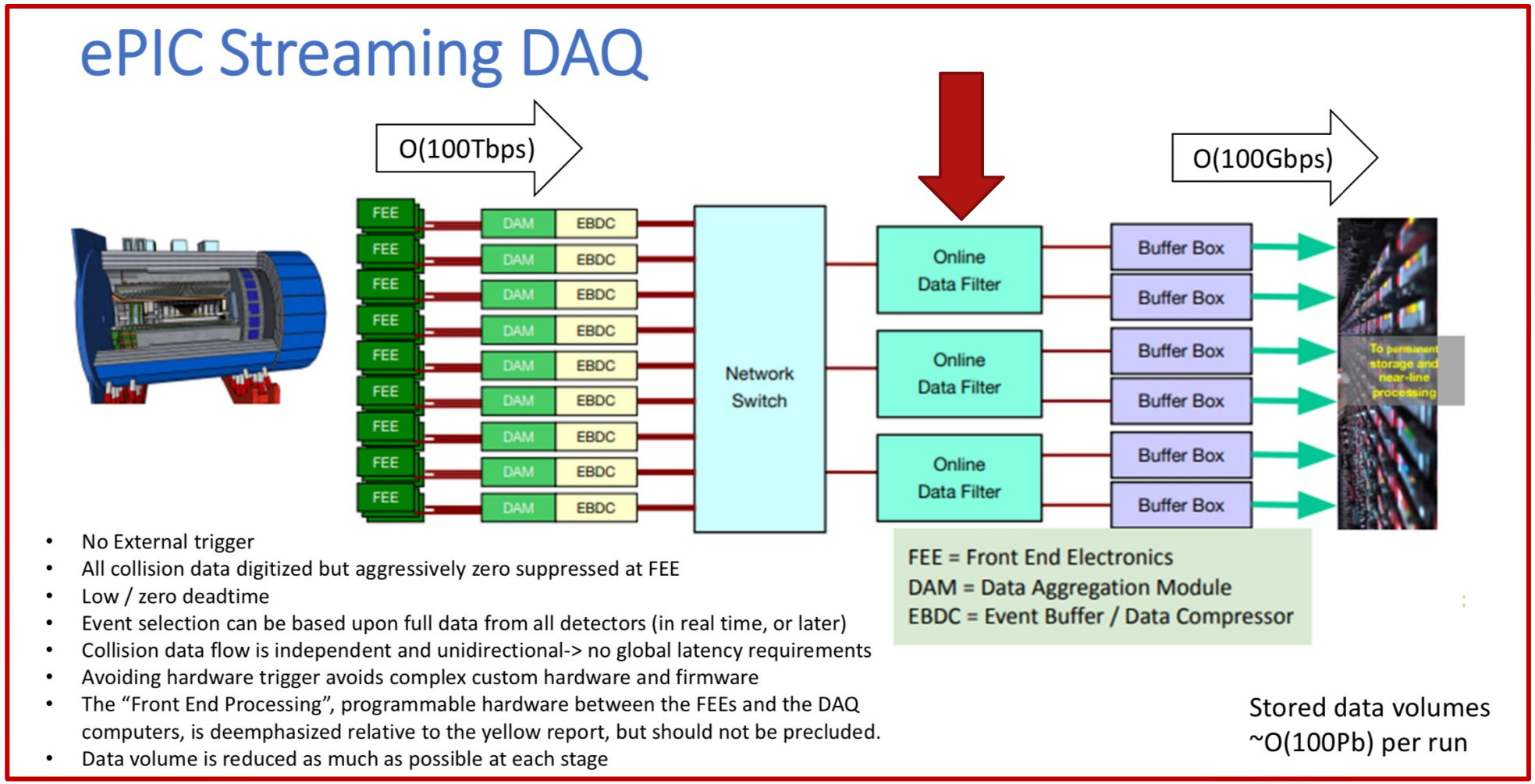
Outline

- Free Streaming Readout
- ALICE O2
- Some (small) activities
- SPADI-Alliance
- Summary

Free Streaming Readout

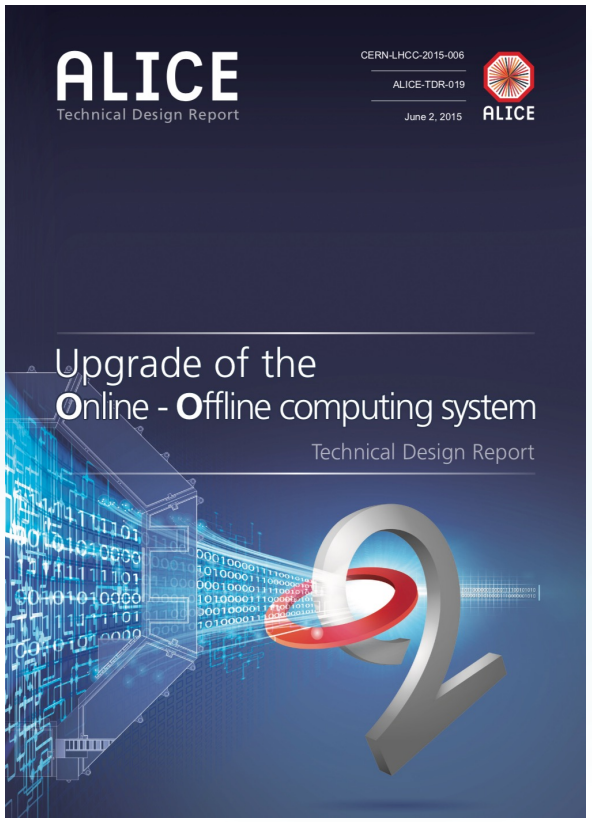
- **Will be a future standard DAQ system**

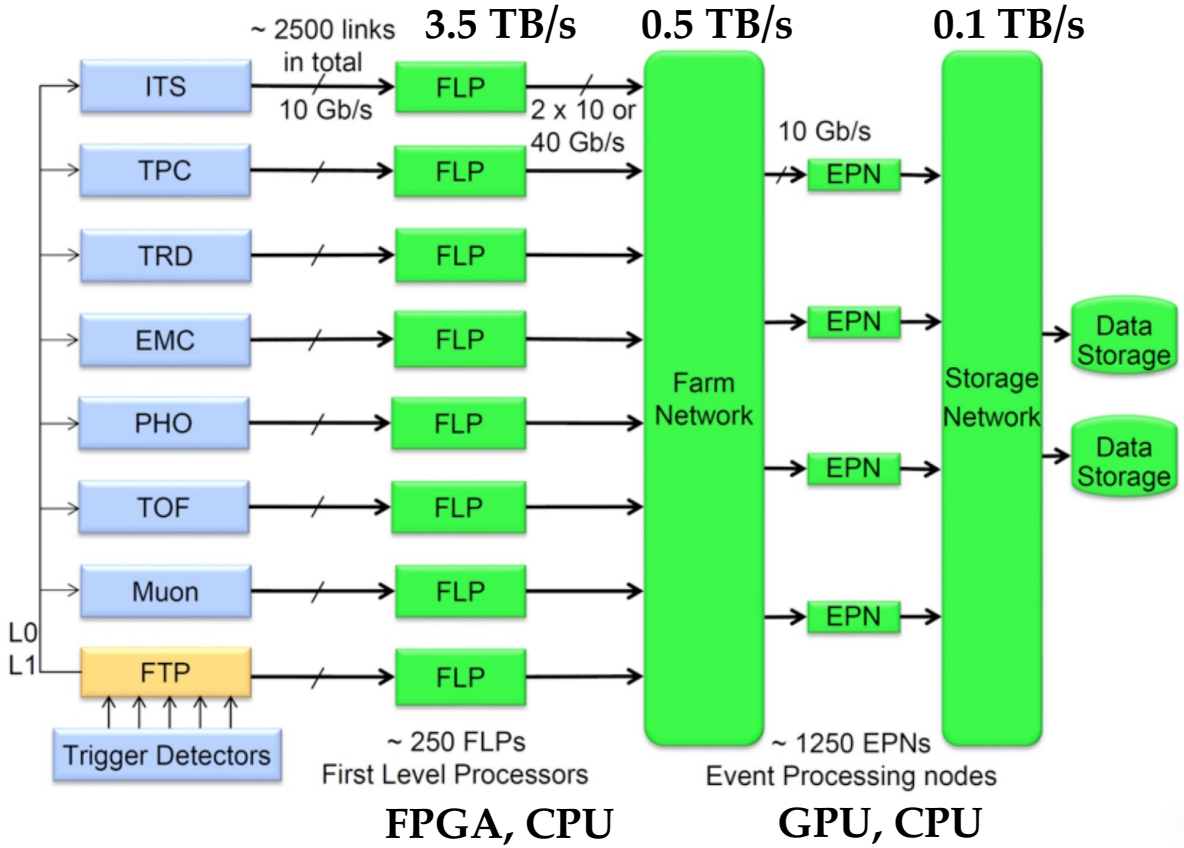


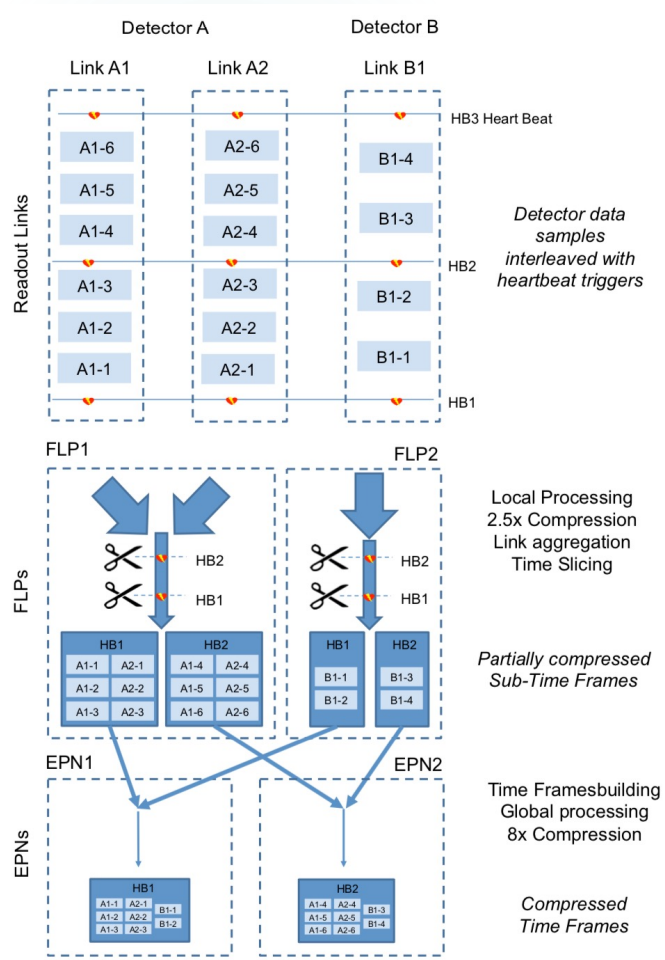
- No External trigger
- All collision data digitized but aggressively zero suppressed at FEE
- Low / zero deadtime
- Event selection can be based upon full data from all detectors (in real time, or later)
- Collision data flow is independent and unidirectional-> no global latency requirements
- Avoiding hardware trigger avoids complex custom hardware and firmware
- The “Front End Processing”, programmable hardware between the FEEs and the DAQ computers, is deemphasized relative to the yellow report, but should not be precluded.
- Data volume is reduced as much as possible at each stage

ALICE O² system

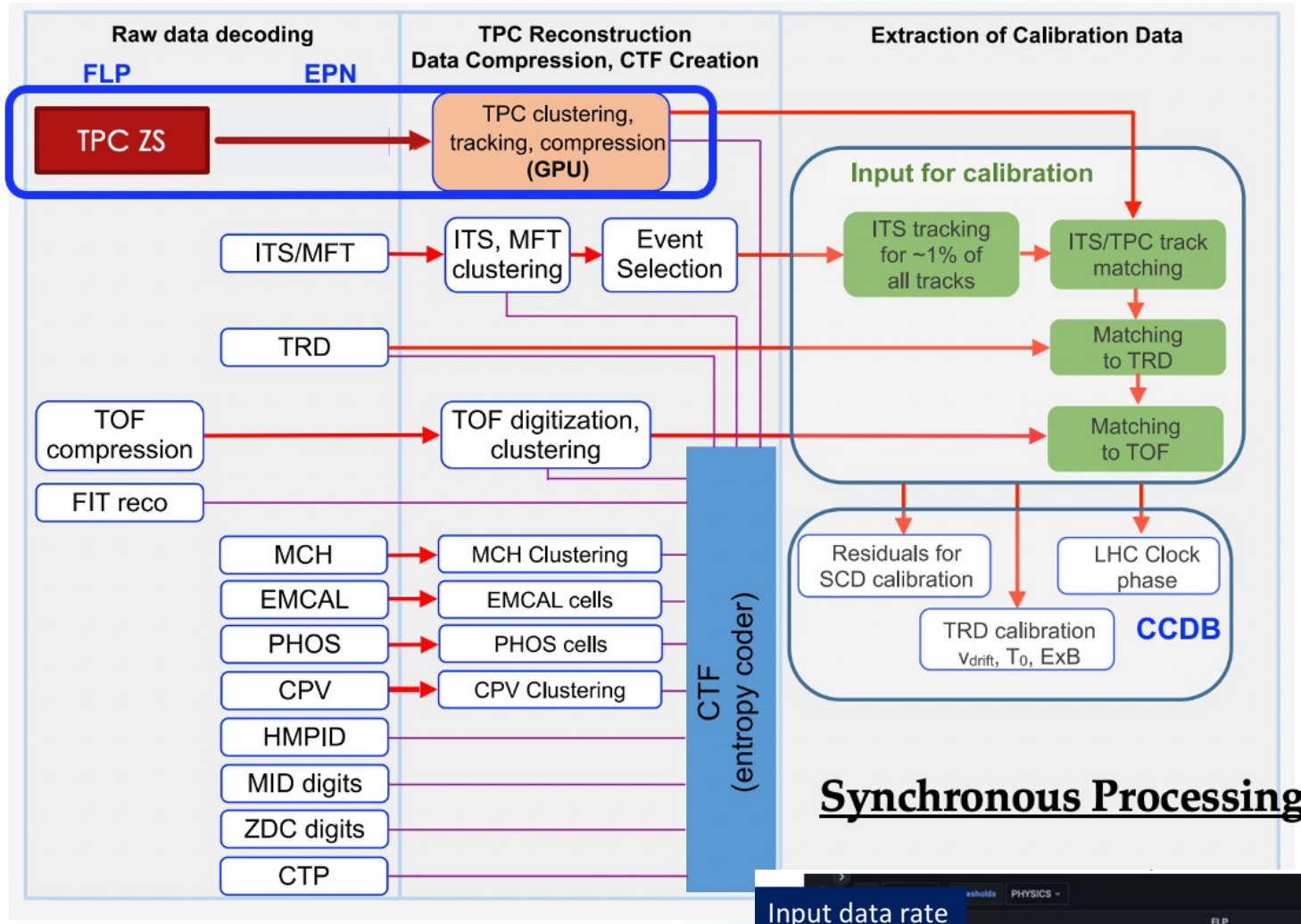
50kHz Pb-Pb collisions
TPC moved from triggered readout (gating grid) to continuous readout with GEMs
ALICE had experiences on hardware accelaration (GPUs) in HLT during Run2
→ New Free streaming DAQ (O²) proposed in 2015



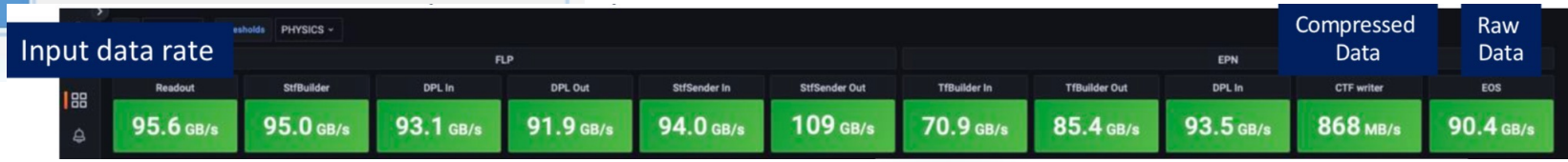




Online processing in ALICE O²



8 GPU/EPN, 250 EPNs

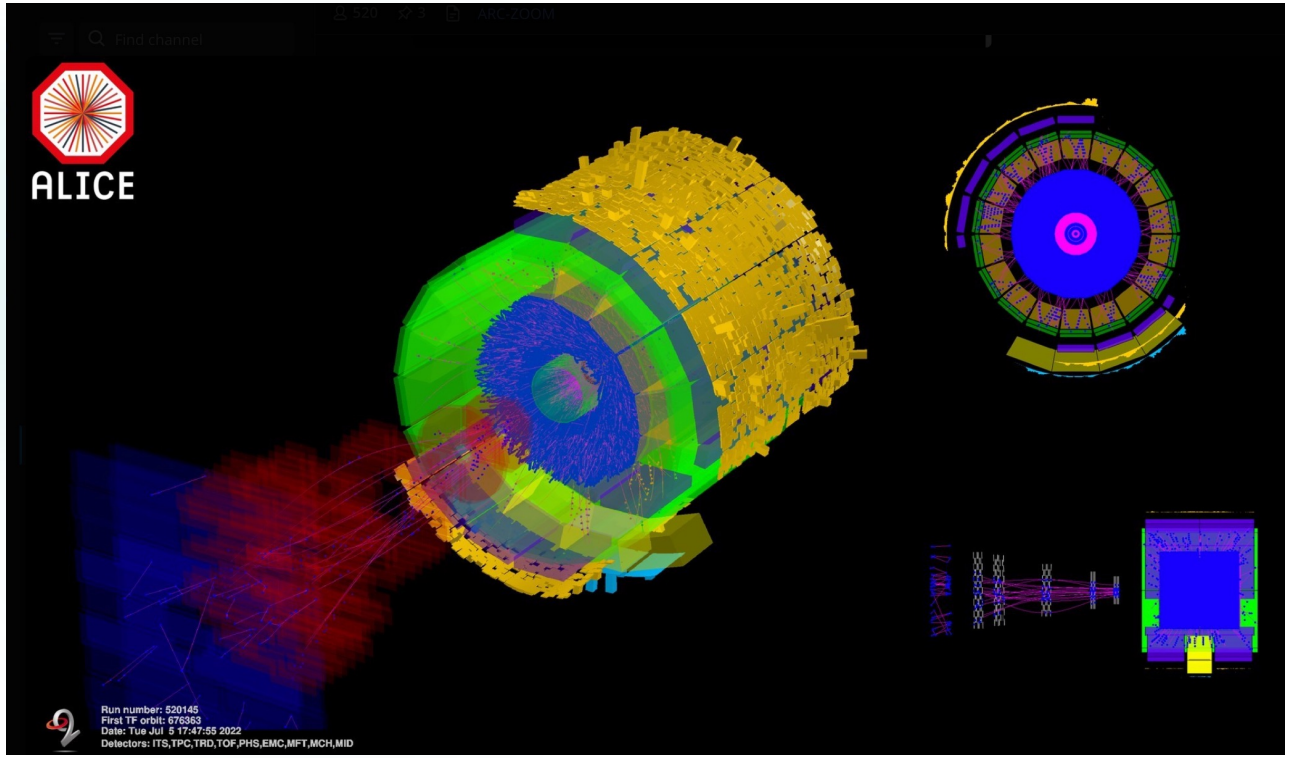


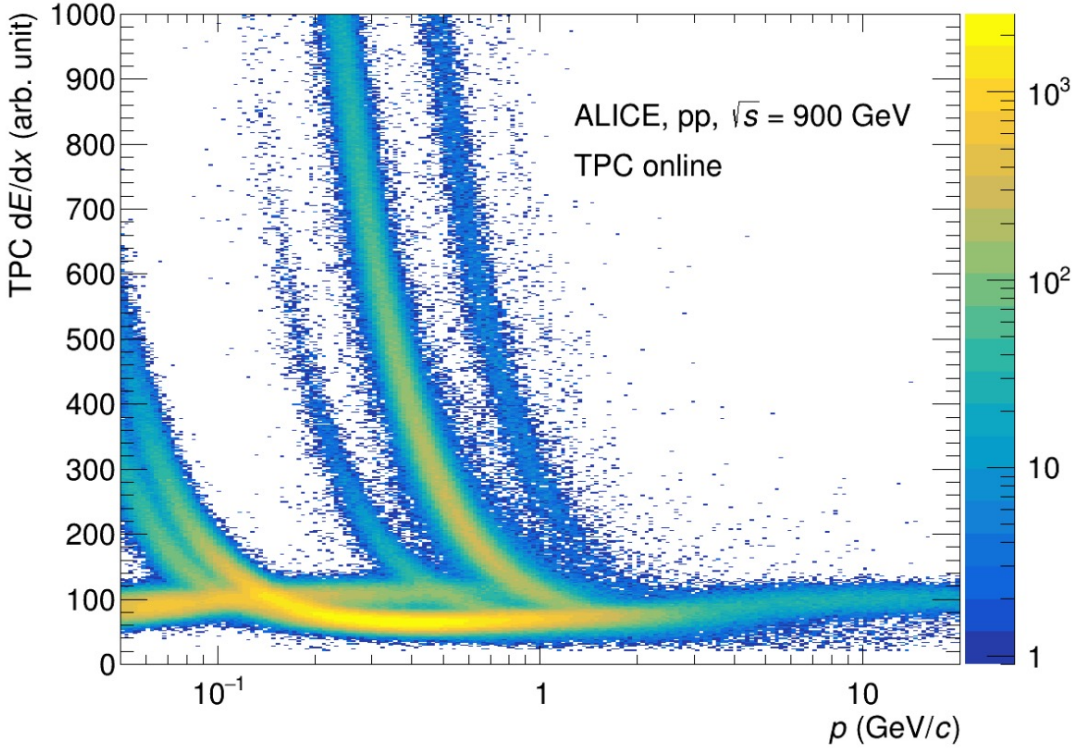
Online processing performance

- **Online clustering, tracking, PID**

All are done ONLINE

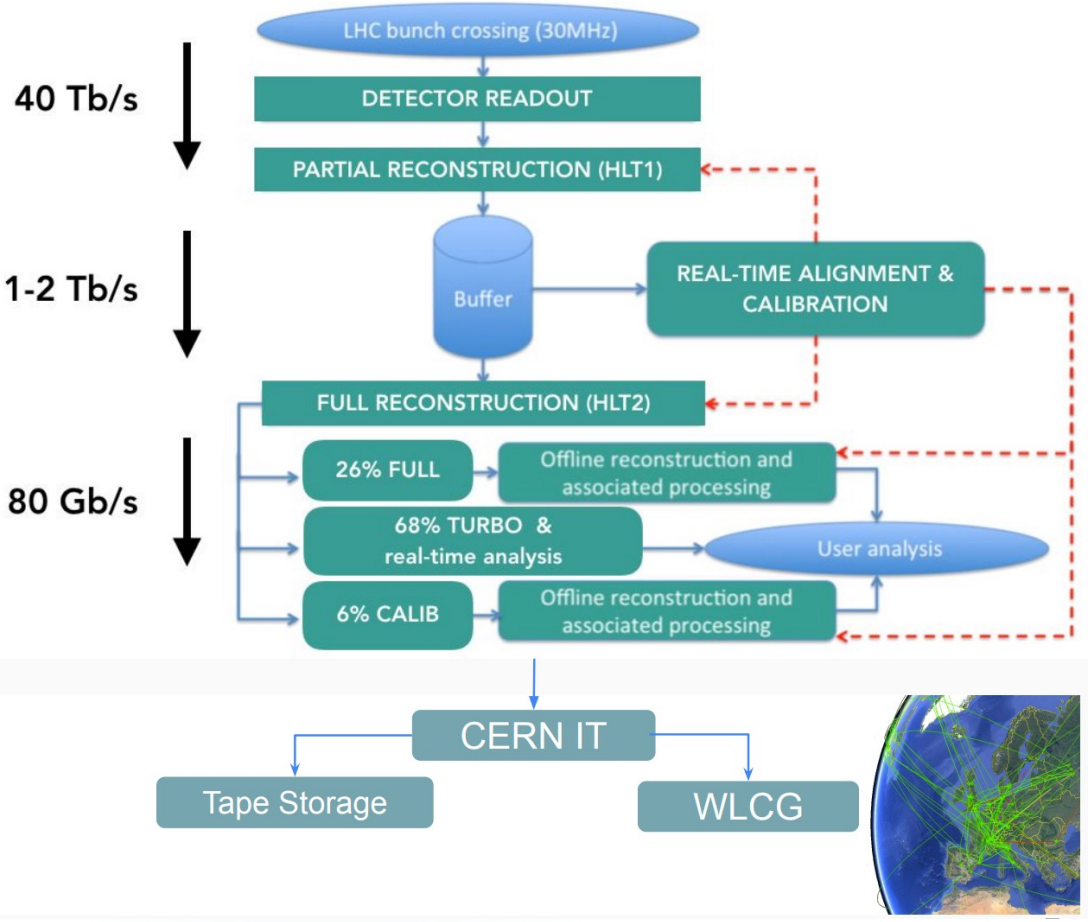
Event display after online reconstruction
1 TF = 11.5 ms, 10 kHz IR → ~100 collisions

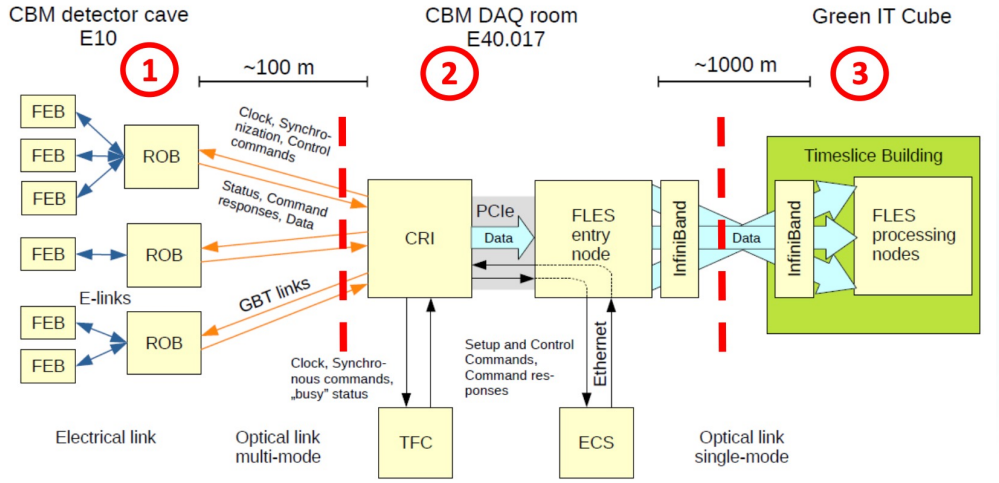


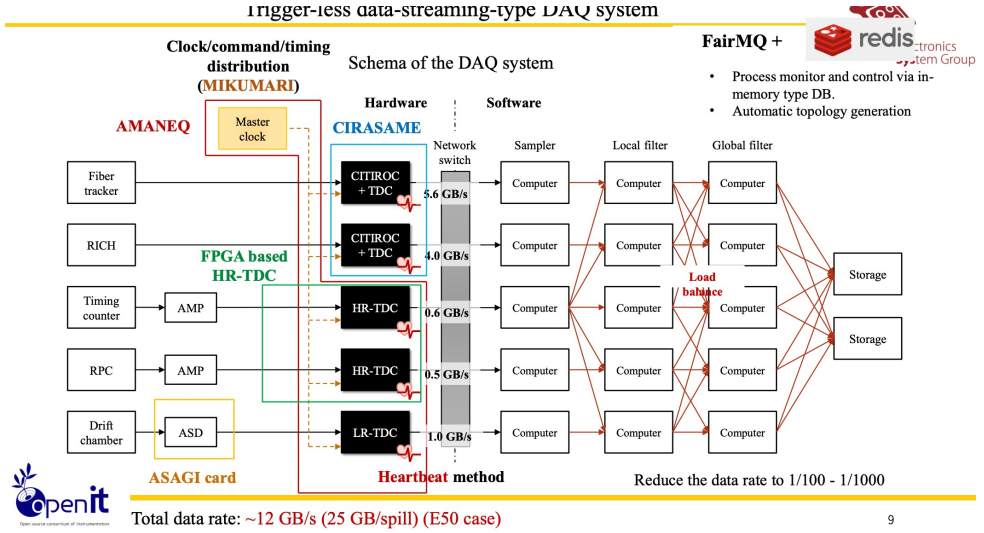


Will be used in many experiments

- ALICE, LHCb, sPHENIX, CBM, J-lab, J-PARC, etc…





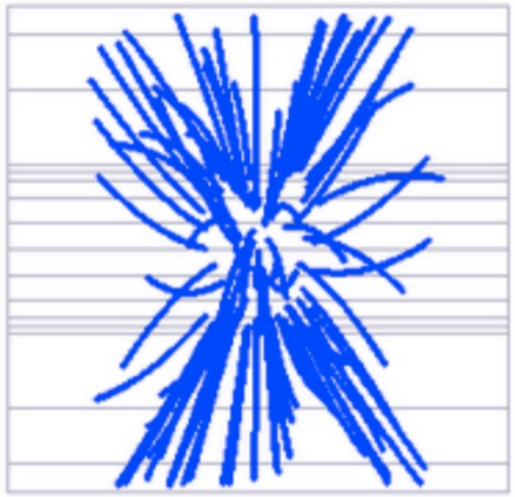


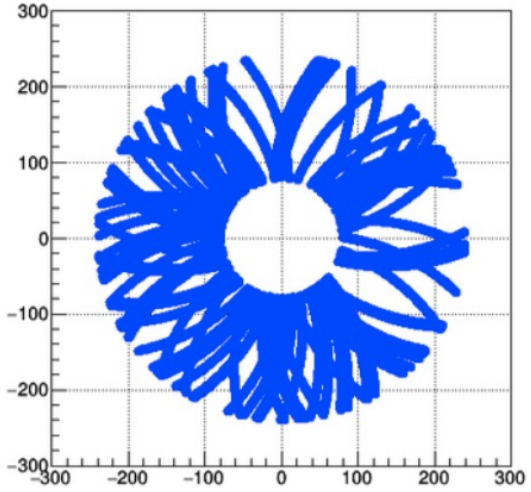
My activities: GPU processing

- **Kalman filter tracking**
- **ML for pile-up identification**

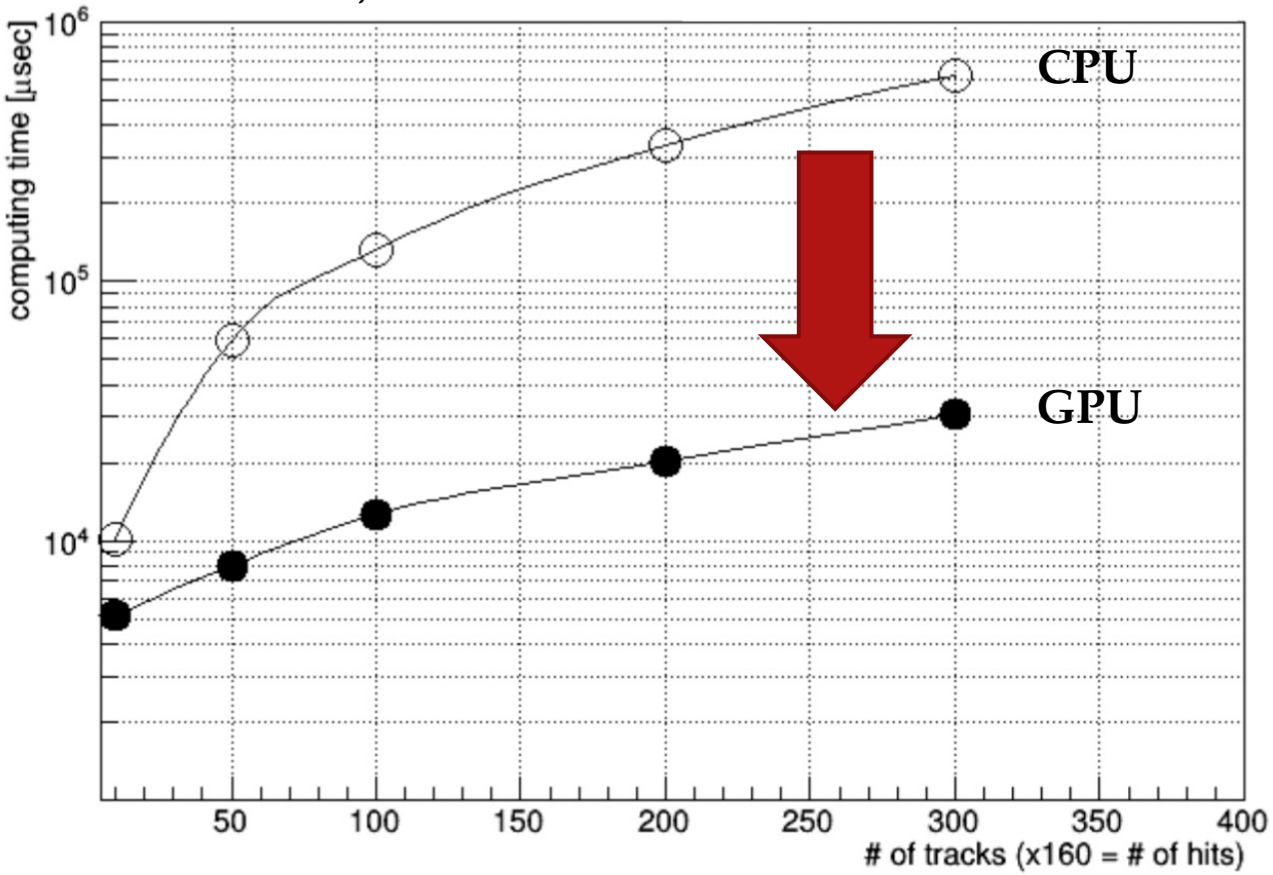
These works were done in 2016.

TPC Tracking



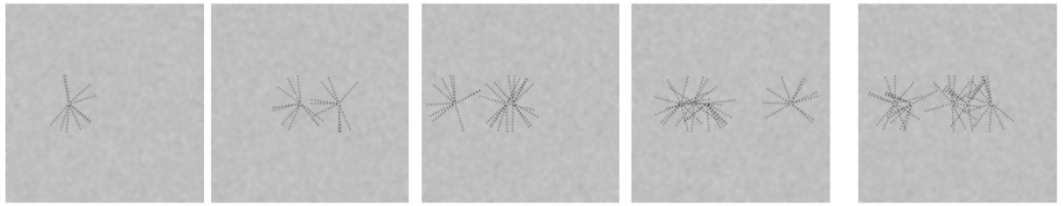


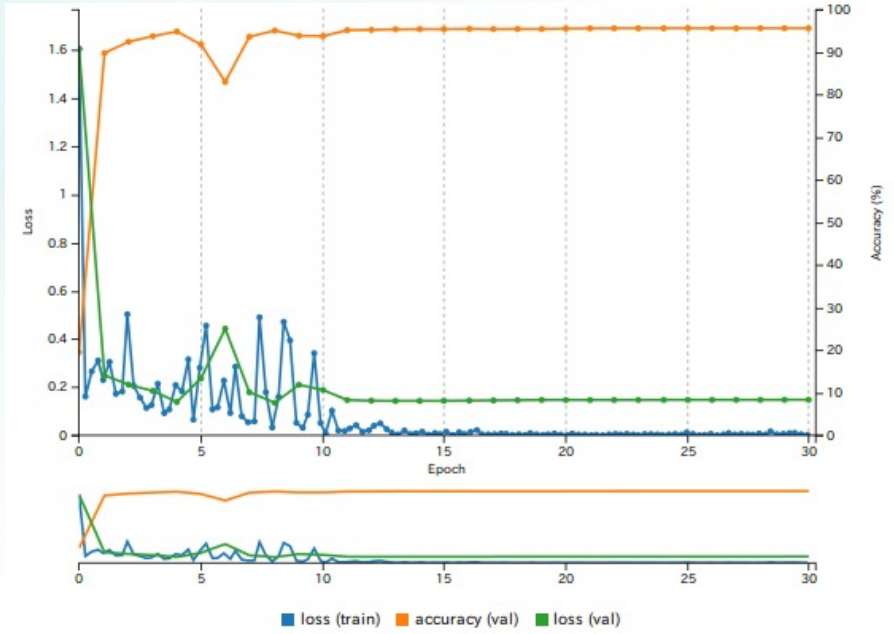
GPU = NVIDIA GTX970
CUDA 7.5, 8.0



My activities: GPU processing

- Kalman filter in GPU
- ML for pile-up identification



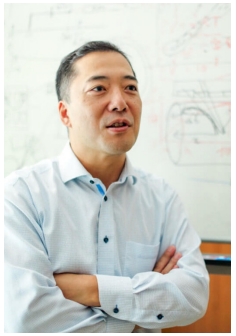


LeNET(vtxtmp) Image Classification Model

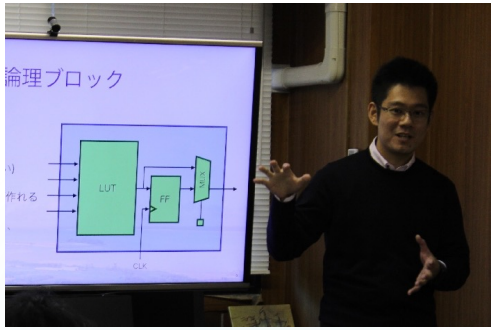
Path	Top predictions
/home/gunji/NVIDIA_CUDA-7.5_Samples/deep_learning/tmp/vtxtmp/test/1/0000.png	1 100.0% 2 0.0% 3 0.0% 4 0.0% 5 0.0%
/home/gunji/NVIDIA_CUDA-7.5_Samples/deep_learning/tmp/vtxtmp/test/2/0000.png	2 100.0% 1 0.0% 3 0.0% 4 0.0% 5 0.0%
/home/gunji/NVIDIA_CUDA-7.5_Samples/deep_learning/tmp/vtxtmp/test/3/0000.png	3 99.99% 4 0.01% 2 0.0% 1 0.0% 5 0.0%
/home/gunji/NVIDIA_CUDA-7.5_Samples/deep_learning/tmp/vtxtmp/test/4/0000.png	4 99.99% 5 0.01% 3 0.0% 2 0.0% 1 0.0%
/home/gunji/NVIDIA_CUDA-7.5_Samples/deep_learning/tmp/vtxtmp/test/5/0000.png	5 100.0% 4 0.0% 1 0.0% 3 0.0% 2 0.0%
/home/gunji/NVIDIA_CUDA-7.5_Samples/deep_learning/tmp/vtxtmp/test/1/0001.png	1 100.0% 2 0.0% 3 0.0% 4 0.0% 5 0.0%
/home/gunji/NVIDIA_CUDA-7.5_Samples/deep_learning/tmp/vtxtmp/test/2/0001.png	2 100.0% 1 0.0% 3 0.0% 4 0.0% 5 0.0%
/home/gunji/NVIDIA_CUDA-7.5_Samples/deep_learning/tmp/vtxtmp/test/3/0001.png	3 99.92% 2 0.08% 4 0.0% 1 0.0% 5 0.0%
/home/gunji/NVIDIA_CUDA-7.5_Samples/deep_learning/tmp/vtxtmp/test/4/0001.png	4 99.8% 5 0.2% 3 0.0% 2 0.0% 1 0.0%
/home/gunji/NVIDIA_CUDA-7.5_Samples/deep_learning/tmp/vtxtmp/test/5/0001.png	5 100.0% 4 0.0% 3 0.0% 1 0.0% 2 0.0%
/home/gunji/NVIDIA_CUDA-7.5_Samples/deep_learning/tmp/vtxtmp/test/1/0002.png	1 100.0% 2 0.0% 3 0.0% 4 0.0% 5 0.0%
/home/gunji/NVIDIA_CUDA-7.5_Samples/deep_learning/tmp/vtxtmp/test/2/0002.png	2 100.0% 3 0.0% 1 0.0% 4 0.0% 5 0.0%
/home/gunji/NVIDIA_CUDA-7.5_Samples/deep_learning/tmp/vtxtmp/test/3/0002.png	3 99.92% 2 0.08% 4 0.0% 1 0.0% 5 0.0%
/home/gunji/NVIDIA_CUDA-7.5_Samples/deep_learning/tmp/vtxtmp/test/4/0002.png	4 54.47% 5 45.53% 3 0.0% 1 0.0% 2 0.0%
/home/gunji/NVIDIA_CUDA-7.5_Samples/deep_learning/tmp/vtxtmp/test/5/0002.png	5 99.42% 4 0.58% 3 0.0% 1 0.0% 2 0.0%

TPC cluster finder in FPGA

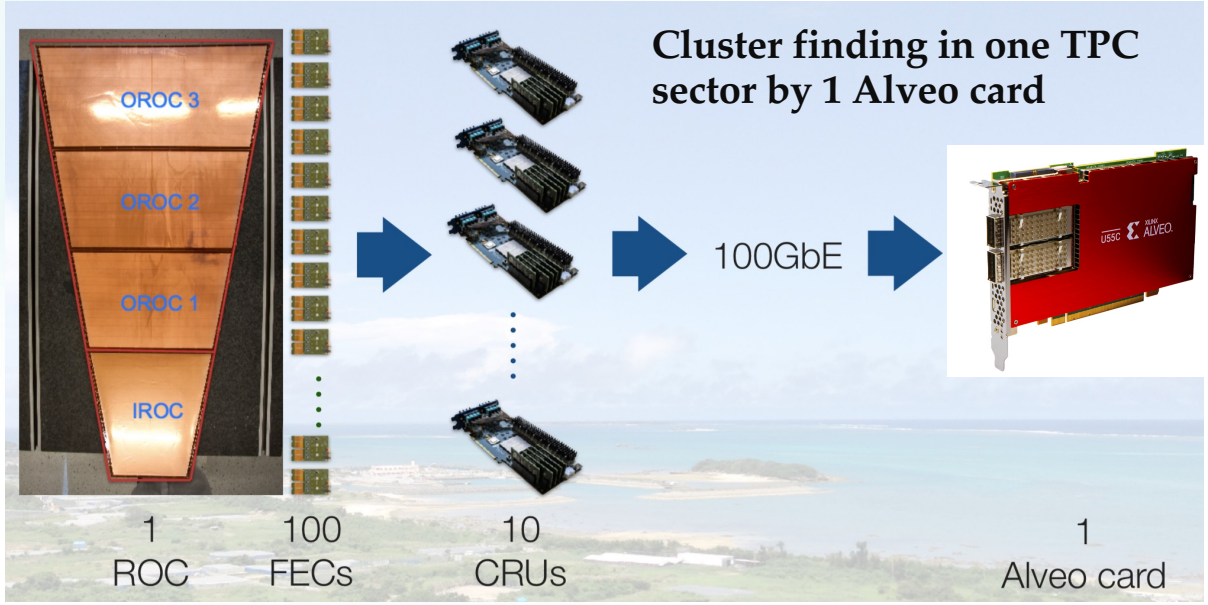
- ALICE TPC clustering on FPGA
  - Xilinx Alveo u55c, u280
  - High Level Synthesis (C++)



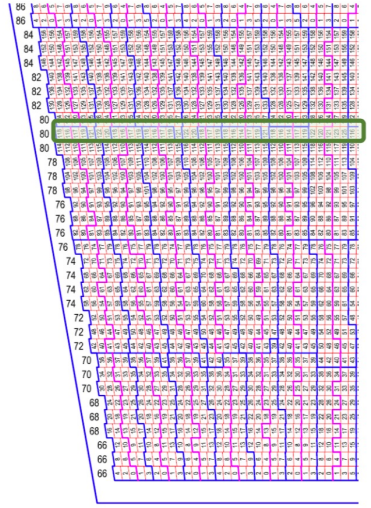
Ken Oyama (NiAS)

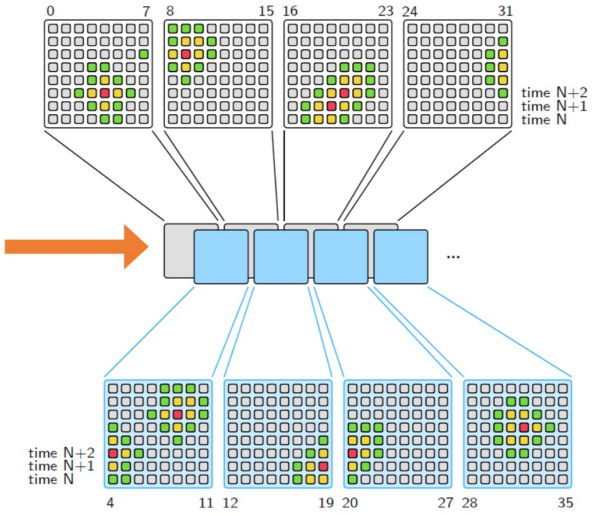


Yasunori Osana (Rukyu -> Komamoto)



- The heaviest processing in our FPGA
- find local maxima in pad-timebin 2D space
- processor modules
  - scan rectangular regions
  - optimize size v.s. number of processors
  - available clock cycle is the boundary condition

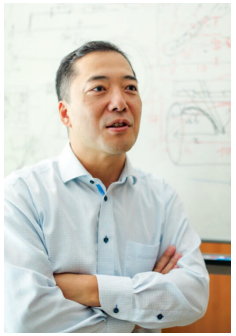




S. Klewin's PhD thesis, Heidelberg

TPC cluster finder in FPGA

- ALICE TPC clustering on FPGA
  - Xilinx Alveo u55c, u280
  - High Level Synthesis (C++)



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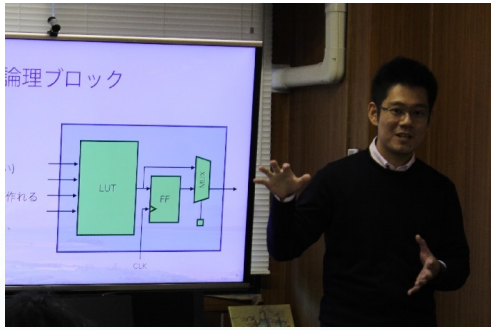

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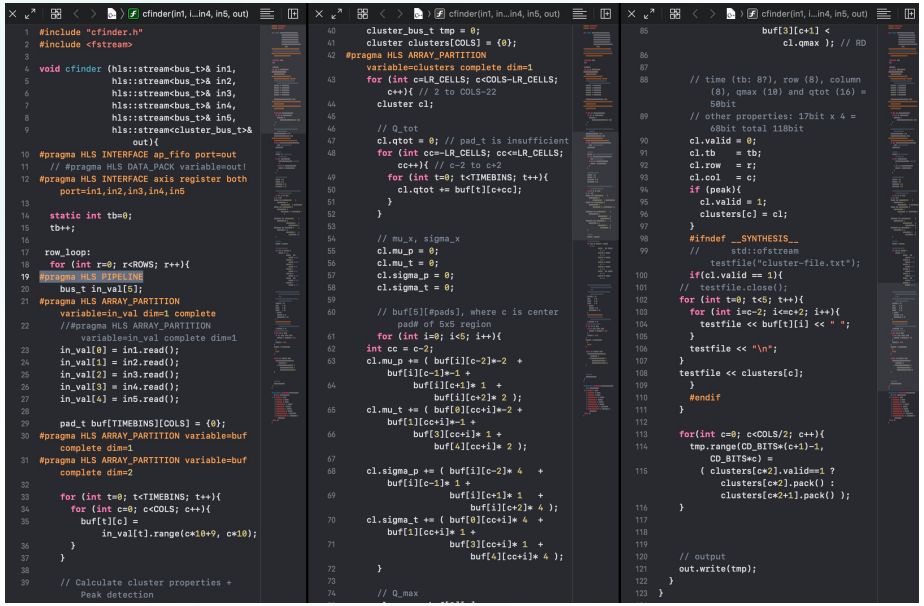
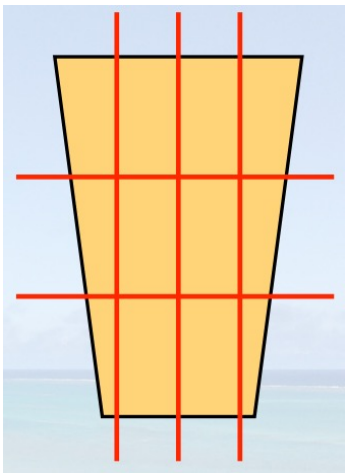
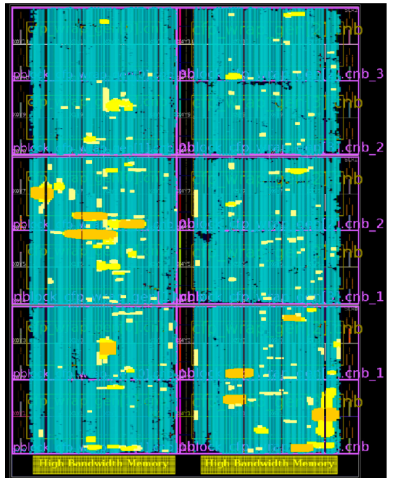




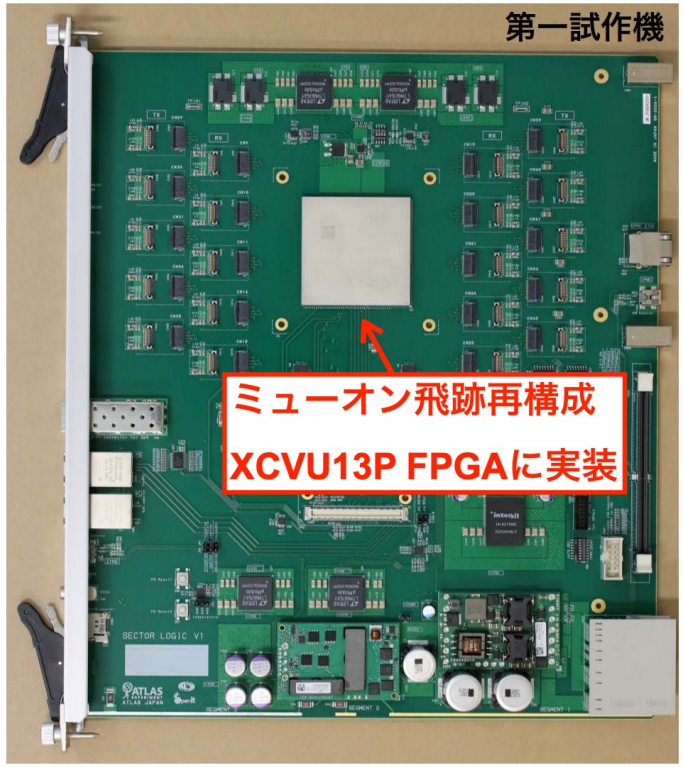


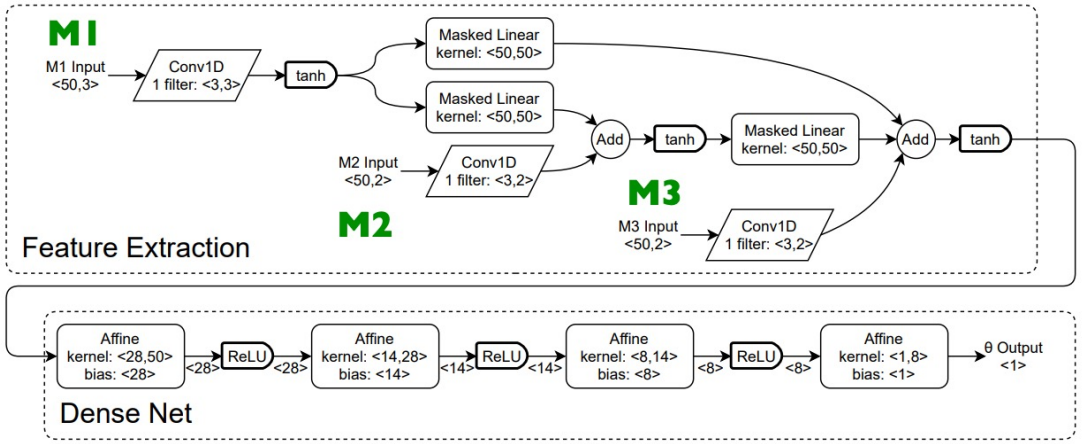
U55で10 CRU分が入った
290MHzで動作 → 5MSPSに対して58 clock

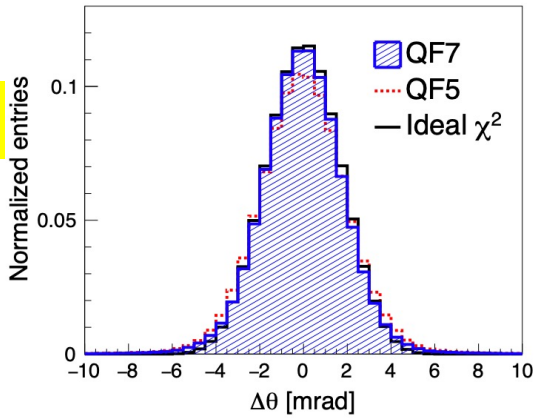
	Used	Available	%
LUT	714,307	1,303,680	54.8
FF	814,523	2,607,360	31.2
BRAM	846.5	2,016	42.0

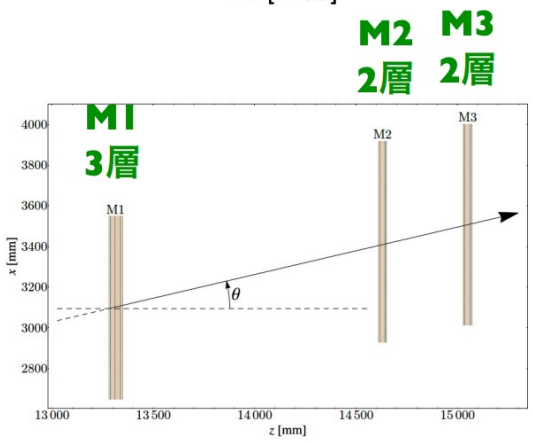
Online tracking using ML

- **ATLAS muon tracking** Prof. Horii (Nagoya Univ.) for ATLAS
  - Implementation of ML-based online tracking
  - Latency < 100ns







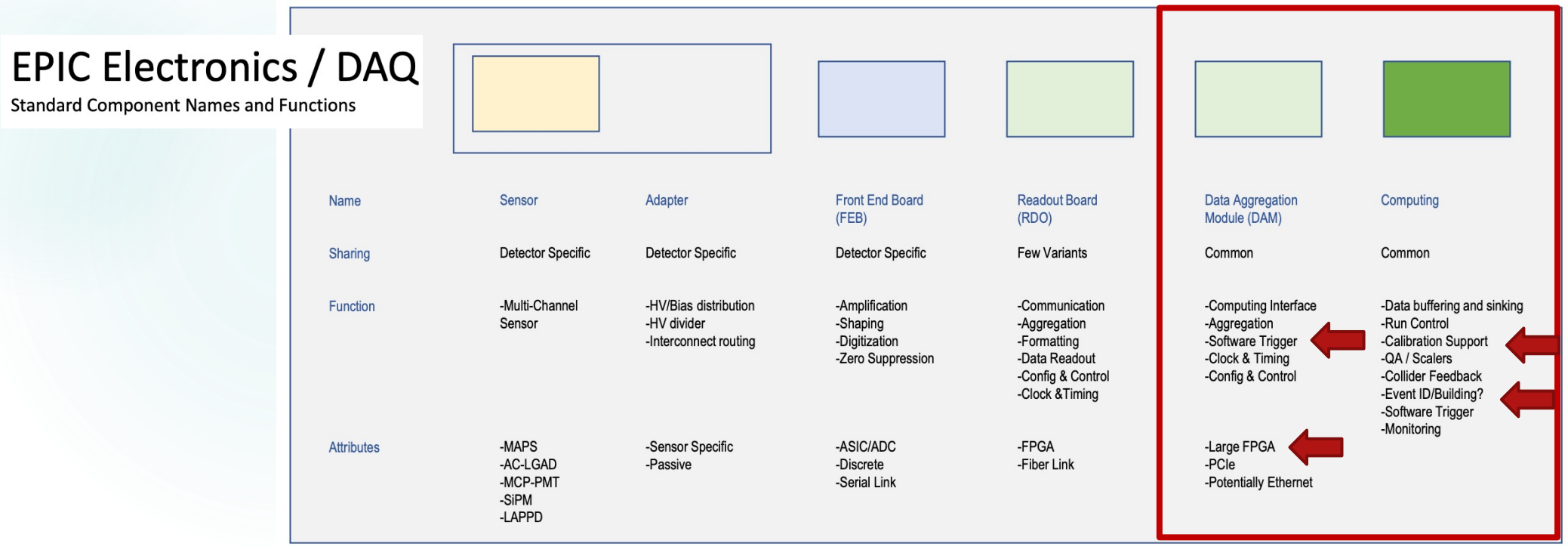


Model	Resolution [mrad]	Latency [ns]	DSP48	LUT	FF	BRAM
BL	1.9	-	-	-	-	-
QF7	2.0	69	1,389 (45%)	34,848 (8.0%)	5,433 (0.6%)	75 (2.8%)
QF5	2.2	69	88 (2.9%)	40,039 (9.3%)	3,419 (0.4%)	75 (2.8%)
QF3	2.8	56	2 (< 0.1%)	21,682 (5.0%)	2,242 (0.3%)	75 (2.8%)

リソース使用率は、Super Logic Regionあたりの値

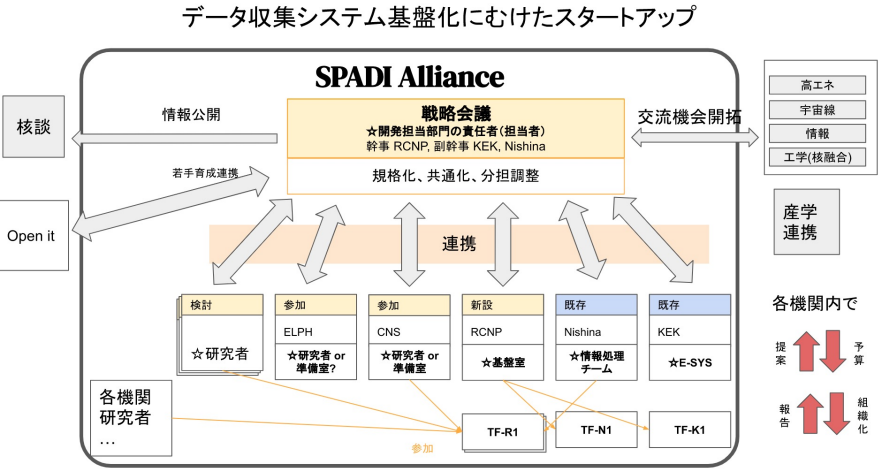
Interest in contributing ePIC-DAQ

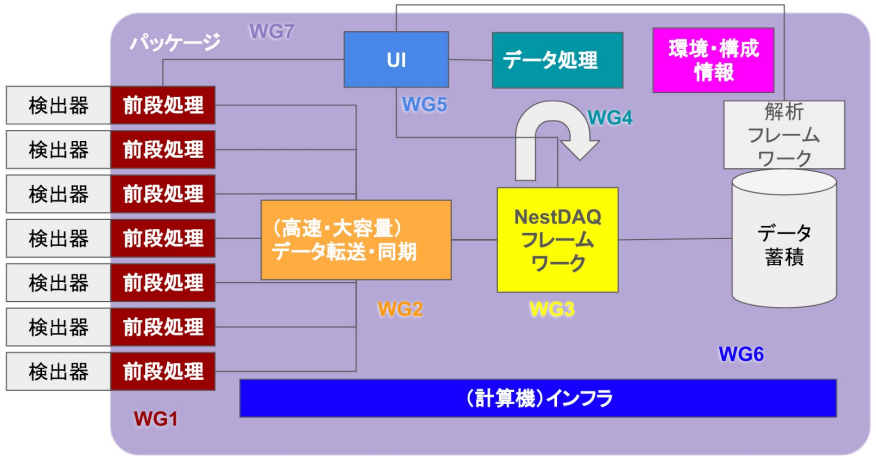
- Plans for ePIC
  - Data processing and software trigger using hardware acceleration (FPGA, GPU, CPU)
  - Vertexing and Tracking at central barrel, PID, jet reconstruction, etc…



SPADI-Alliance

- **"Signal Processing and Data Infrastructure – Alliance (SPADI-Alliance)" in Japan NP community to build and share common infrastructure for Streaming Readout at RIBF, J-PARC, etc…**
  - **ASICs, FECs, streaming software, hardware acceleration**
  - **https://www.rcnp.osaka-u.ac.jp/~spadi/**
  - **~80 members in total**



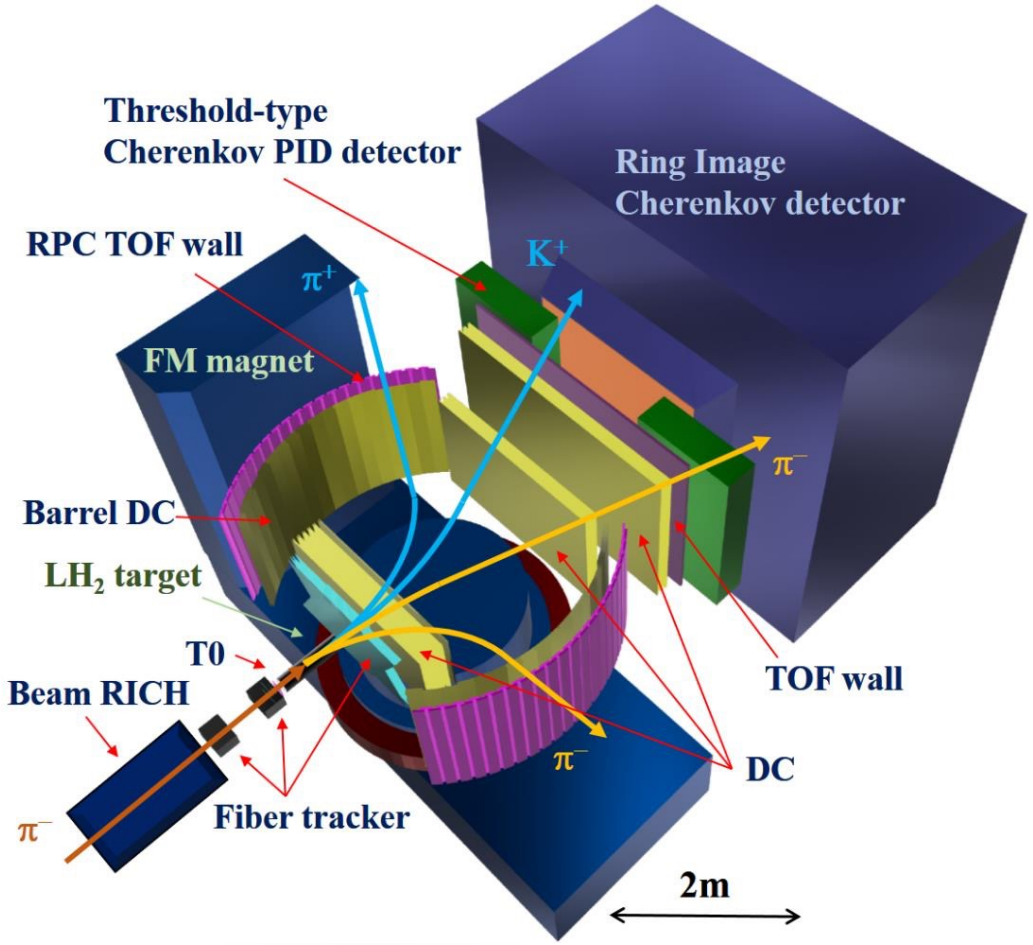


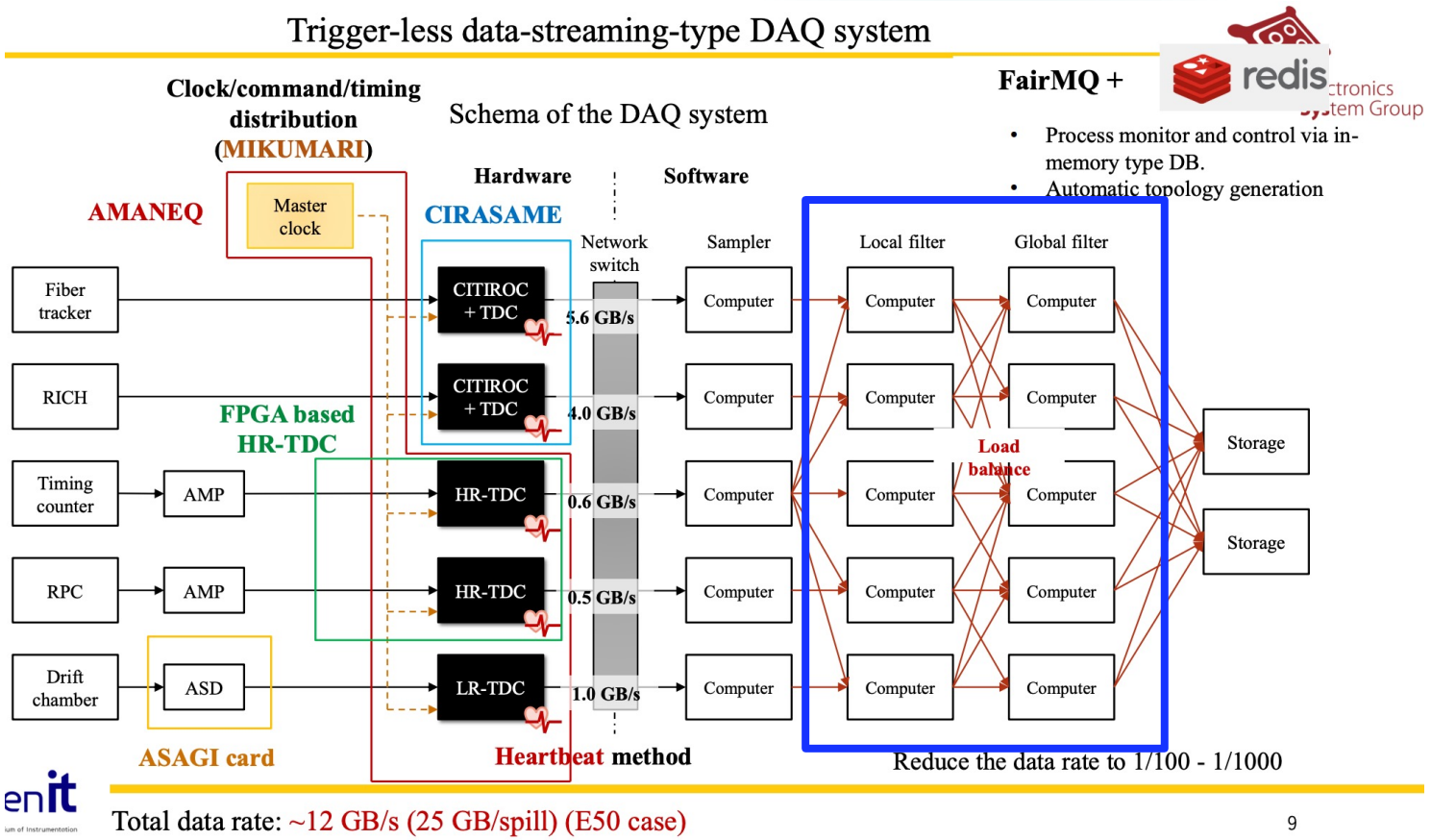
WG1. Analog (ASIC, Front-end)
WG2. Data Transfer, Timing
WG3. NestDAQ framework
WG4. Online processing (T. Gunji)
WG5. User Interface
WG6. Infra-structure
WG7. Packaging

Needs of online processing

J-PARC E50

~10 MHz interaction rate

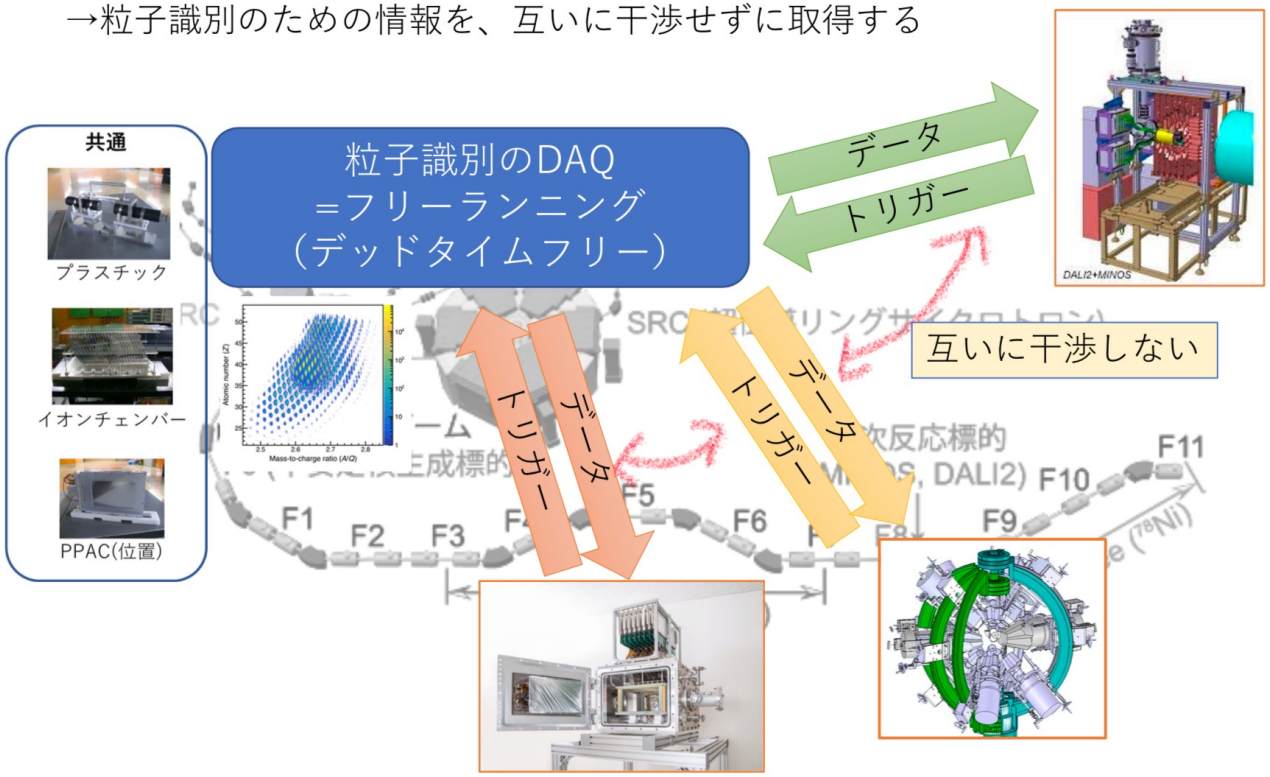


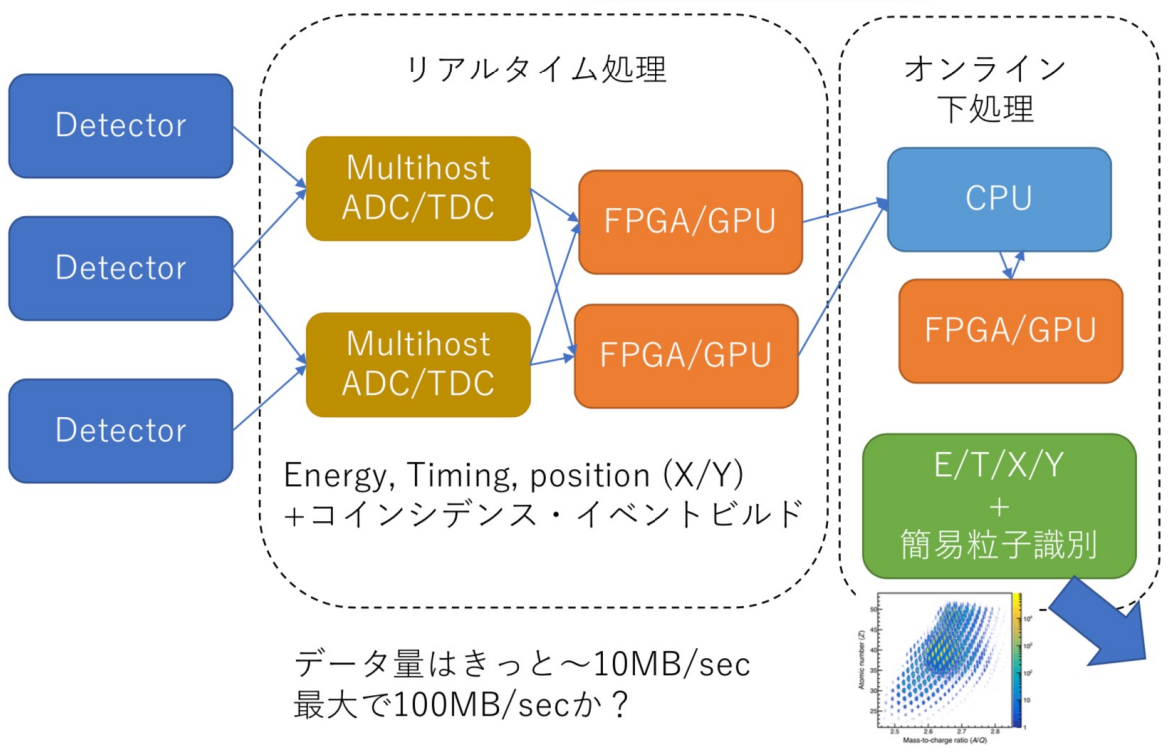


Needs of online processing

RIBF

今までは特定の装置が粒子識別用DAQ(CAMACやVME)を占有
→粒子識別のための情報を、互いに干渉せずに取得する





Interest in contributing DAQ

- Plans for ePIC
  - Data processing and software trigger using hardware acceleration (FPGA, GPU, CPU)
- Possible work items:
  - Run and get familiar with MC simulations
  - Benchmarking of:
    - online reconstruction (tracking, PID, etc)
    - event selections
    - usage of machine learning technique
  - Full system tests to evaluate computing models and estimate computing resources
- Close collaboration within SPADI-A.