

ROC SlowControl FPGA の再実装

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ROC-FPGA

- FPGA (field programmable gate array) : 書き換えを行う開発ツール
FPGAは現場でプログラム可能な論理回路配列という意味
- SlowControl FPGA: SlowControl コマンドをラダーに送受信する
Readbackで使用



Readbackerの現状

- Readbacker

INTTラダー上の読み出しチップ (FPTX) の情報 (レジスタ値) を読み出す

- 現状

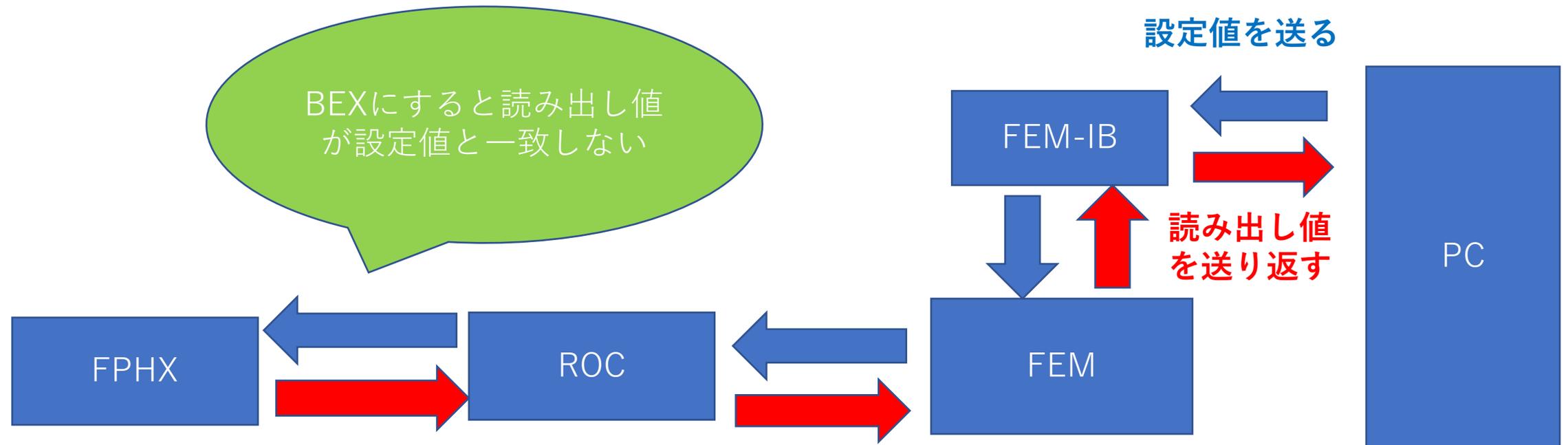
Bus-Extender (BEX) を接続すると、読み出したデータが設定値と異なる

Readbackerの現状

- BEXをつながない時は正常に動作する
設定値をそのまま読み出せる
- BEXをつなぐと、読み出し結果が設定値と異なる
(TO ChipとFrom Chipの値が一致しない)

Reg	Desc	To Chip	From Chip	Rea
*	Wild	0		Rea
1	Mask	0		Rea
2	Dig Ctrl	5	15	Rea
3	Vref	1		Rea
4	DAC0	8	16	Rea
5	DAC1	16	32	Rea
6	DAC2	30	60	Rea
7	DAC3	35	71	Rea
8	DAC4	40	80	Rea
9	DAC5	45	91	Rea
10	DAC6	50	100	Rea
11	DAC7	55	111	Rea
12	N1Sel <3:0>	6		Rea
	N2Sel <7:4>	4		

Readbackerの構成



ROCでデータが1ビットずれて欠けることが分かっている→ROCのFPGAに原因1ビットのずれを補正するようにROC-FPGAを変更するのが目的

セットアップ

- 開発環境

Libero SoC v11.9 (ProAsic3Eで使える)

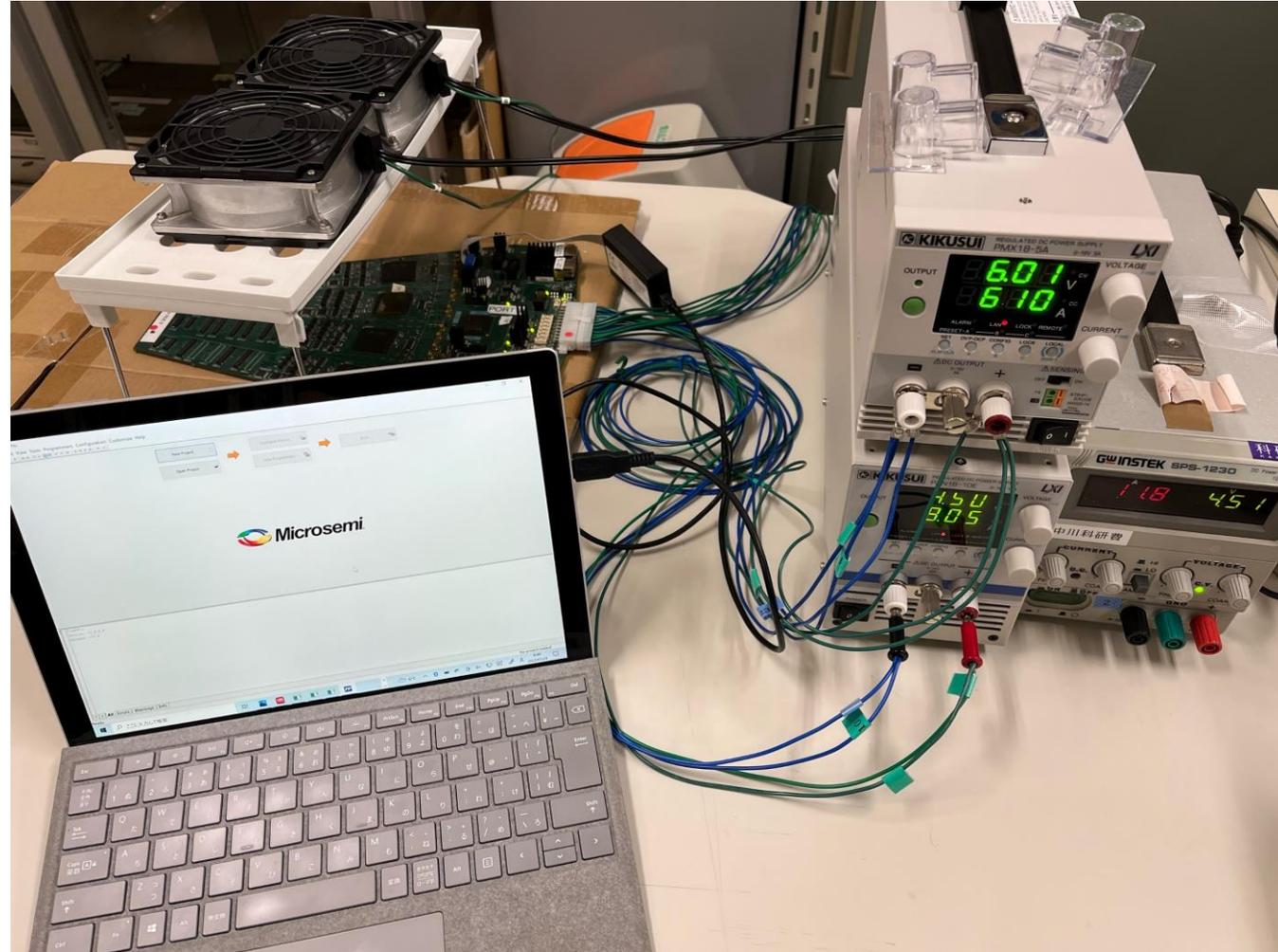
- VHDL言語を用いる 論理合成 + 配線ツール
- V11.9はProAsic3E用の最終版
- FVTX開発にはv9.1が使われている
- Libero SoCのセットアップにはライセンスの入手と設定
ライセンスサーバーの登録が必要

FlashPro (ソフトウェア)

- FPGA書き込み用ソフトウェア
- PCとの接続にFlashPro 5 を用いる

セットアップ

- ROC-FPGA書き換え用のテストベンチ



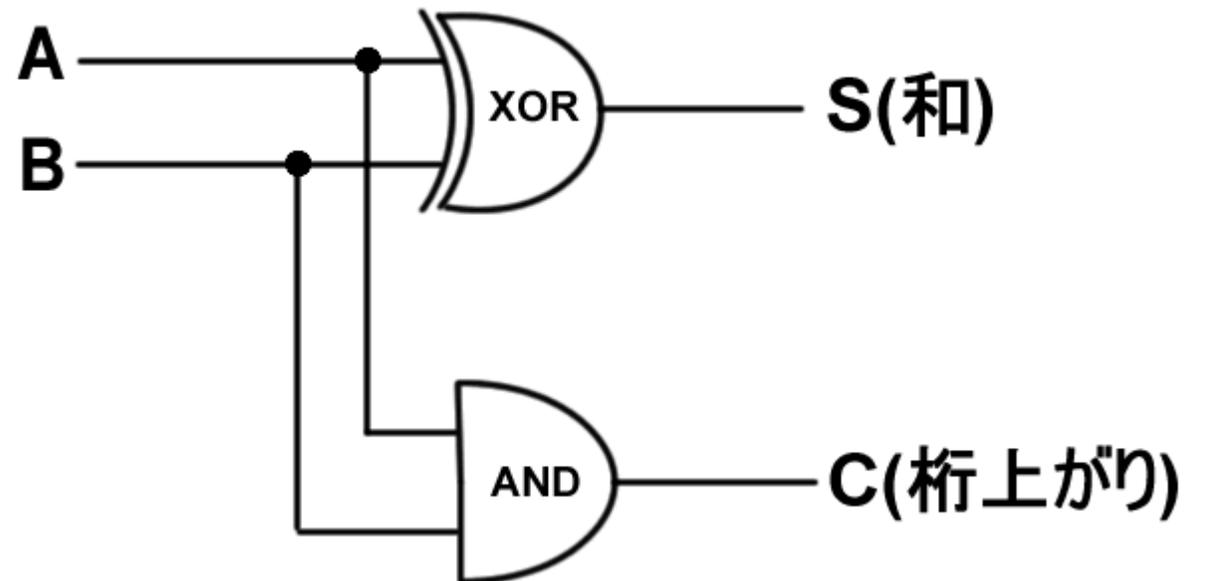
今までしたこと

- 環境の動作テスト
 - Libero SoCとFlashPro動作確認
- FPGAコードの確認とコンパイル
- 書き換え用ベンチの準備

環境の動作テスト (Liberio SoC)

- 回路を作成し、論理合成→シュミレーションを試みた

```
Reports # x | StartPage # x | sample3.vhd # x | sample3_0.vhd # x |
5 -- File history:
6 --   <Revision number>: <Date>: <Comments>
7 --   <Revision number>: <Date>: <Comments>
8 --   <Revision number>: <Date>: <Comments>
9 --
10 -- Description:
11 --
12 -- <Description here>
13 --
14 -- Targeted device: <Family::ProASIC3E> <Die::A3PE1500> <Package::676 FBGA>
15 -- Author: <Name>
16 --
17 -----
18
19 library IEEE;
20
21 use IEEE.std_logic_1164.all;
22 use IEEE.std_logic_arith.all;
23 use IEEE.std_logic_unsigned.all;
24
25 entity sample1 is
26 port (
27     A:in std_logic;
28     B:in std_logic;
29     S:out std_logic;
30     C: out std_logic);
31 end sample1;
32
33 architecture architecture_sample1 of sample1 is
34
35 begin
36     S<=A xor B;
37     C<=A and B;
38     -- architecture body
39 end architecture_sample1;
40
```

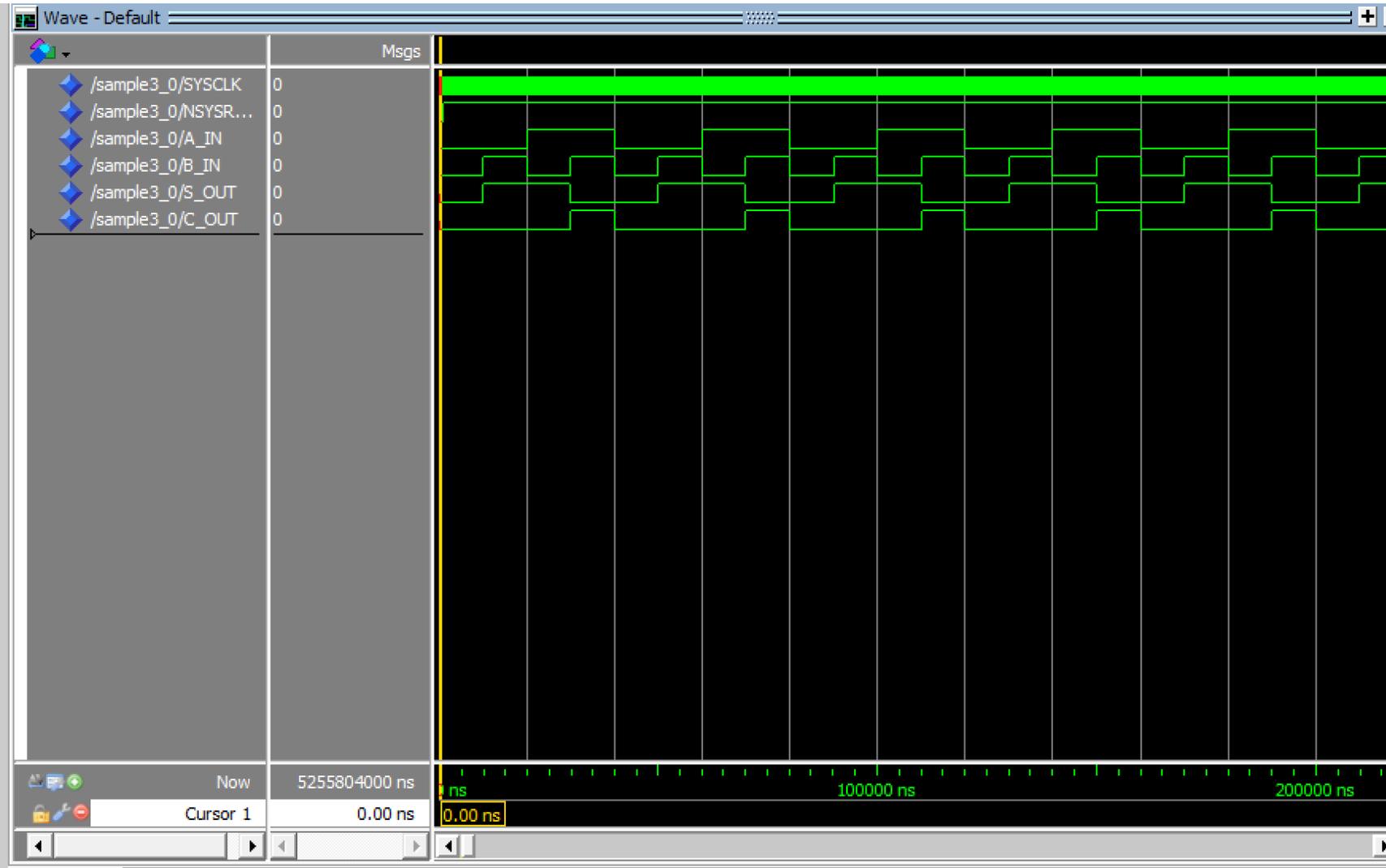


シュミレーション

先ほどの回路でシュミレーションを行うことが出来た

真理値表

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



FlashProによるFPGAのVerify

- FVTXのWebページにあるFPGAコードを使ってROCの SlowControl FPGAをVerify (同じコードかどうかチェック)

FVTX Group

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FVTX FPGA Code

Archived VHDL code for test benches can be found [here](#)

Clock Manager Code for Spartan 3: can be found [here for 9.4 MHz code](#) and [here for 10 MHz Code](#). If you want to look at Spartan 3 board pins consult the [user guide](#) (page 49 -).

LANL ROC, FEM, FEM Interface Card VHDL Codes for 1008:

	ROC		FEM				GUIs		
	Slow Control	Data	JTAG	Slow Control	Data	FEM_IB	nevis_gui.py	fphxtb.py	Comment
						23-Mar-15 Inverted BCO for NE with Trigger			FEM_IB: Added inverted BCO based Mar13 trigger version of FEM_IB cor
				23-Mar-15 FVTX Trigger					SlowControl_FEM: FVTX Trigger Production.
	12-Sep-12, fast, and slow version								ROC Slow Control: PLL changed to 9.4 MHz input BCO rather than 10 MHz changed so that there is a 5.1335 ns delay of READ_CLK w.r.t BCO clock when generated by PLL (default used to be 1.335 ns delay). Also send LATCH and SC_EN for FPGA the SC Fiber (11 and 12) so that it can be monitored to debug SW4, column 1 pin
	5-Sep-12, fast								ROC Slow Control: PLL changed to 9.4 MHz input BCO rather than 10 MHz changed so that there is no delay of READ_CLK w.r.t BCO clock when generated by PLL (default used to be 1.335 ns delay). This seems to allow all channels to be calibrated when collecting calibration data.
		FPGA-A							

Verifyのテスト

- FVTXのWebページのSlowControl FPGAコードを全てVerifyを行ったがエラーが出た
- デザインが異なるというエラーだと考えられる

The screenshot shows the FlashPro software interface. The top menu bar includes File, Edit, View, Tools, Programmers, Configuration, Customize, and Help. The main workspace contains a workflow diagram with buttons for 'New Project', 'Open Project', 'Configure Device', 'View Programmers', and 'VERIFY'. Below this is a table of detected programmers.

Programmer				
	Program	Port	Programmer	Program
1	S2001L82UX	FlashPro5	usbS2001	RUN FAILED

Below the table is a 'Refresh/Rescan for Programmers' button. At the bottom, the console window displays the following error message:

```
programmer 'S2001L82UX' : Verify 0 failed at row 5636.  
programmer 'S2001L82UX' : EXPORT_ERROR_CODE[16] = 805a  
programmer 'S2001L82UX' : Finished: Thu Jan 19 18:35:12 2023 (Elapsed time 00:00:00)  
● Error: programmer 'S2001L82UX' : Executing action VERIFY FAILED, EXIT 11, refer to FlashPro online help for details.
```

The status bar at the bottom shows the file path: C:\roc_fpga\ROC_slow_control_fast_21May12\ROC_slow_control\designer\impl1\ROC_slow_control_top_fp\projectData\ROC_slow_control_top.stp SINGLE

Verifyのテスト

一部のコードではそもそもVerifyが出来なかった (RUNならできる)



```
Error: Failed to run ACTION.  
Project closed.  
Software Version: 11.9.0.4  
programmer 'S2001L82UX' : FlashPro5  
Warning: The programmer with id '08756' in the project file cannot be detected and connected.  
Opened 'C:\¥roc_fpga¥ROC_slow_control_fast¥ROC_slow_control¥designer¥impl1¥ROC_slow_control_top_1_fp¥ROC_slow_control_top.pro'  
Error: A programming file must be loaded before running the command 'run_selected_actions'.
```

< >

All Errors Warnings Info

SlowControl FPGAのコンパイル

- FVTXのWebページにある一番新しいFPGAコードを使ってLibero SoCでコンパイルを行った。何も変えずに行うとエラーがでる

The screenshot displays the Libero SoC IDE interface. The left pane shows the Design Flow tree with the 'Compile' step selected. The right pane shows the 'Reports' window for 'ROC_slow_control_top.pdc', displaying a summary of 2 errors and 52 warnings. The bottom pane shows the 'Message' window with a list of error and warning messages.

Reports Summary:

- Optimized macros:
 - Dangling net drivers: 0
 - Buffers: 1
 - Inverters: 0
 - Tieoffs: 0
 - Logic combining: 10
- Total macros optimized: 11

Warnings:

- Warning: CMP503: Remapped 8 enable flip-flop(s) to a 2-tile implementation because the CLR/PRE pin on the enable flip-flop is not being driven by a global net.
- Info: BLK016: Delete the global instance Inst_input_block/RST_CLKINT because of clock sharing. The driver net will be rerouted.
- Info: BLK016: Delete the global instance Inst_data_streamer/RST_CLKINI because of clock sharing. The driver net will be rerouted.
- Info: BLK016: Delete the global instance Inst_sc/Inst_calibrator/RST_CLKINT because of clock sharing. The driver net will be rerouted.
- Info: BLK016: Delete the global instance Inst_input_block/HARD_RST_CLKINT because of clock sharing. The driver net will be rerouted.

Errors:

- Error: PDC-71: Clock net name 'BCO_CLK' is not valid

Message Window:

- Please refer to the log file for details about 14 Warning(s)
- Removing instance U_AND2_3_4 because it does not drive other instances. To preserve this instance, use the syn_noprune synthesis directive.
- Signal SER_AMPL_EN_OUT is floating: a simulation mismatch is possible.
- create_generated_clock with both -multiply_by and -divide_by not supported for this target technology
- Found inferred clock pll_main/GLA_inferred_clock which controls 201 sequential elements including Inst_sc/Inst_command_decoder/DATA_FPHX_OUT. This clock has no specified timing constraint which may adversely impact design performance.
- Found issues with constraints. Please check constraint checker report "C:\FVTX_VHDL_code\ROC_slow_control\yghnthesis\ROC_slow_control_top_cck.rpt".
- Found inferred clock pll_main/GLA_inferred_clock with period 3.33ns. Please declare a user-defined clock on object "n:Inst_DCM_MAIN.GLA"
- Source for clock Inst_DCM_MAIN/Core:GLA not found in netlist. Run the constraint checker to verify if constraints are applied correctly.

コンパイルのエラー

エラーの内容を確認すると上から3行目が#がなくコメントになっていなかったなので訂正

```
All 2 Errors 52 Warnings 8 Info
Optimized macros:
- Dangling net drivers: 0
- Buffers: 1
- Inverters: 0
- Tieoff: 0
- Logic combining: 10
Total macros optimized 11
Warning: CMP503: Remapped 8 enable flip-flop(s) to a 2-tile implementation because the CLR/PRE pin on the enable flip-flop is not being driven by a global net.
Info: BLK016: Delete the global instance Inst_input_block/RST_CLKINT because of clock sharing. The driver net will be rerouted.
Info: BLK016: Delete the global instance Inst_data_streamer/RST_CLKINT because of clock sharing. The driver net will be rerouted.
Info: BLK016: Delete the global instance Inst_sc/Inst_calibrator/RST_CLKINT because of clock sharing. The driver net will be rerouted.
Info: BLK016: Delete the global instance Inst_input_block/HARD_RST_CLKINT because of clock sharing. The driver net will be rerouted.
There were 0 error(s) and 51 warning(s) in this design.
=====
Reading user pdc (Physical Design Constraints) file(s) postcompile
Error: PDC-71: Clock net name 'BCO_CLK' is not valid
There were 1 error(s) and 0 warning(s) in reading the user pdc.
The Compile command failed ( 00:00:01 )
Error: Failure when executing Tcl script. [ Line 30 ]
The Execute Script command failed ( 00:00:08 )
Warning: The database was closed without a save, modifications are lost
Design closed.
```

```
Reports ROC_slow_control_top.vhd StartPage ROC_slow_control_top.sdc ROC_slow_control_top.pdc
1 #assign_global_clock -net HARD_RST
2 #assign_global_clock -net GLOBAL_RST
3 #assign_global_clock -net BCO_CLK
4 #assign_global_clock -net CLK_TX_SC
5 #assign_global_clock -net CLK_RX_SC
6
7 #set_io TEST_OUT\[0\] -pinname A11 -fixed yes
8 #set_io TEST_OUT\[1\] -pinname A10 -fixed yes
9 #set_io TEST_OUT\[2\] -pinname B13 -fixed yes
10
11 set_io BCO_CLK_0_n -pinname P23 -fixed yes
12 set_io BCO_CLK_0_p -pinname N22 -fixed yes
13 set_io BCO_CLK_OUT_0_n -pinname N26 -fixed yes
14 set_io BCO_CLK_OUT_0_p -pinname M26 -fixed yes
15 set_io CALIB_IO_0\[0\] -pinname C11 -fixed yes
16 #set_io CALIB_IO_0\[1\] -pinname F13 -fixed yes
17 set_io CALIB_IO_0\[2\] -pinname B11 -fixed yes
18 set_io CALIB_IO_0\[3\] -pinname G13 -fixed yes
19 set_io CALIB_IO_1\[0\] -pinname A11 -fixed yes
20 #set_io CALIB_IO_1\[0\] -pinname A15 -fixed yes
21 set_io CALIB_IO_1\[1\] -pinname C13 -fixed yes
22 set_io CALIB_IO_1\[2\] -pinname A10 -fixed yes
23 #set_io CALIB_IO_1\[2\] -pinname A14 -fixed yes
24 set_io CALIB_IO_1\[3\] -pinname B13 -fixed yes
25 #set_io CALIB_IO_1\[3\] -pinname B15 -fixed yes
26 set_io CALIB_IO_2\[0\] -pinname C12 -fixed yes
27 set_io CALIB_IO_2\[1\] -pinname E13 -fixed yes
28 set_io CALIB_IO_2\[2\] -pinname B12 -fixed yes
29 set_io CALIB_IO_2\[3\] -pinname D13 -fixed yes
30 set_io CALIB_IO_3\[0\] -pinname A13 -fixed yes
31 set_io CALIB_IO_3\[1\] -pinname G14 -fixed yes
32 set_io CALIB_IO_3\[2\] -pinname A12 -fixed yes
33 set_io CALIB_IO_3\[3\] -pinname F14 -fixed yes
34 set_io CLK_RX_SC -pinname R6 -fixed yes
```

SlowControl FPGAコードのコンパイル

- 結果コンパイルに成功→このファイルをFPGA書き換えテストに利用

Libero - C:\roc_fpga\ROC_slow_control\ROC_slow_control\ROC_slow_control.prj

Project File Edit View Design Tools Help

Design Flow

ROC_slow_control_top

Tool

- Import Timing Constraints
- Implement Design
- Synthesize
- Constrain
- Verify Post-Synthesis Implementation
- Simulate
- Compile
- Constrain Place and Route
- Place and Route
- Verify Post Layout Implementation
- Simulate
- Verify Timing
- Verify Power
- Export Back Annotated Files
- Generate Programming Data
- Program Design
- Program Device

Reports

```
1 #assign_global_clock -net HARD_RST
2 #assign_global_clock -net GLOBAL_RST
3 #assign_global_clock -net BCO_CLK
4 #assign_global_clock -net CLK_TX_SC
5 #assign_global_clock -net CLK_RX_SC
6
7 #set_io TEST_OUT\{0\} -pinname A11 -fixed yes
8 #set_io TEST_OUT\{1\} -pinname A10 -fixed yes
9 #set_io TEST_OUT\{2\} -pinname B13 -fixed yes
10
11 set_io BCO_CLK_0_n -pinname P23 -fixed yes
12 set_io BCO_CLK_0_p -pinname N22 -fixed yes
13 set_io BCO_CLK_OUT_0_n -pinname N26 -fixed yes
14 set_io BCO_CLK_OUT_0_p -pinname M26 -fixed yes
15 set_io CALIB_IO_0\{0\} -pinname C11 -fixed yes
16 set_io CALIB_IO_0\{1\} -pinname F13 -fixed yes
17 set_io CALIB_IO_0\{2\} -pinname B11 -fixed yes
18 set_io CALIB_IO_0\{3\} -pinname G13 -fixed yes
19 set_io CALIB_IO_1\{0\} -pinname A11 -fixed yes
20 #set_io CALIB_IO_1\{0\} -pinname A15 -fixed yes
21 set_io CALIB_IO_1\{1\} -pinname C13 -fixed yes
22 set_io CALIB_IO_1\{2\} -pinname A10 -fixed yes
23 #set_io CALIB_IO_1\{2\} -pinname A14 -fixed yes
24 set_io CALIB_IO_1\{3\} -pinname B13 -fixed yes
25 #set_io CALIB_IO_1\{3\} -pinname B15 -fixed yes
26 set_io CALIB_IO_2\{0\} -pinname C12 -fixed yes
27 set_io CALIB_IO_2\{1\} -pinname E13 -fixed yes
28 set_io CALIB_IO_2\{2\} -pinname B12 -fixed yes
29 set_io CALIB_IO_2\{3\} -pinname D13 -fixed yes
30 set_io CALIB_IO_3\{0\} -pinname A13 -fixed yes
```

Message

Messages Errors Warnings Info Manage suppressed messages

Message

- Found issues with constraints. Please check constraint checker report "C:\roc_fpga\ROC_slow_control\ROC_slow_control\synthesis\ROC_slow_control_top_cck.rpt".
- Found inferred clock pll_main\GLA_inferred_clock with period 3.33ns. Please declare a user-defined clock on object "n:Inst_DCM_MAIN.GLA"
- Source for clock Inst_DCM_MAIN/Core:GLA not found in netlist. Run the constraint checker to verify if constraints are applied correctly.

Compile [ROC_slow_control_top]

- Please refer to the log file for details about 51 Warning(s) , 8 Info(s)

Place and Route [ROC_slow_control_top]

- Please refer to the log file for details about 3 Info(s)

Generate Bitstream [ROC_slow_control_top]

- Please refer to the log file for details about 1 Info(s)

Validation

Log Message

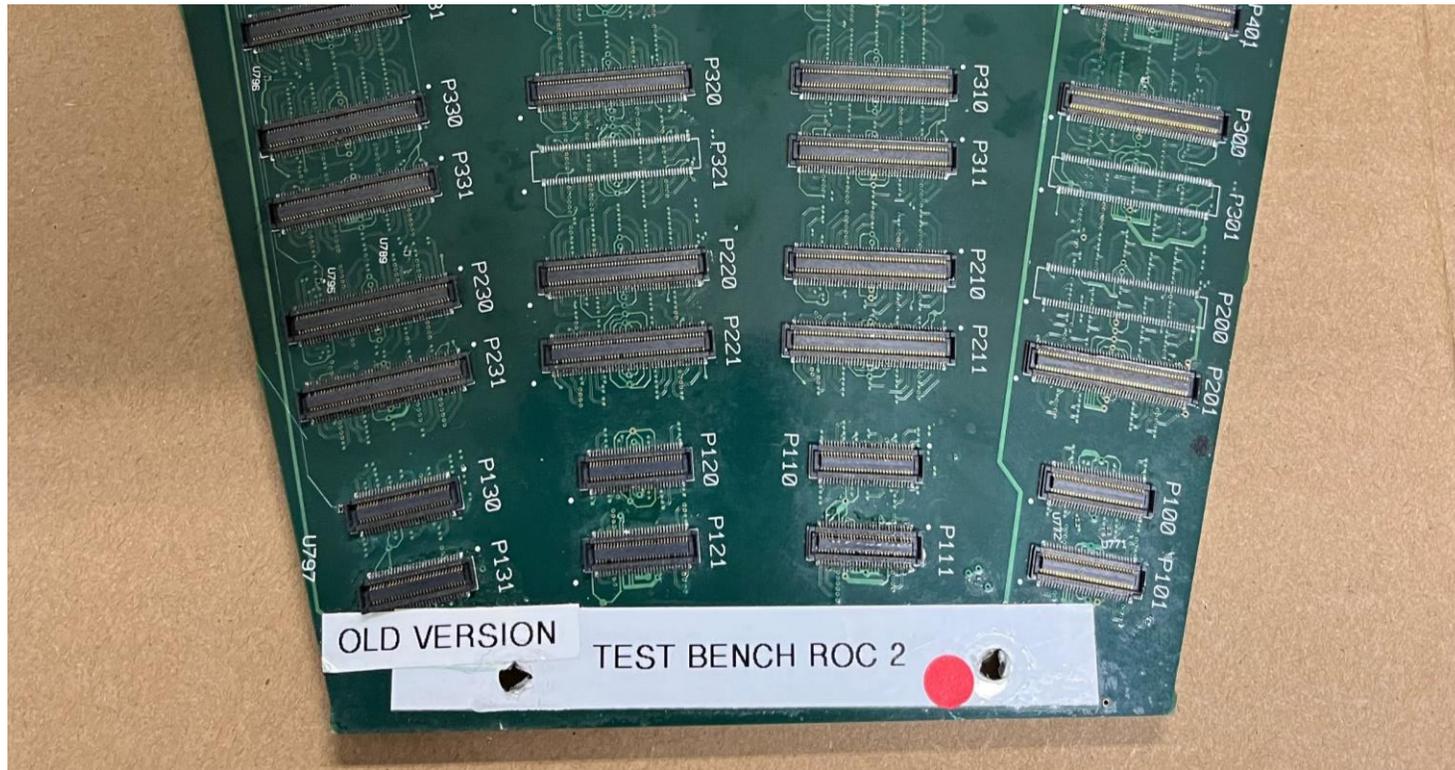
Fam: ProASIC3E Part: A3PE1500-2FG676 VHDL

ここに入力して検索

10°C 16:05 2023/01/20

FPGAコード書き換えテスト

- Verifyのテストを行っているときはROC7を使用していたが実際にProgramするために古いROCを使用した



FPGAの書き換えテスト

- 先ほどのコンパイルに成功したFPGAコードを使ってProgramを行うと成功し、次にそのコードでのVerifyも成功→FPGAの書き換えが成功

The screenshot displays the software interface for FPGA programming. At the top, a sequence of buttons is shown: 'New Project', 'Open Project', 'Configure Device', 'View Programmers', and 'VERIFY'. Arrows indicate the flow from 'New Project' to 'Configure Device', and from 'View Programmers' to 'VERIFY'. The 'View Programmers' button is highlighted with a blue border.

Below the buttons, a table titled 'Programmer' shows the status of the programming process:

Programmer	Program	Port	Programmer	Program
1 S2001L82UX	FlashPro5	usbS2001	RUN PASSE	☐

At the bottom, a 'Refresh/Rescan for Programmers' button is visible.

The bottom section of the screenshot shows the command-line output of the programming process:

```
programmer 'S2001L82UX': Verifying FPGA Array
programmer 'S2001L82UX': Verifying FPGA Array -- pass
programmer 'S2001L82UX': Finished: Fri Jan 20 15:57:15 2023 (Elapsed time 00:01:15)
programmer 'S2001L82UX': Executing action PROGRAM PASSED.

o - o - o - o - o - o

programmer 'S2001L82UX': Scan Chain...
programmer 'S2001L82UX': Vpump will not be driven from the programmer, an external voltage source has been detected that will provide Vpump.
programmer 'S2001L82UX': Scan Chain PASSED.
programmer 'S2001L82UX': Executing action VERIFY
programmer 'S2001L82UX': EXPORT FSN[48] = 910369243c50
programmer 'S2001L82UX': Verifying FPGA Array
programmer 'S2001L82UX': Verifying FPGA Array -- pass
programmer 'S2001L82UX': Finished: Fri Jan 20 15:58:04 2023 (Elapsed time 00:00:29)
programmer 'S2001L82UX': Executing action VERIFY PASSED.

o - o - o - o - o - o
```

まとめと今後すること

- FPGAを書き換えることができるようになった
- 実際にFPGAコードを変更したものをFPGAにProgramをして変更した通りに動作するかテスト

