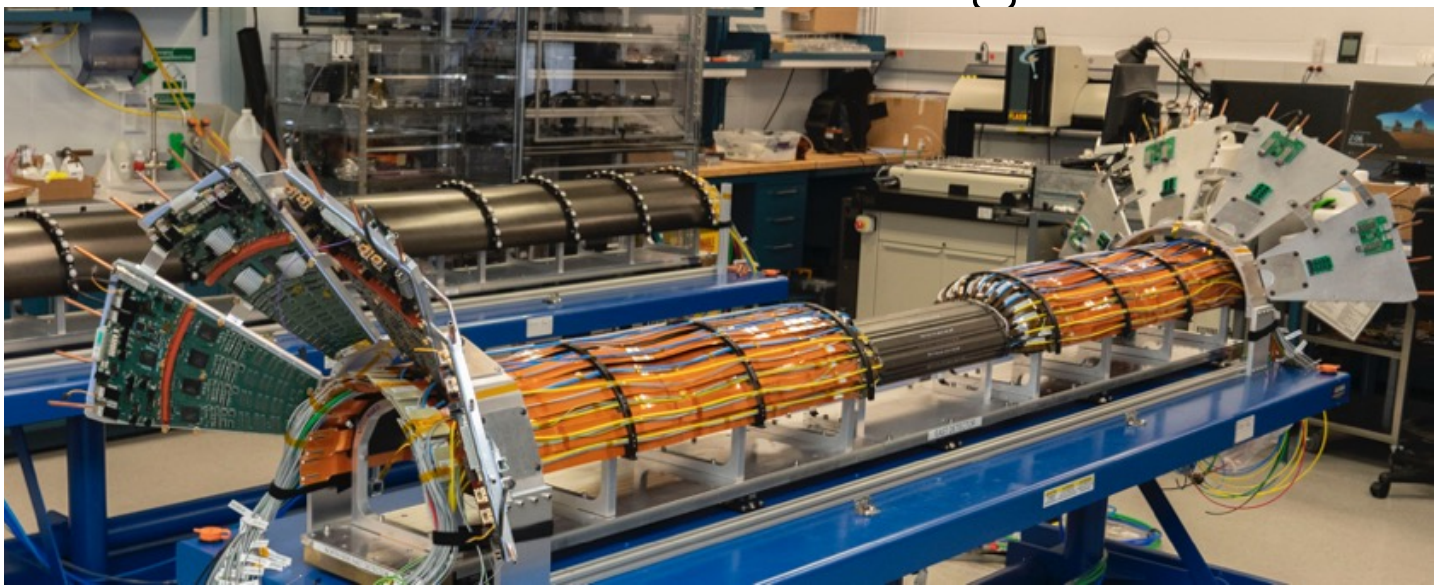
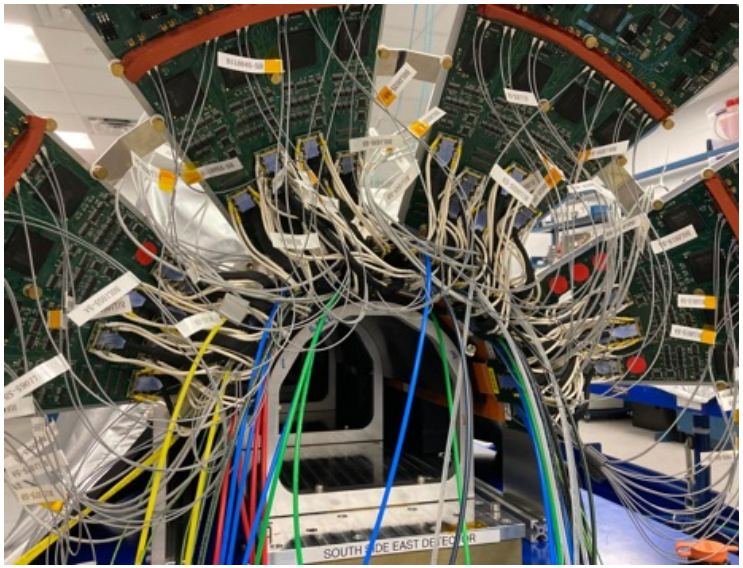
INTT Commissioning Plan

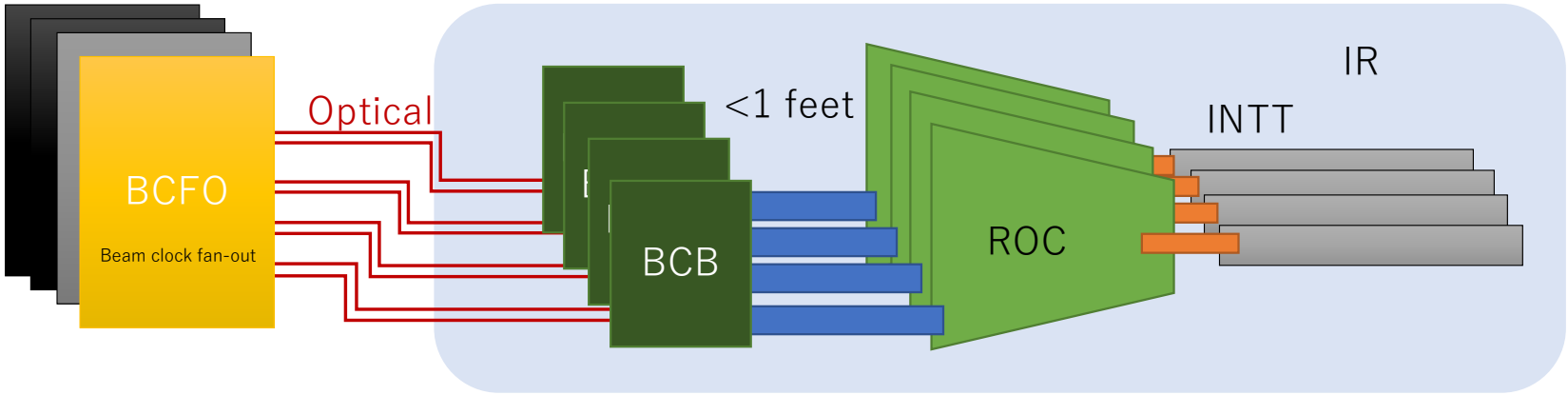
RIKEN/RBRC

Itaru Nakagawa

INTT Barrel Cabling





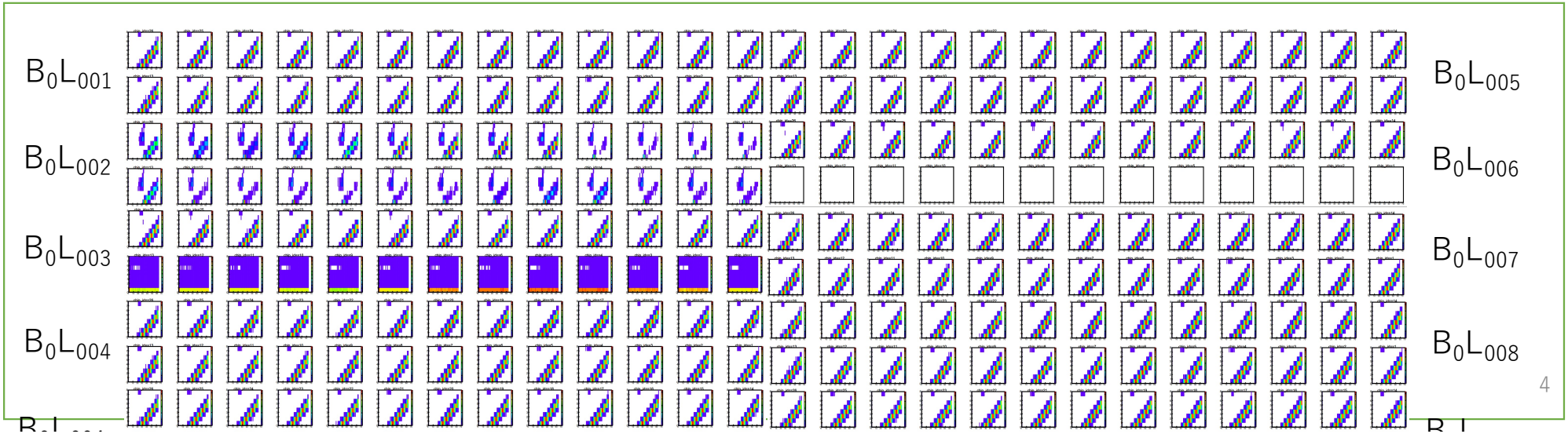


Commissioning without beam

1. Apply 100V bias (HV GUI). Diagnose any over current channels.
2. Power on a ladder by ladder (LV GUIs) and apply 100V bias. Run the calibration. Make sure the results appears in the expected ladder map in the Calibration Monitor.
3. Diagnose missing channels and try to recover.
4. Random trigger noise run (random external trigger). Debug any large noise half ladder or channels.
5. Tune the alert range of LV/HV voltage/current control panels (alert features of LV/HV GUI).
6. Save dead/hot channels in the database. (Expert GUI)

Calibration Monitor

- Should have a calibration results at a glance. At least the results of ½ barrel appears in a single page. Is it possible?
- Perhaps a calibration mode can be implemented to the OnlineMonitor, but #of hits/strip is not sufficient. We definitely need ADC vs. Amplitude 2D plots.

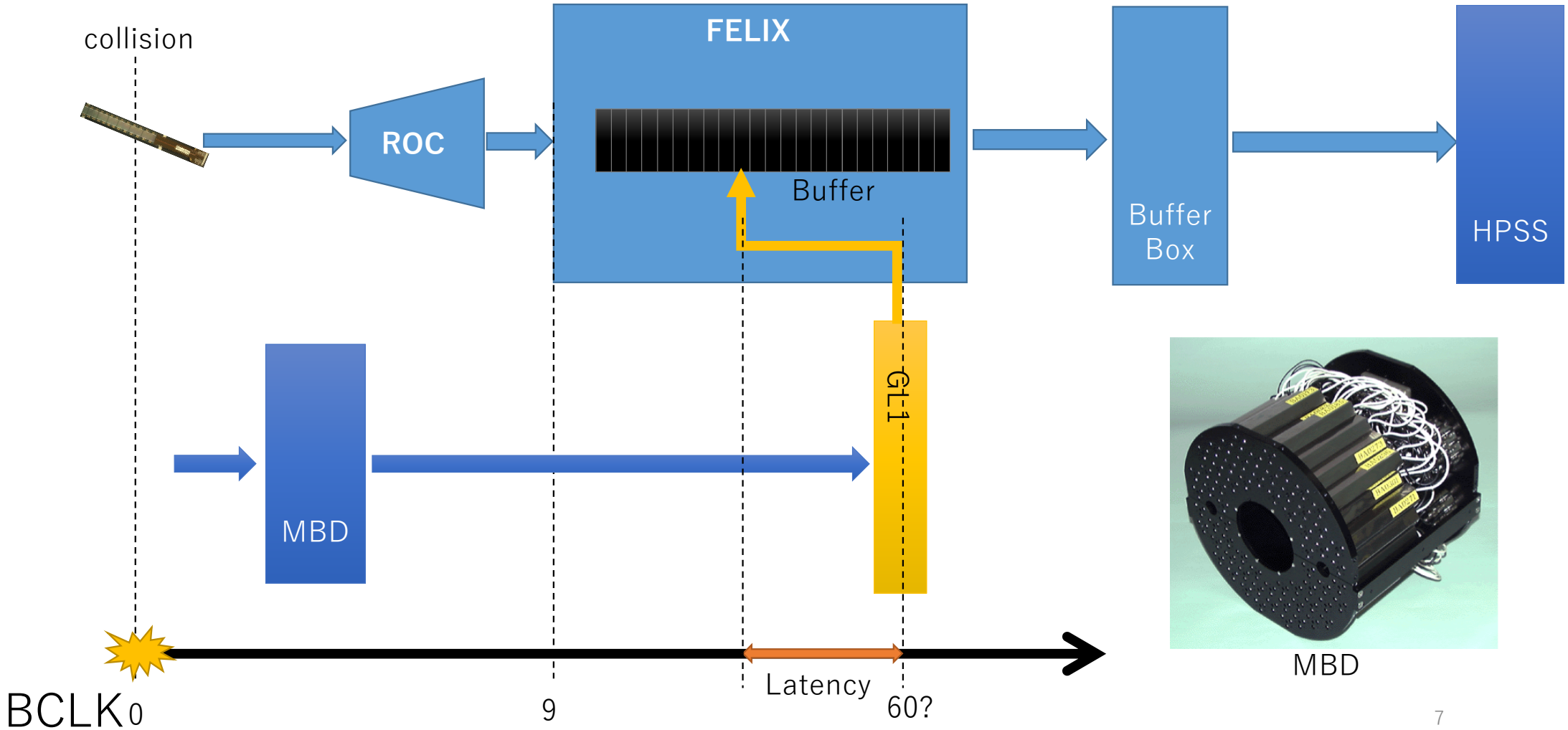


Commissioning with beam

1. BCO Timing Scan (INTT Hit Yield/Event).
2. BCO Phase Scan fine tweak the timing with respect to BCO.
3. Mis-cabling check by the geometry (Event Display)
4. Diagnose missing channels and try to recover
5. Check yield uniformity (Online Monitor)
6. Gain matching between ladders or fine tweak noise
7. DAC Scan at HV=100V (DAC Scan Analyzer)
8. Bias Voltage Scan (MIP/MPV Fitter)
9. DAC0 threshold optimization. S/N evaluation chip by chip.

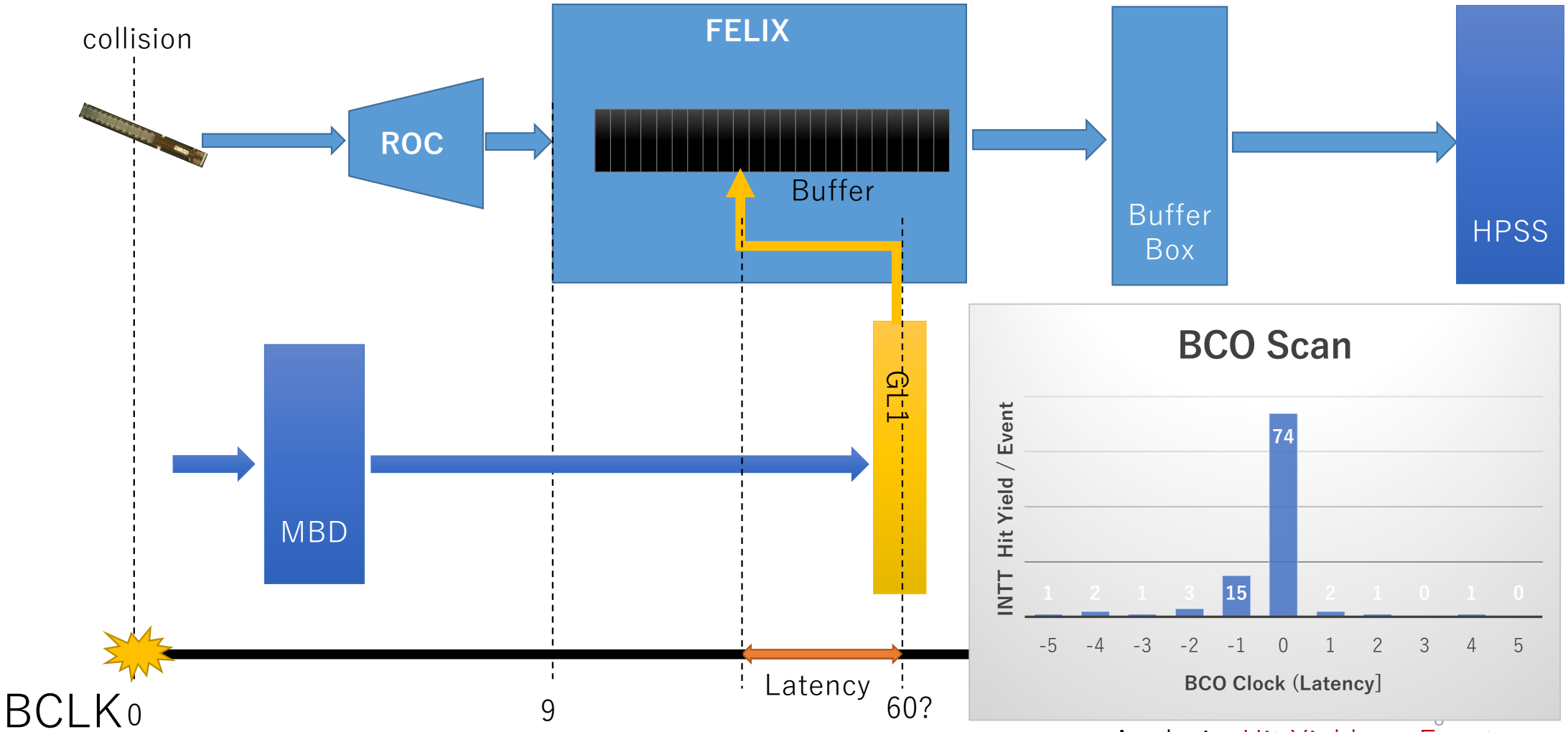
Timing Tune

Timing Tune



MBD

1. BCO Scan



Analysis: Hit Yield per Event

2. BCO Phase Scan

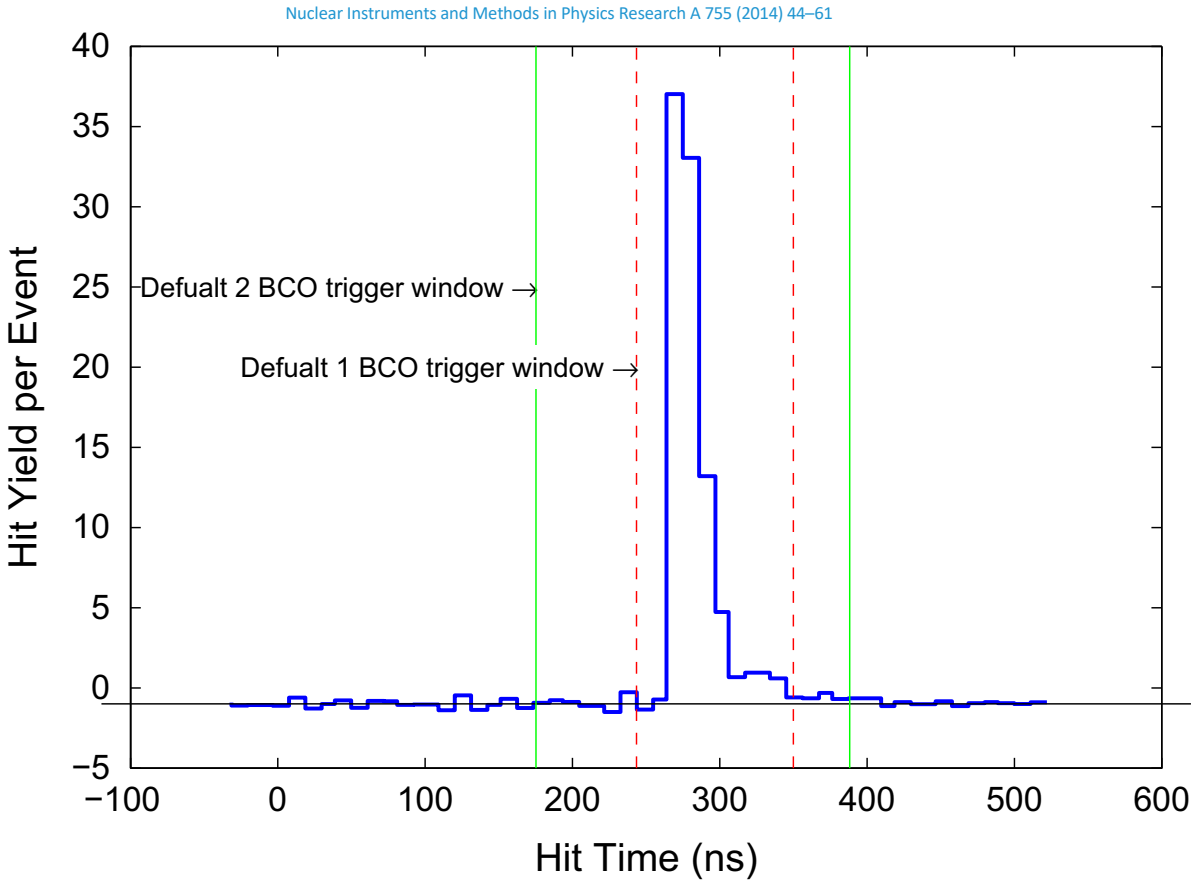


Fig. 32. Timing distribution of the FVTX hits relative to the RHIC beam clock.

6.1. Timing

The distribution in time of FVTX hits is studied relative to the RHIC collision time by comparing the hit rate at different FVTX delay values relative to the RHIC beam clock. The timing distribution for two sectors of wedges in the south arm is shown in Fig. 32. Most hits fall in a window ∼30 ns wide.

Two standard trigger timing configurations were used during FVTX operation, as shown by the vertical lines in Fig. 32: during relatively low trigger rate running (in heavy ion systems) hits arriving in a time window two RHIC beam clocks (BCO) wide (1 BCO∼106 ns) are accepted. In high trigger rate p+p running, a 1 BCO-wide window is used to avoid recording accidental hits from neighboring beam crossings (1 BCO apart).

On 2023/01/12 22:22, Huang, Jin wrote:

That was exactly how it was done and highly recommended for intt too. It took few hours of a special low bunch fill to perform this scan, shifting BCO phase 19-20ns at a time. That appears the only way to set timing for the sub-bco delay
Jin

2. BCO Phase Scan

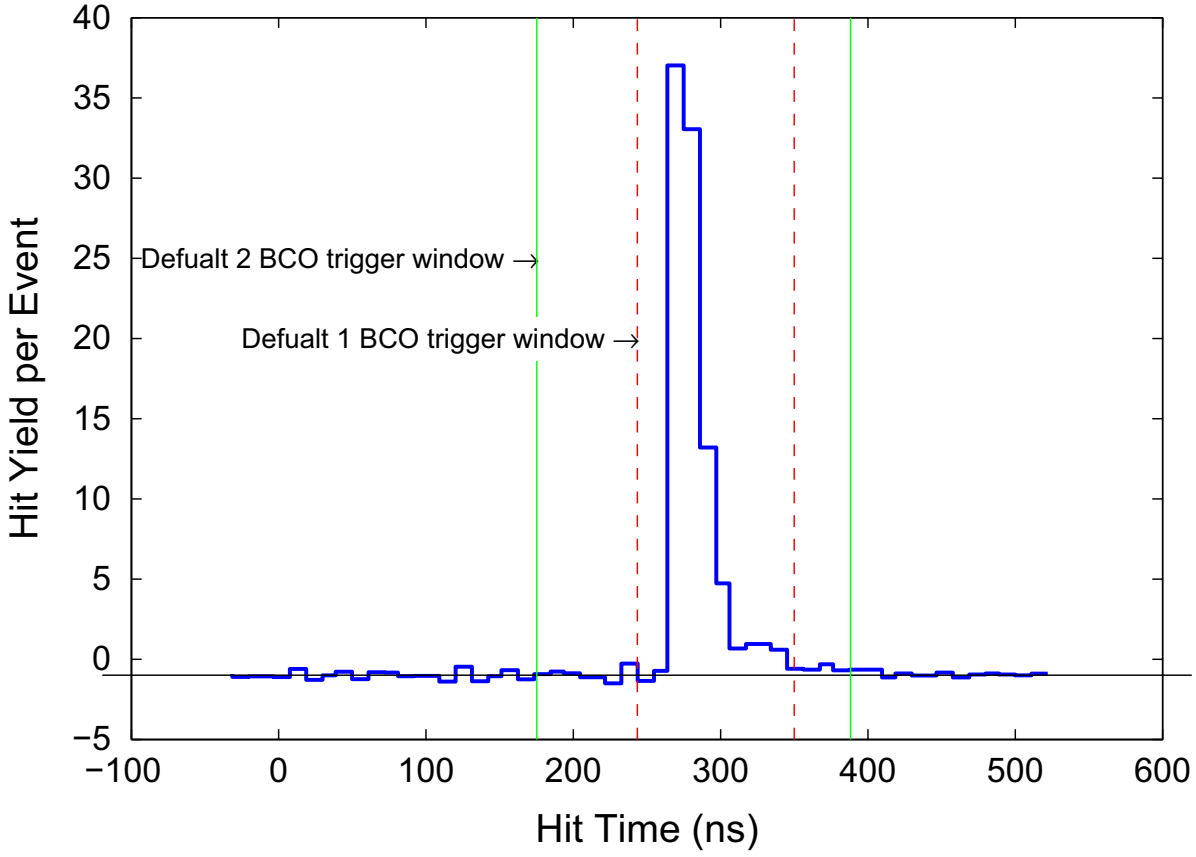
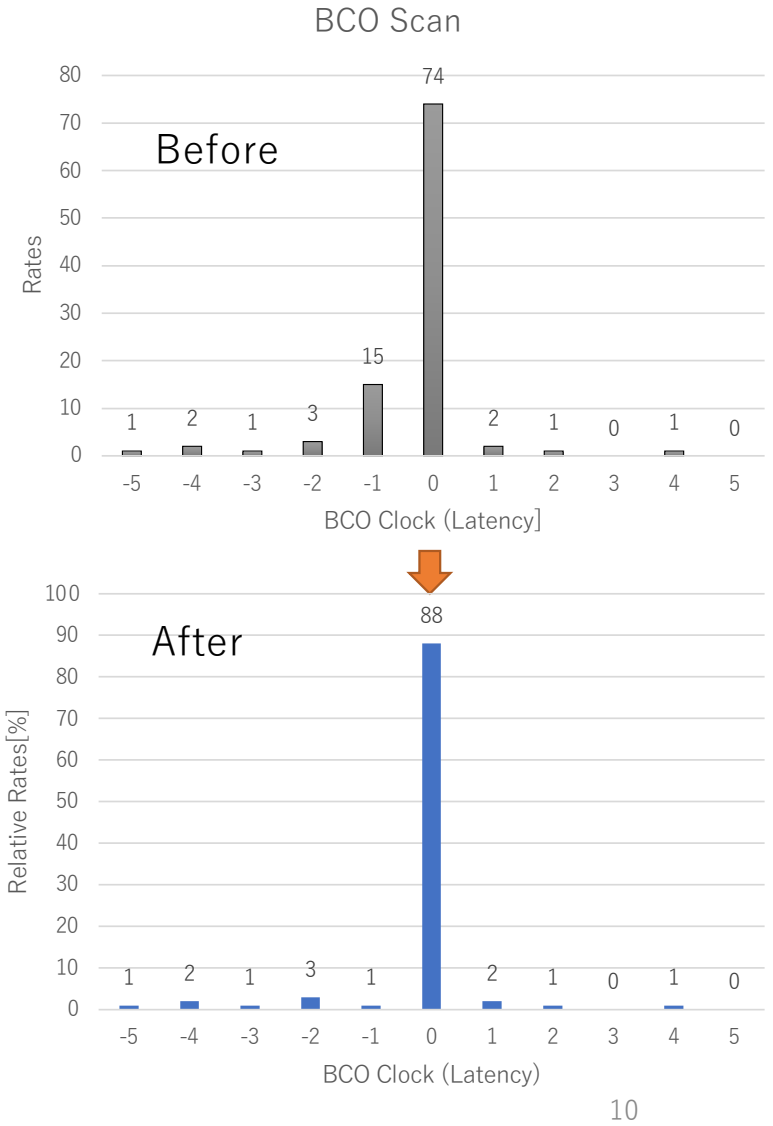
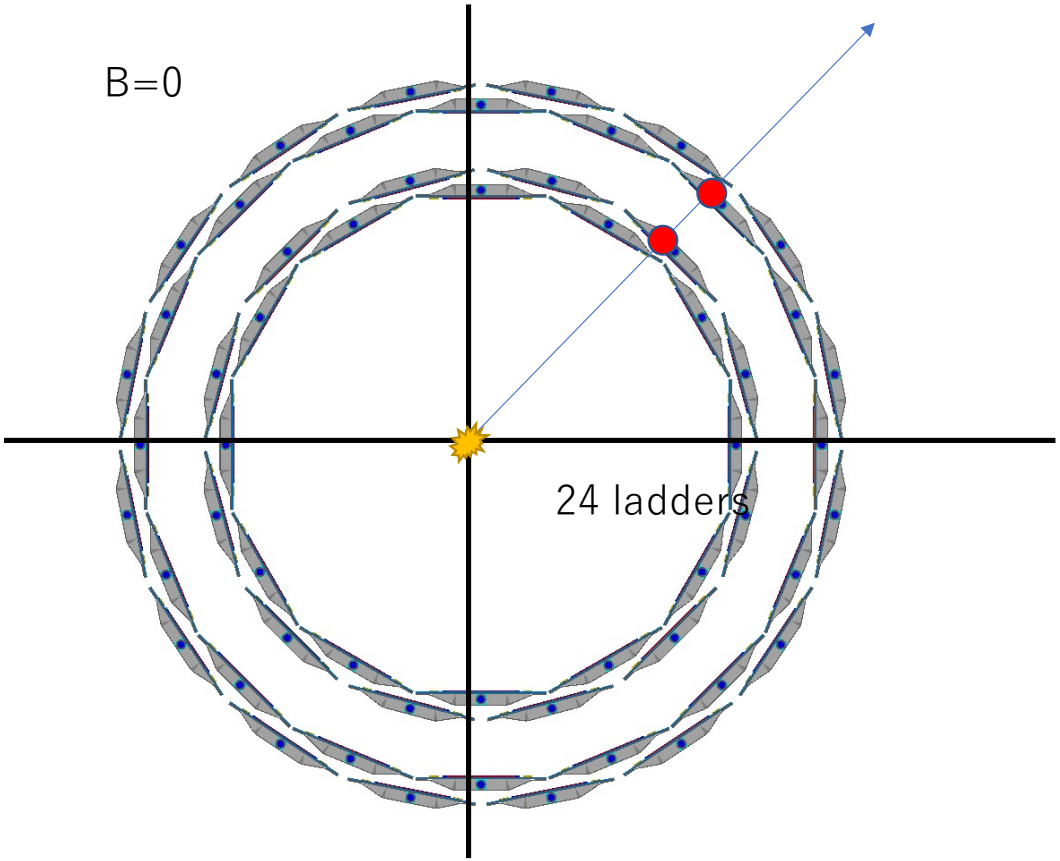


Fig. 32. Timing distribution of the FVTX hits relative to the RHIC beam clock.

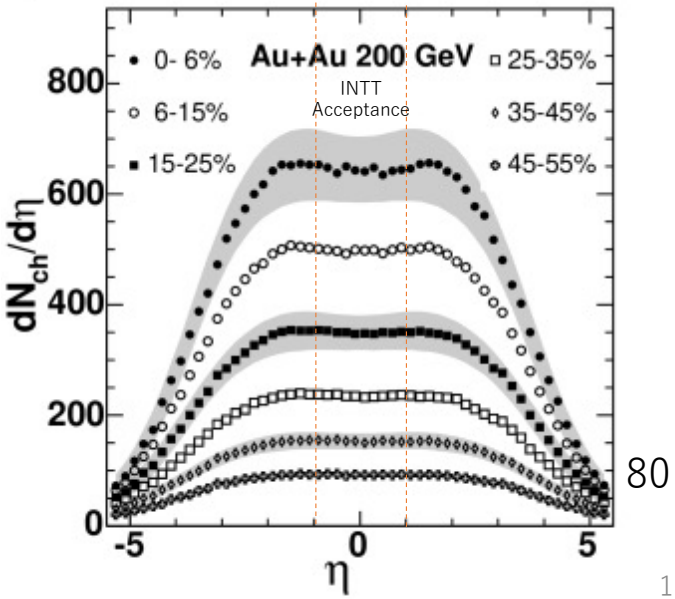


Ladder Geometrical Check

3. Hit Matching



- In early stage of the commissioning, sPHENIX is operated with magnetic field off.
  - Tracks are expected to be straight.
  - At the 45-55% centrality collision, $80/|\eta|$ tracks -> 4 tracks/half ladder -> 0.15 hit/chip.
  - Matching hits between L0 and L1 can be identified by eye using the event display without fancy tracking algorithm.



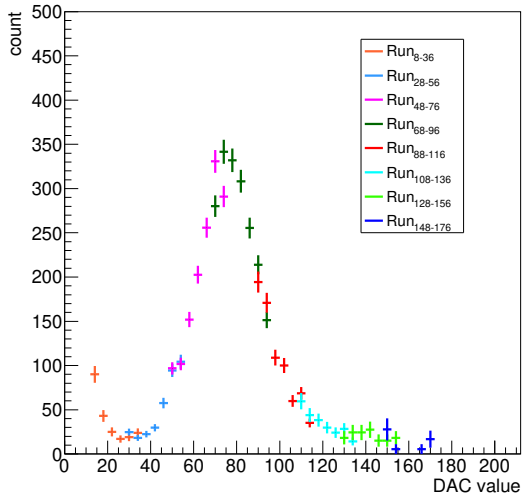
https://wiki.sphenix.bnl.gov/index.php/INTT_GEANT_model/geometry#/media/File:2020-05-30-160330_940x871_scrot.png

DAC Scan

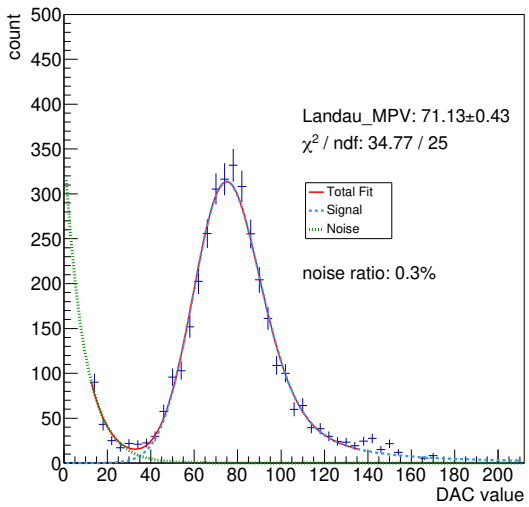
DAC Scan

Scan	1	2	3	4	5	6	7	8
DAC0	8	28	48	68	88	108	128	148
1	12	32	52	72	92	112	132	152
2	16	36	56	76	96	116	136	156
3	20	40	60	80	100	120	140	160
4	24	44	64	84	104	124	144	164
5	28	48	68	88	108	128	148	168
6	32	52	72	92	112	132	152	172
7	36	56	76	96	116	136	156	176

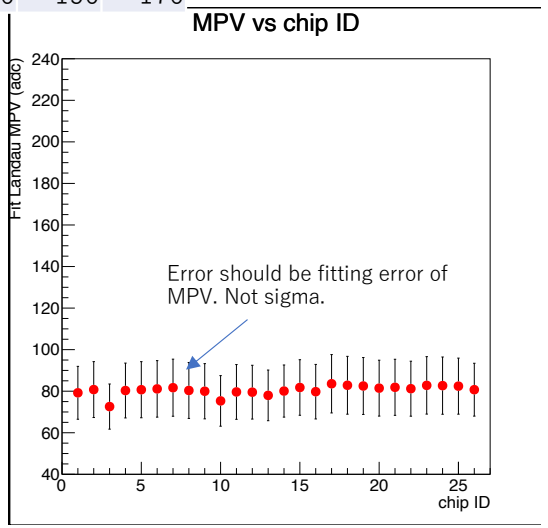
ビームテストと同じ設定で良いか？
オーバーラップbinは二つ？



- Chip-by-Chip Base
- Clustering
- Normalization btwn adjacent runs
- Concatenate all runs



- Fitting with Landau+Gaussian convolution function.



Half ladder by half ladder

All ladders
Save all fitting parameters:
MPV, Width, …

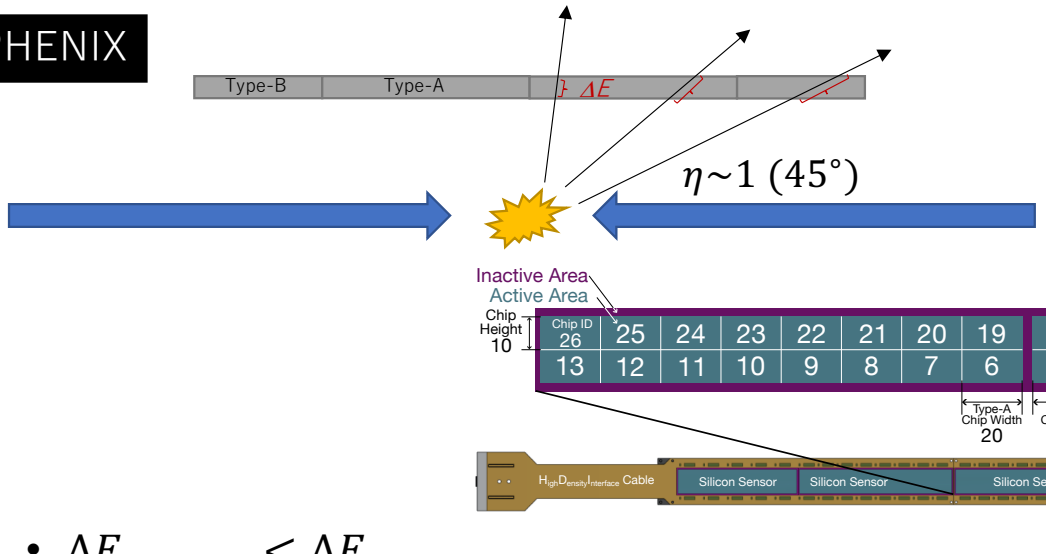
From ELPH annual report and Cheng-Wei's slide 2022/4/15

How Energy Deposit Looks like in sPHENIX?

DACのオーバーフローが出ちゃうか？

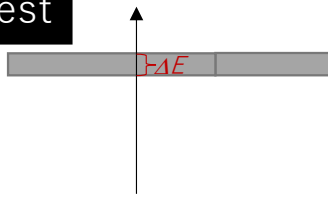
Cheng-Wei's slide 2022/4/15

sPHENIX

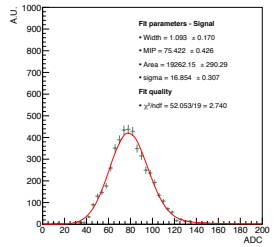


- $\Delta E_{Type-A} < \Delta E_{Type-B}$
- $\Delta E_{Chip13} < \Delta E_{Chip12} < \cdots < \Delta E_{Chip1}$
- $\Delta E_{Chip1} \sim \Delta E_{Chip13} \times \sqrt{2}$ $(\eta \sim 1)$
- $\Delta E_{Chip13} = \Delta E_{Chip26}$

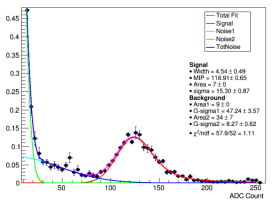
BEAM Test



Testbeam2021, 50 V
Positron beam, 1 GeV



Testbeam2019, 100 V
Proton beam, 120 GeV



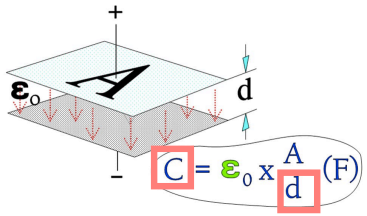
- $\Delta E_{Type-A} = \Delta E_{Type-B}$
- $\Delta E_{Chip13} = \Delta E_{Chip12} = \cdots = \Delta E_{Chip1}$
- $\Delta E_{Chip13} = \Delta E_{Chip26}$

$\Delta E^{sPHENIX}_{Chip13}@50V \sim \Delta E^{ELPH2021}_{Chip13}@50V$, $\Delta E^{sPHENIX}_{Chip13}@100V \sim \Delta E^{FNAL2019}_{Chip13}@100V$?
To be studied by a simulation in advance.

Bias Voltage Scan

Bias Voltage Dependence

Cheng-Wei's slide 2022/4/15



$$W = \sqrt{2\epsilon\,(V + V_{bi})/Ne} = \sqrt{2\rho\mu\epsilon(V + V_{bi})}$$

d

$$C = \sqrt{\frac{\varepsilon_0\varepsilon_r}{2\mu\rho|V|}} \cdot A$$

$$\frac{dE/dx \cdot d}{I_0} = \frac{3.87\cdot10^6\,\mathrm{eV/cm}\cdot0.03\,\mathrm{cm}}{3.62\,\mathrm{eV}} \approx 3.2\cdot10^4\,\mathrm{e^-h^+-pairs}$$

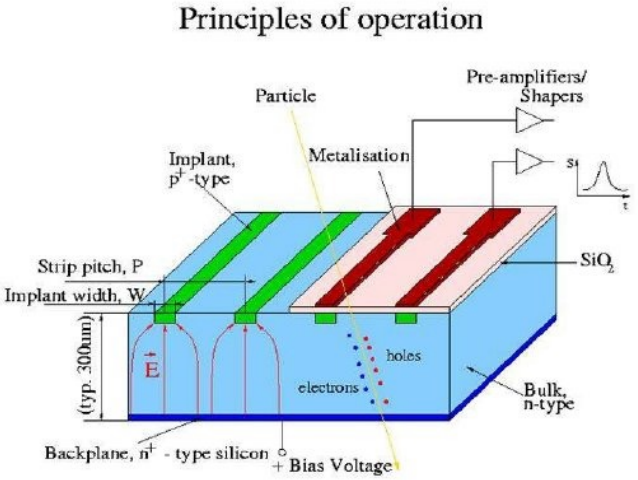
Signal

Based on the theory :

$$C \propto \frac{1}{d} \propto \frac{1}{\sqrt{V}} \propto \frac{1}{signal}$$

C : capacitance
d : the distance of the depletion region
V : supply bias voltage
signal : edep

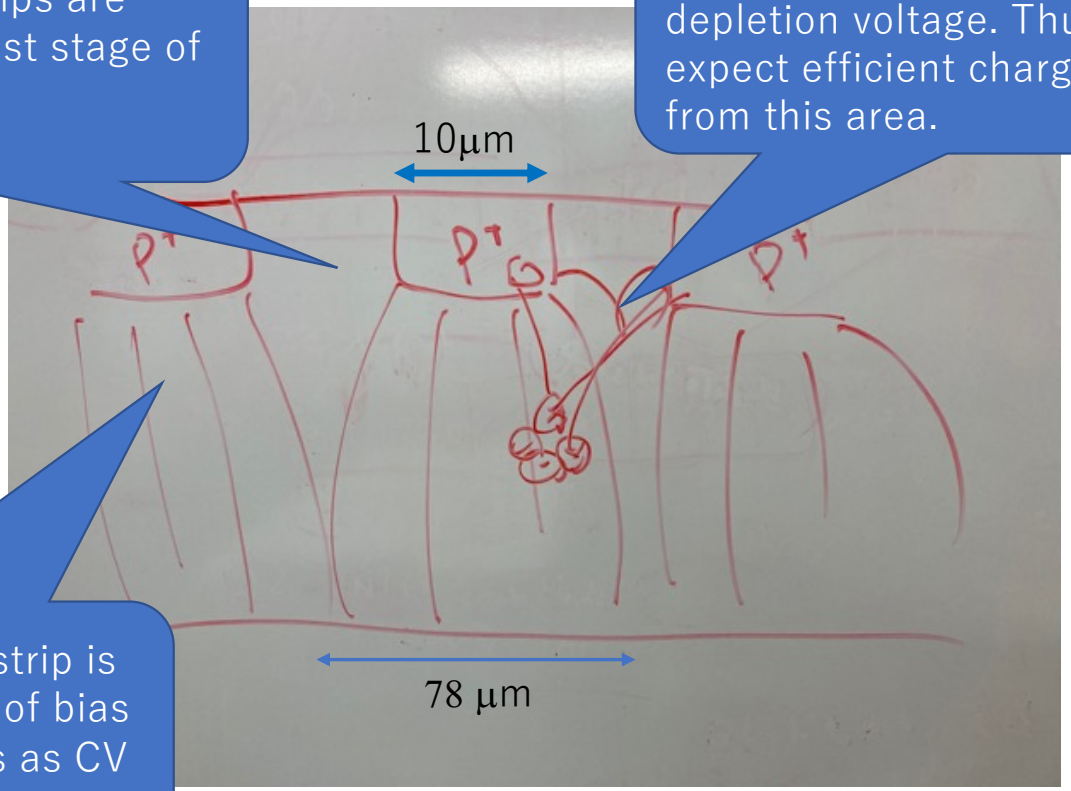
Itaru's Slide 2022/06/22



Electric field at non-fully depleted voltage

Electric field between strips are developed towards the last stage of fully depletion voltage.

This area between strips might not be depleted even slightly below the depletion voltage. Thus we cannot expect efficient charge collection from this area.



REALITY

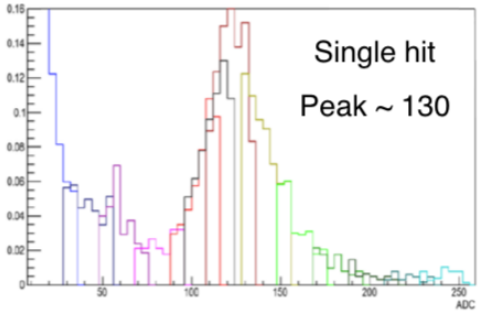
The electric field just below strip is well developed as a function of bias voltage. This directly appears as CV response.

The best way to prove this hypothesis is to see the position dependence of the resolution within the strip width.
We'll see a dip in the efficiency distribution around the edge of a strip.

Not sure if this is doable with cosmic ray…

Bias Voltage Scan Plan

- Importance: It is likely we ends up with operating <100V due to over current of some silicons.
- We need to know the collecting # of electrons below 100V.



Scan	1	2	3	4	5	6	7	8
DAC0	8	28	48	68	88	108	128	148
1	12	32	52	72	92	112	132	152
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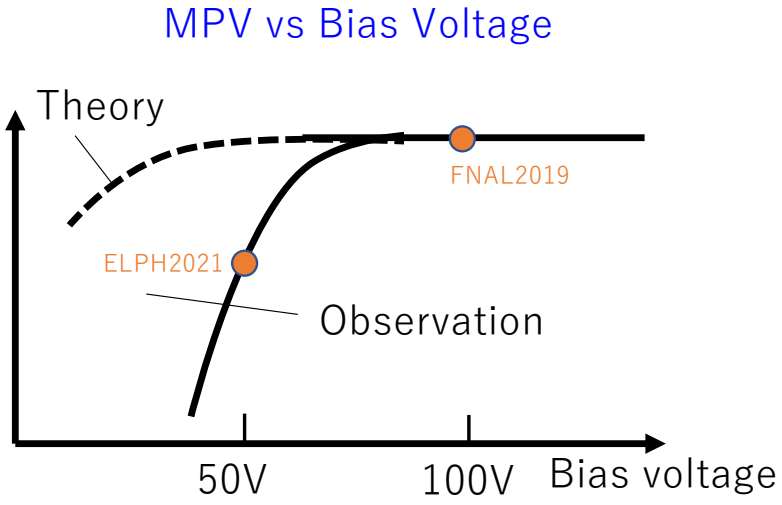
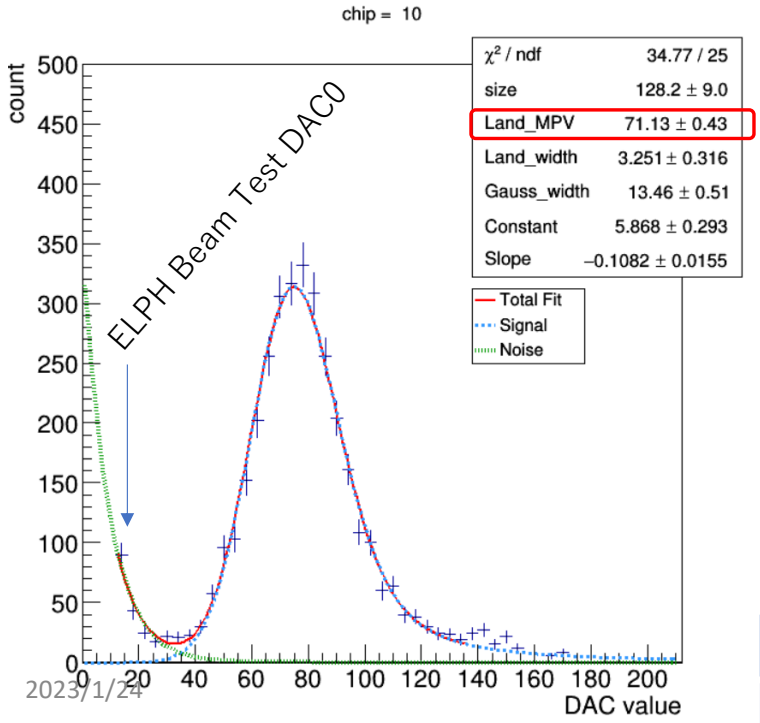
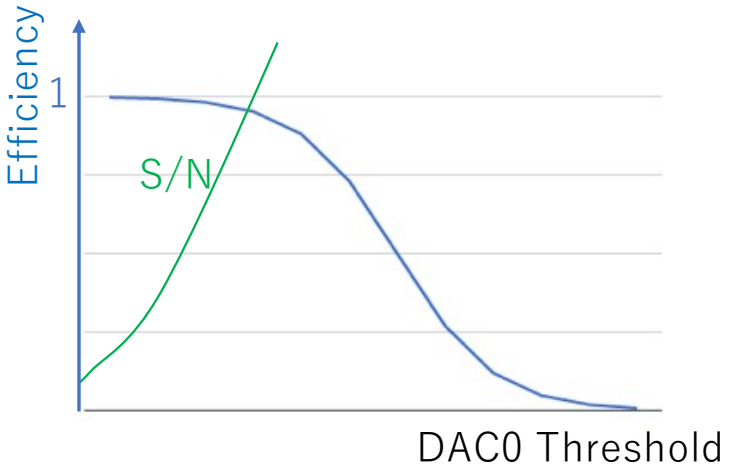


- Scan at 90V, 80V, 70V, 60V, 50V only around MIP region.
- Need immediate semi-online analysis (DAC Scan code) if data is satisfactory to cover MPV peak.
- The goal is to make the plot of MPV vs. Bias voltage.
- Not sure if we can run a simulation.

DAC0 Threshold Scan

DAC0 Threshold Scan





DAC0	12	13	14	15	16	17	18
S/N							
Efficiency							

- We may need to customize the DAC0 value Chip-by-Chip Basis for noisy chips
- Need to confirm MPV/MIP are same for all Chips.

Yield Uniformity

- Online Monitor

Monitoring

1. Define online monitor. Develop and test anomaly (dead/hot channel) checker.
2. Establish flushing anomaly checker results to database.

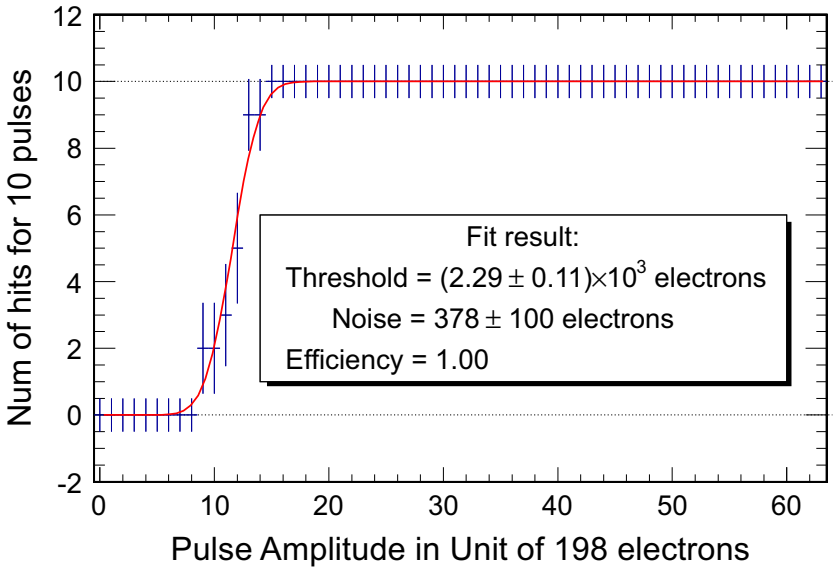


Fig. 35. Typical calibration data for a single channel (data points), fit with a normal cumulative distribution function.

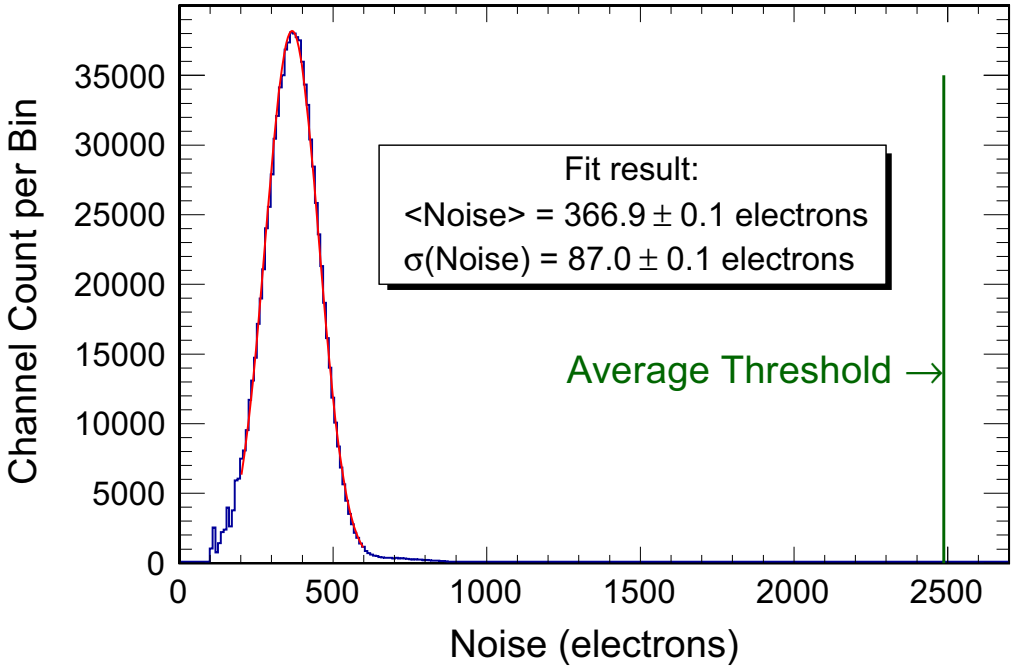


Fig. 36. Histogram of the noise parameter, σ, for all channels under operating conditions, in a typical calibration run. A Gaussian distribution fit to the data gives a mean noise level of 367 electrons. The nominal discriminator threshold at ~2500 electrons is shown by the vertical line.