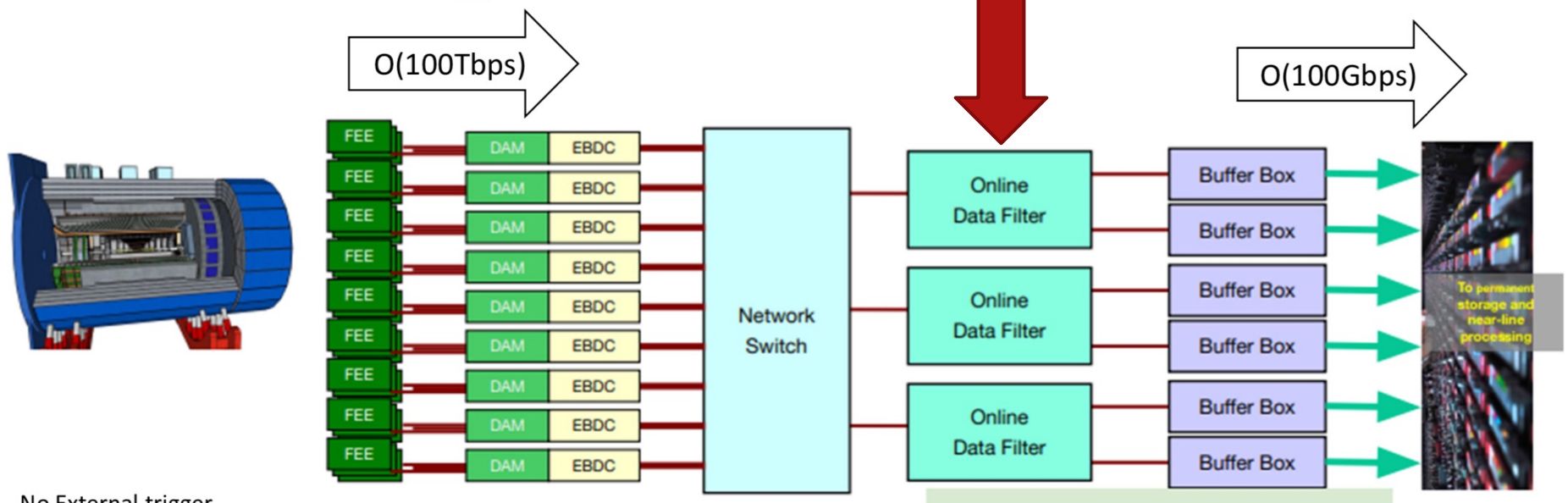
Free Streaming Readout

T. Gunji (CNS, Tokyo)

- **Will be a future standard DAQ system**



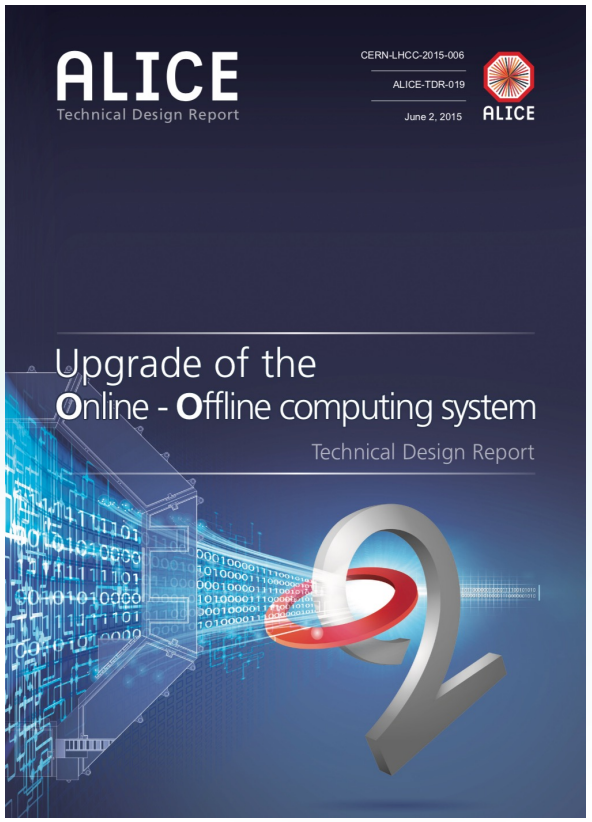
- No External trigger
- All collision data digitized but aggressively zero suppressed at FEE
- Low / zero deadtime
- Event selection can be based upon full data from all detectors (in real time, or later)
- Collision data flow is independent and unidirectional-> no global latency requirements
- Avoiding hardware trigger avoids complex custom hardware and firmware
- The “Front End Processing”, programmable hardware between the FEEs and the DAQ computers, is deemphasized relative to the yellow report, but should not be precluded.
- Data volume is reduced as much as possible at each stage

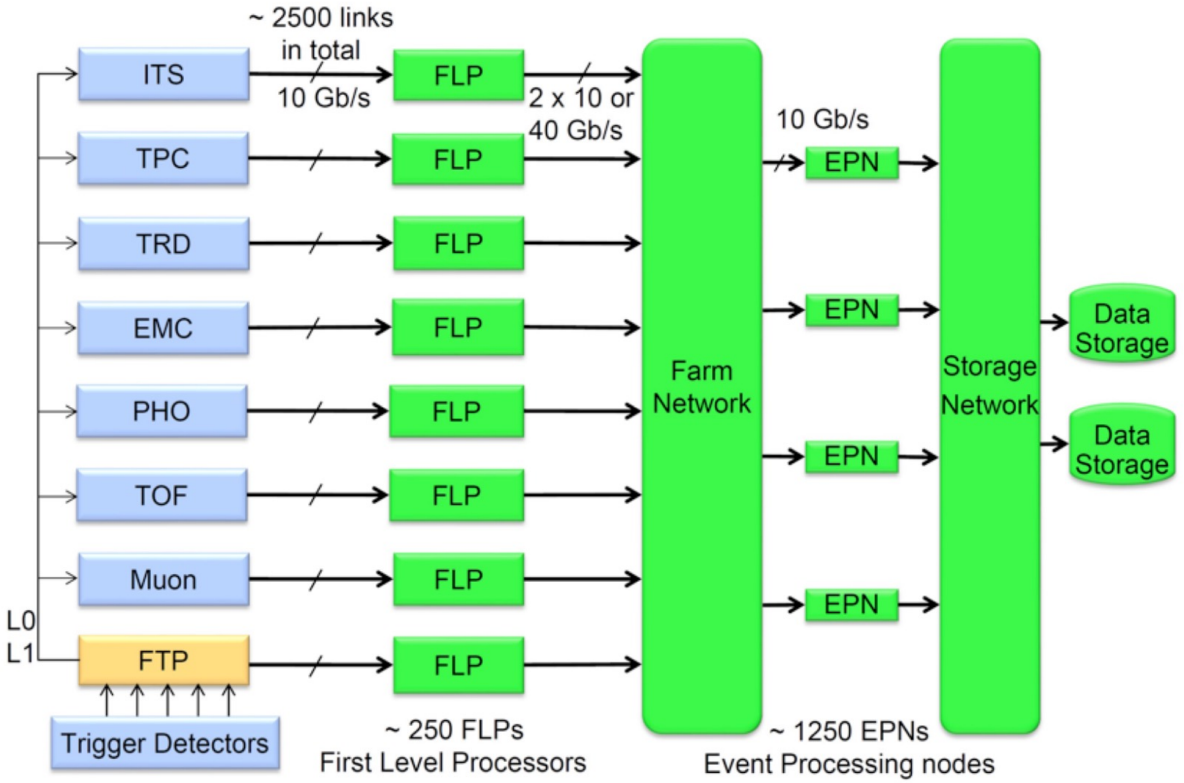
Stored data volumes
~O(100Pb) per run

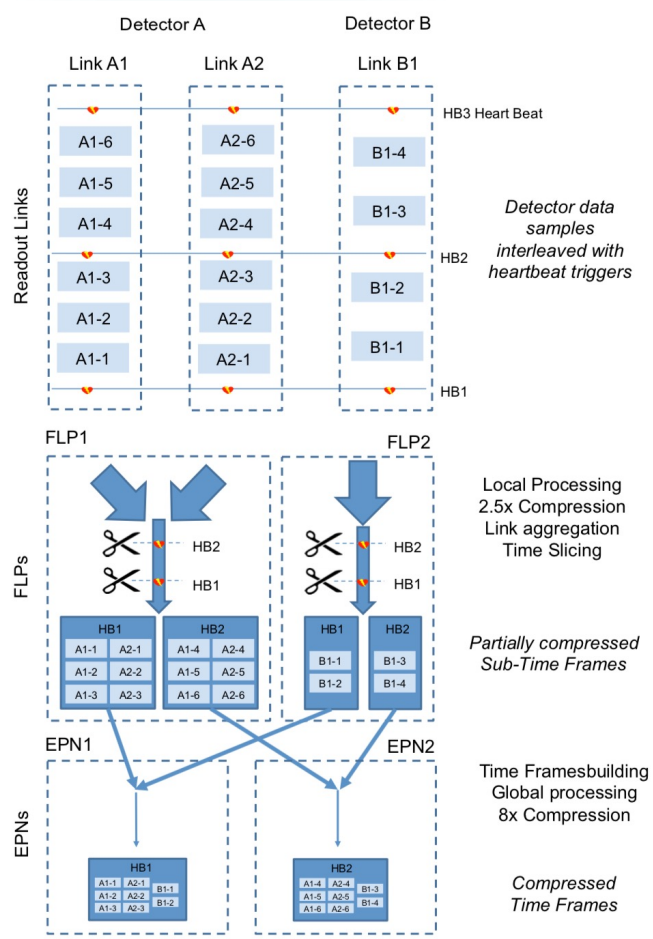
ALICE O²

T. Gunji (CNS, Tokyo)

50kHz Pb-Pb collisions
TPC moved from triggered readout (gating grid) to continuous readout with GEMs
ALICE had experiences on hardware accelaration (GPUs) in HLT during Run2
→ New Free streaming DAQ (O²) proposed in 2015





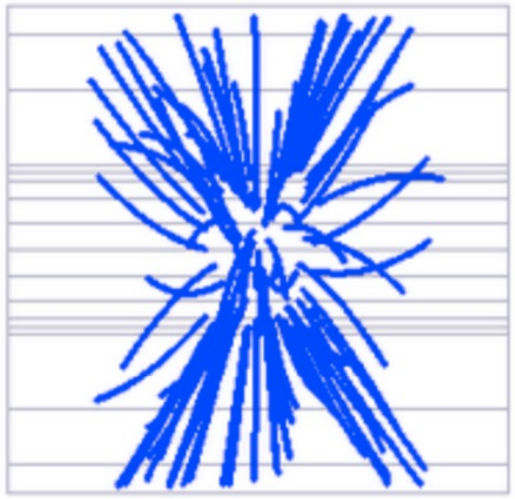


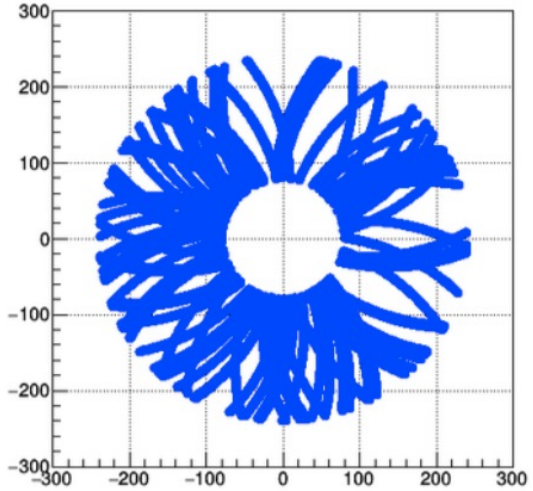
T. Gunji (CNS, Tokyo)

GPU processing

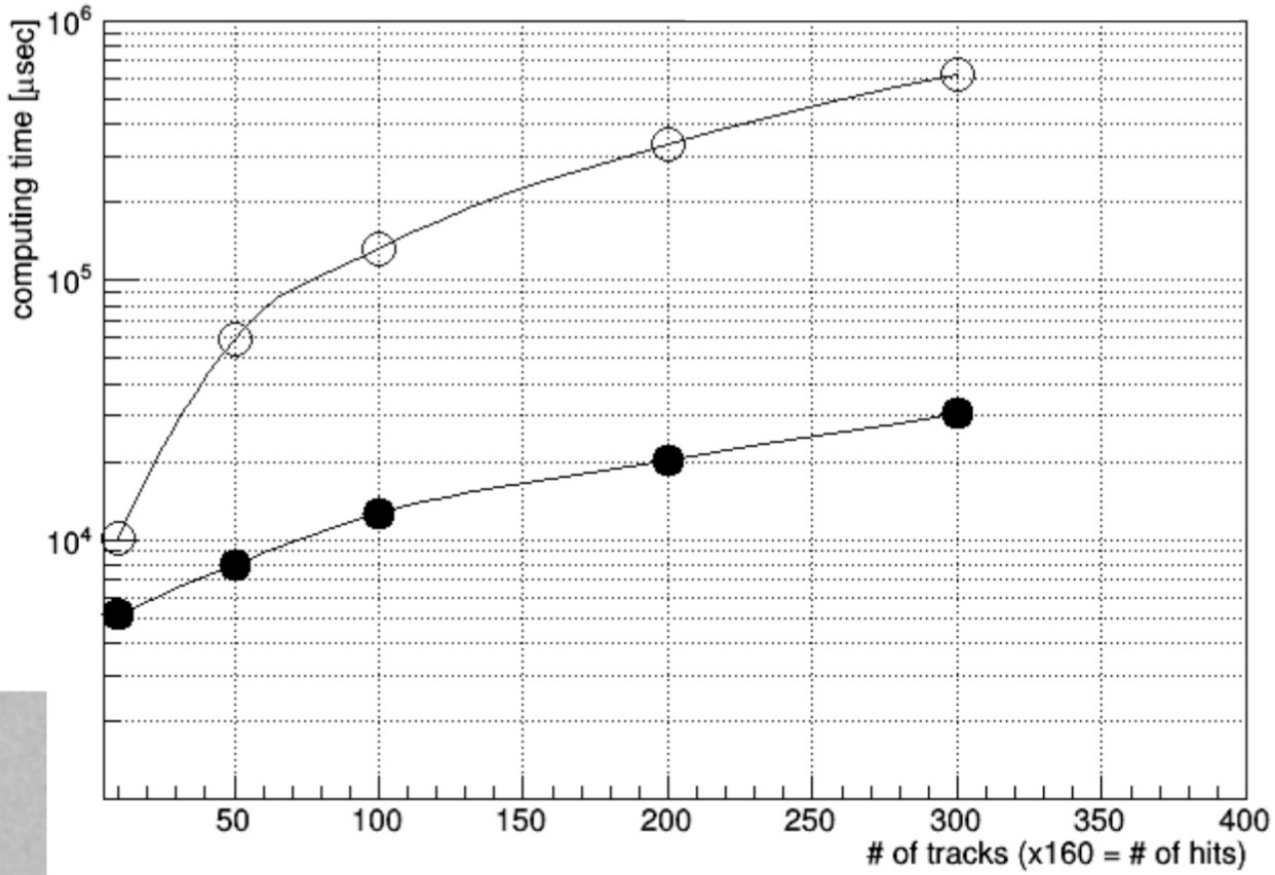
2015年くらい？

TPC Tracking

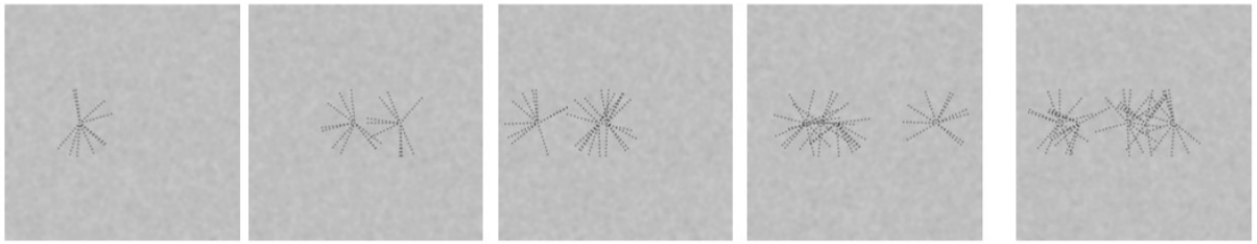




GPU = NVIDIA GTX970
CUDA 7.5, 8.0



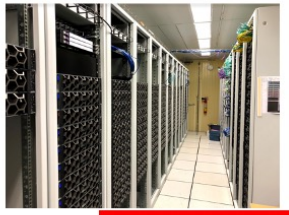
Pile-up detection using ML

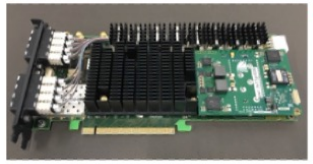


ALICE O² deployed from Run3

T. Gunji (CNS, Tokyo)

O2/FLP
CR1 – First Level Processors
Receive detector data and processing on PCIe-based FPGA board (CRU)





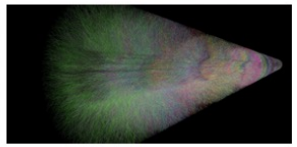
Continuous
Unmodified
Raw data

TPC 3.3 TB/s
ITS2 40 GB/s
Rest 25 GB/s

CTP
Central Trigger Processor
Distribution of timing info, heartbeat trigger

TPC 570 GB/s
ITS 40 GB/s
Rest 5 GB/s

Sub-Timeframes (10-20ms)



O2/EPN
CR0 - Event Processing Nodes
~2000 GPU & CPU

Compressed
Timeframes (CTF)
Calibration data

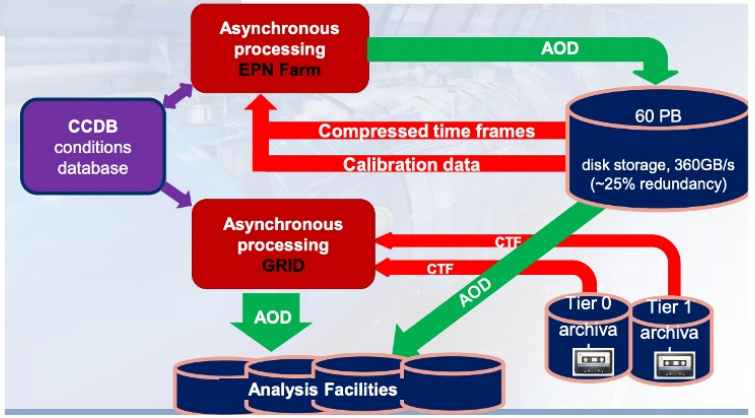
60 PB
disk storage,
360 GB/s

2/3 CTF
1/3 CTF

Tier0
archival

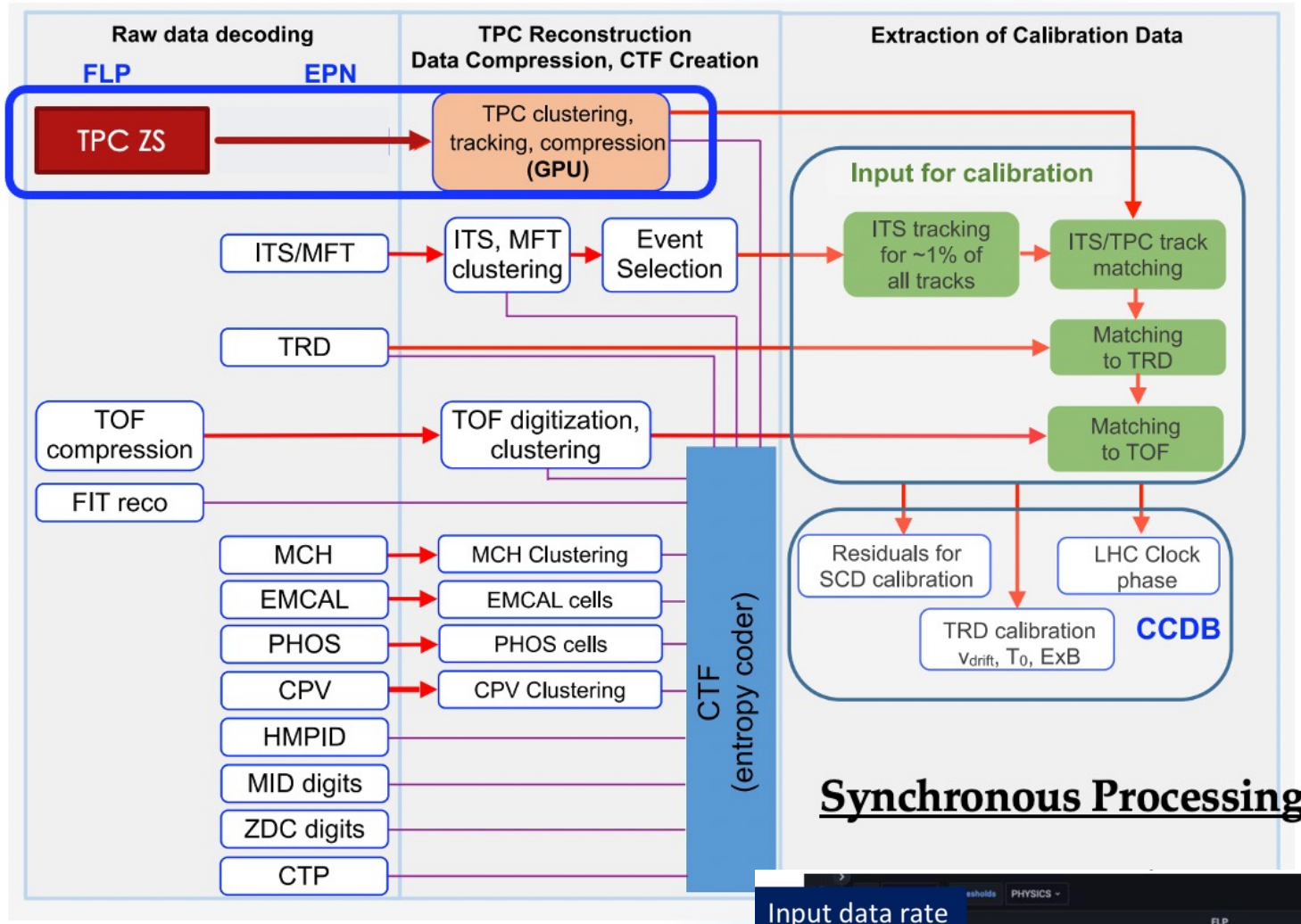
Tier1
archival

O2/PDP
Physics and Data Processing on EPN
- **Synchronous reconstruction**
- **Calibration & asynchronous reconstruction (and event selection only for pp)**
- **Utilize ~2000 GPU and HPC**

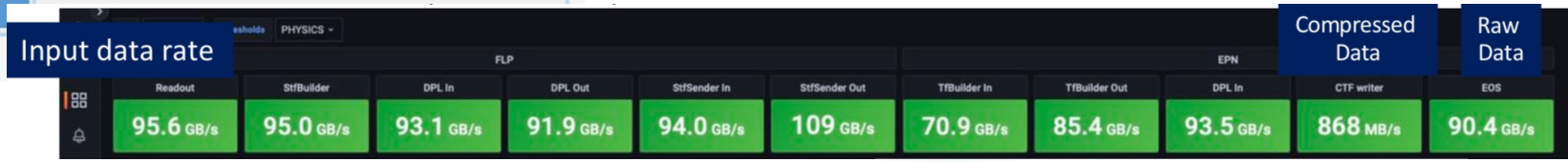


ALICE O² deployed from Run3

T. Gunji (CNS, Tokyo)



8 GPU/EPN, 250 EPNs

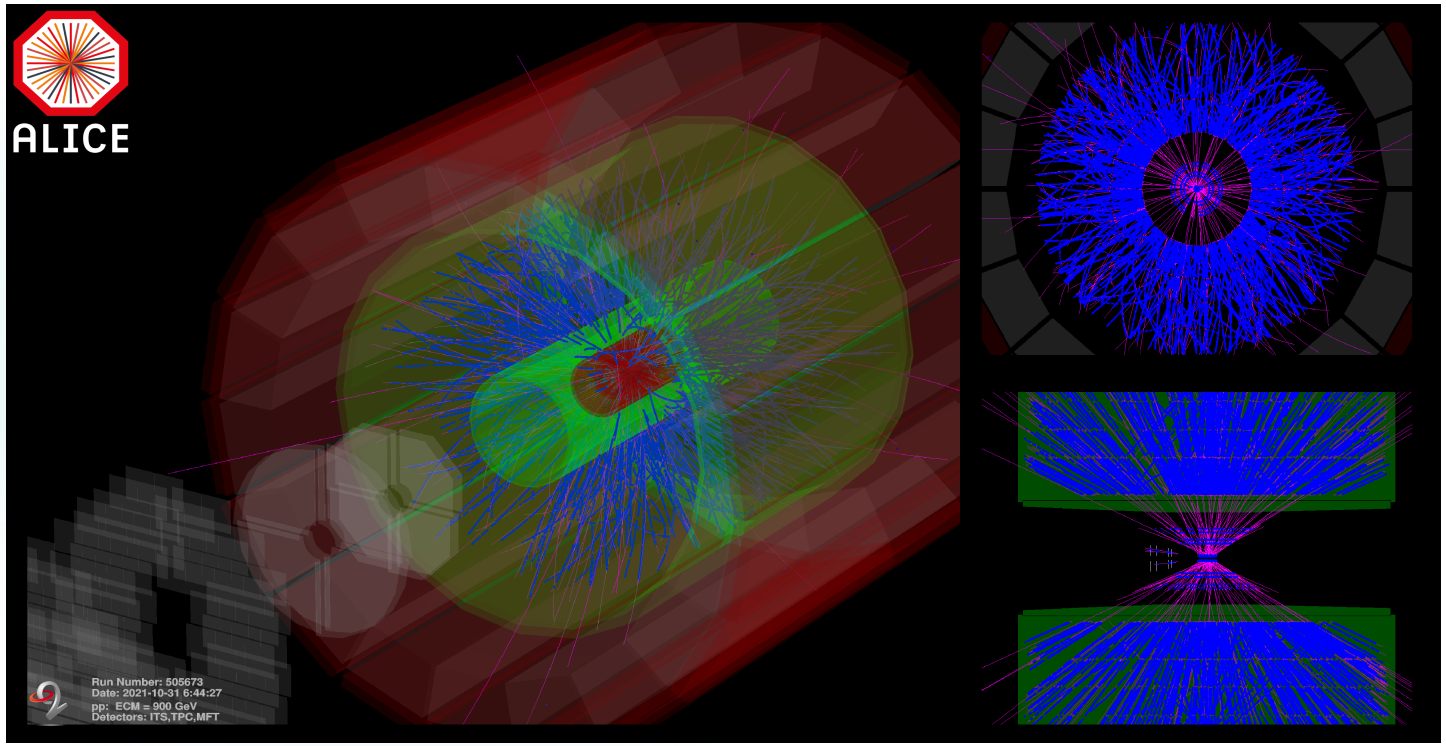


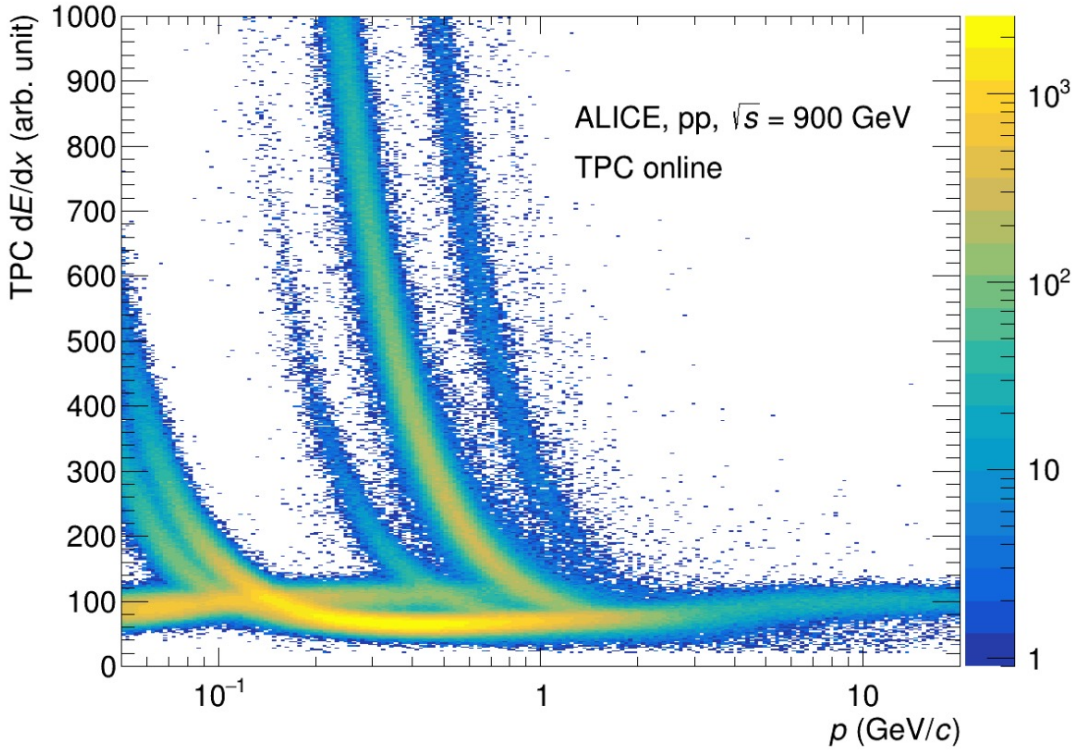
Online processing performance

T. Gunji (CNS, Tokyo)

- Online clustering, tracking, PID,

All are done ONLINE

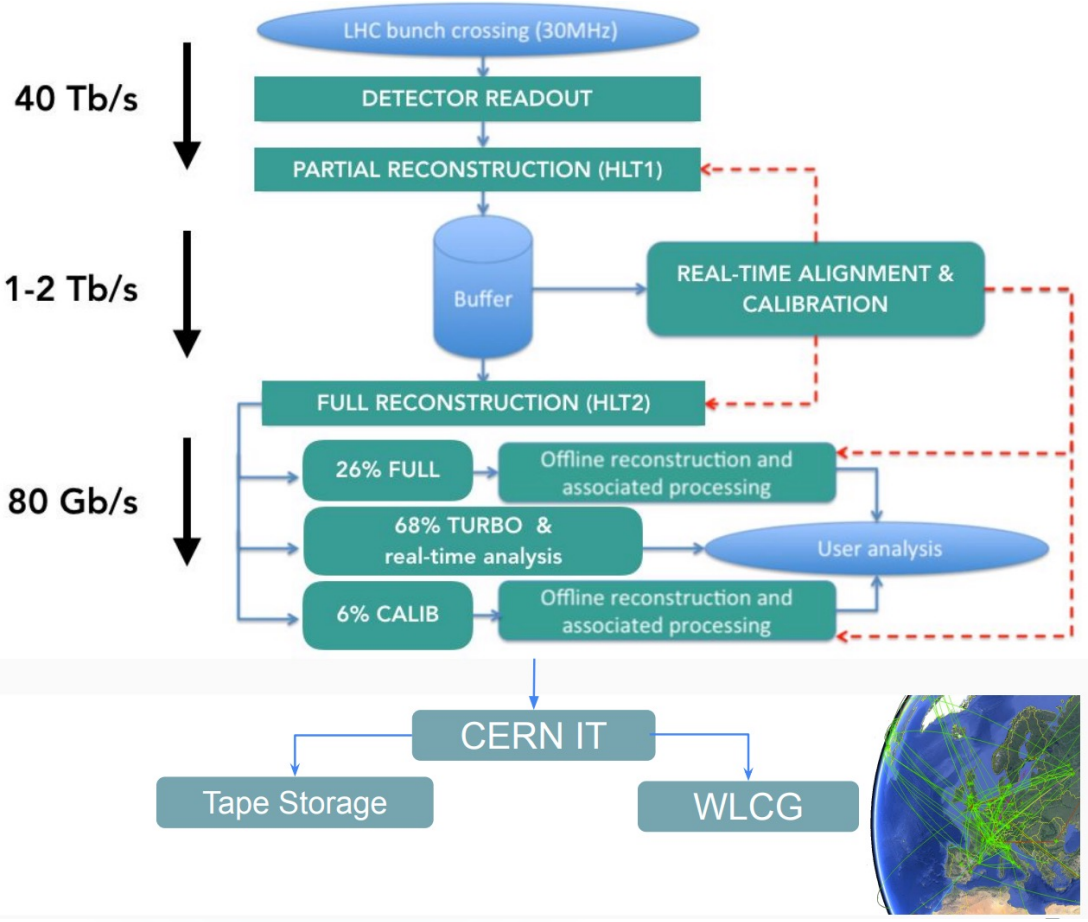


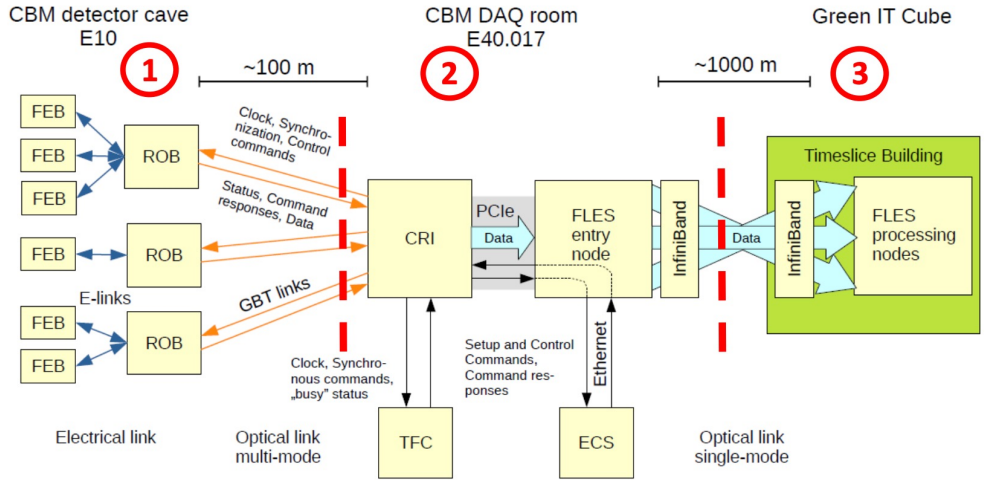


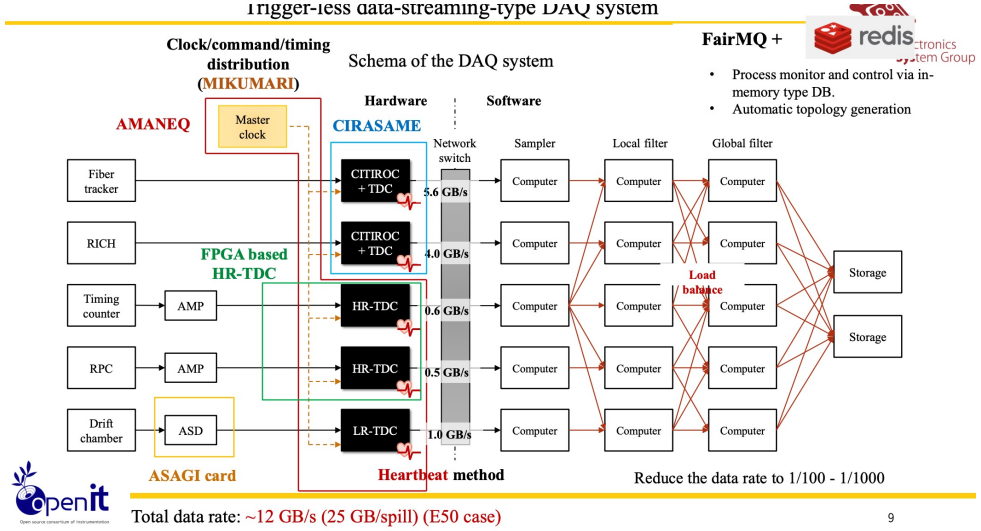
T. Gunji (CNS, Tokyo)

Will be used in many experiments

- ALICE, LHCb, sPHENIX, CBM, J-lab, J-PARC, etc…



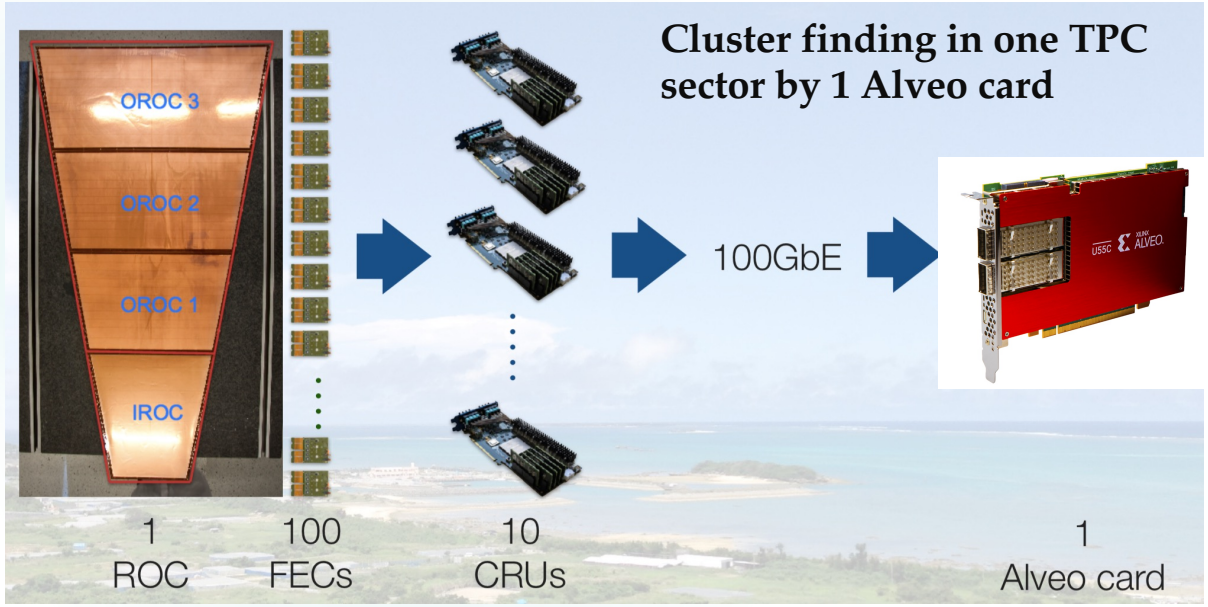




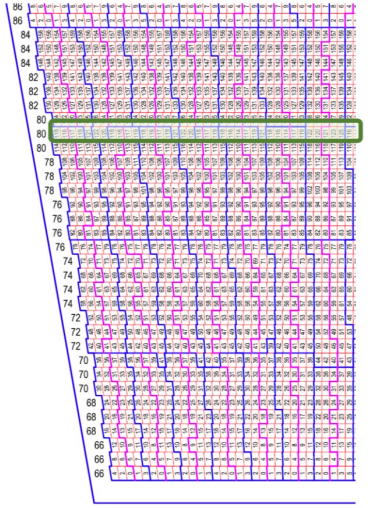
T. Gunji (CNS, Tokyo)

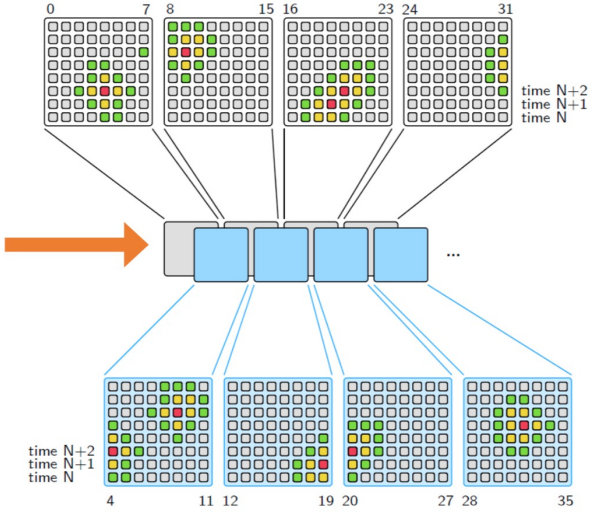
Recent Progress

- ALICE TPC clustering on FPGA (Xilinx Alveo u55c, u280)
  - High Level Synthesis (C++)



- The heaviest processing in our FPGA
- find local maxima in pad-timebin 2D space
- processor modules
  - scan rectangular regions
  - optimize size v.s. number of processors
  - available clock cycle is the boundary condition



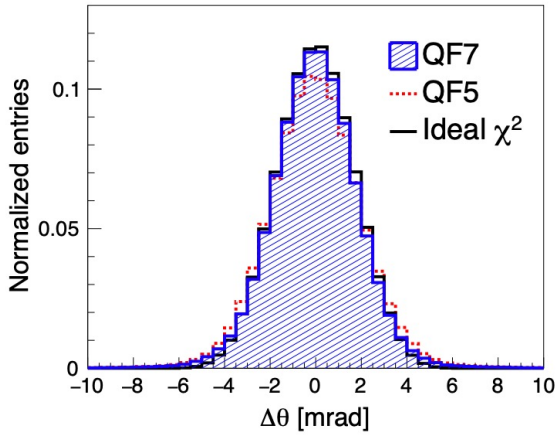


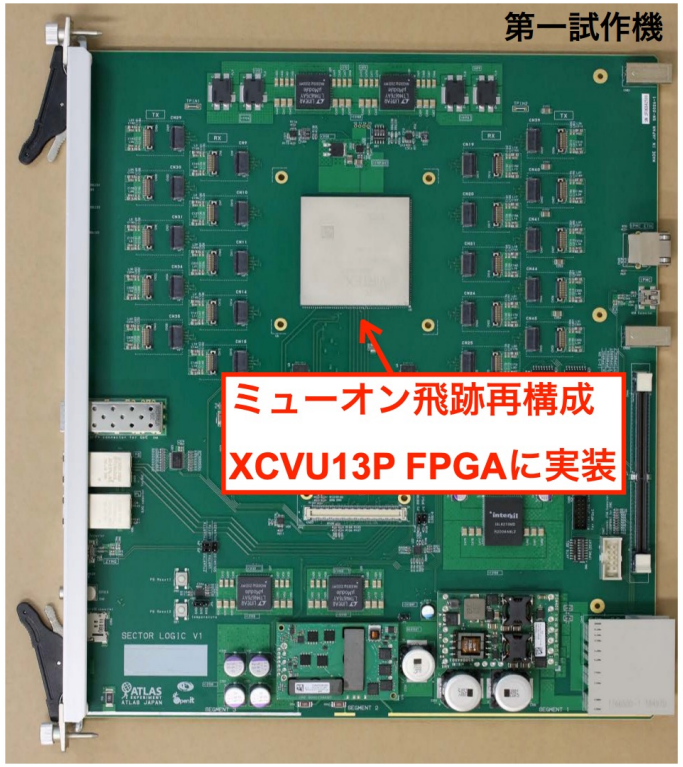
S. Klewin's PhD thesis, Heidelberg

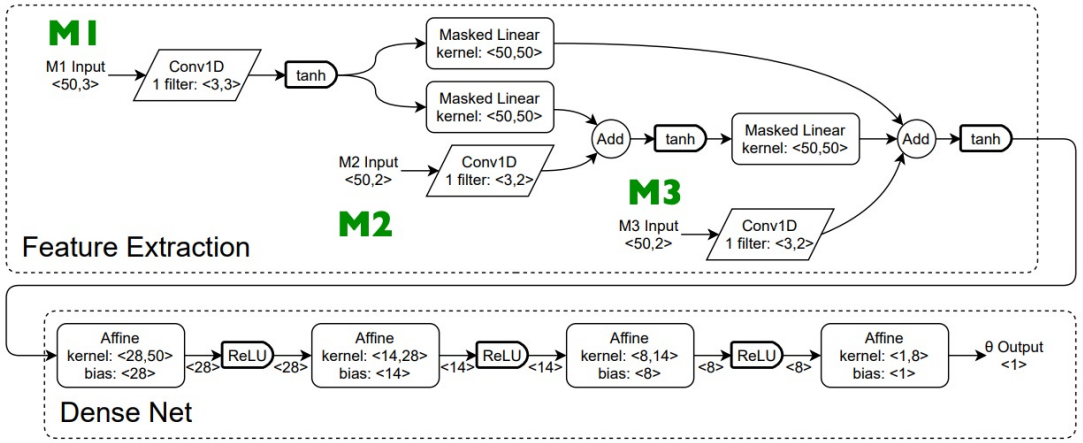
T. Gunji (CNS, Tokyo)

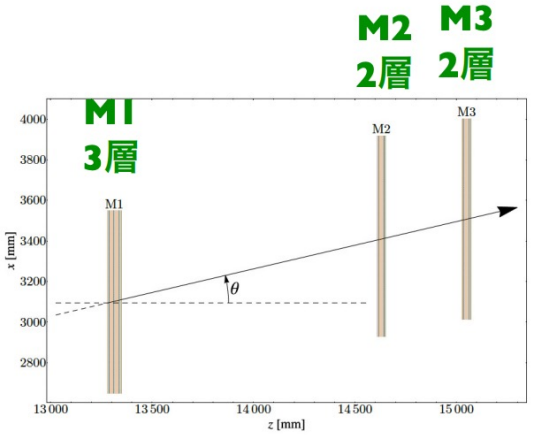
Online tracking using ML

- **ATLAS (Prof. Horii-san)**
  - 機械学習をFPGAに実装すると高速(100ns)でミューオンを再構成









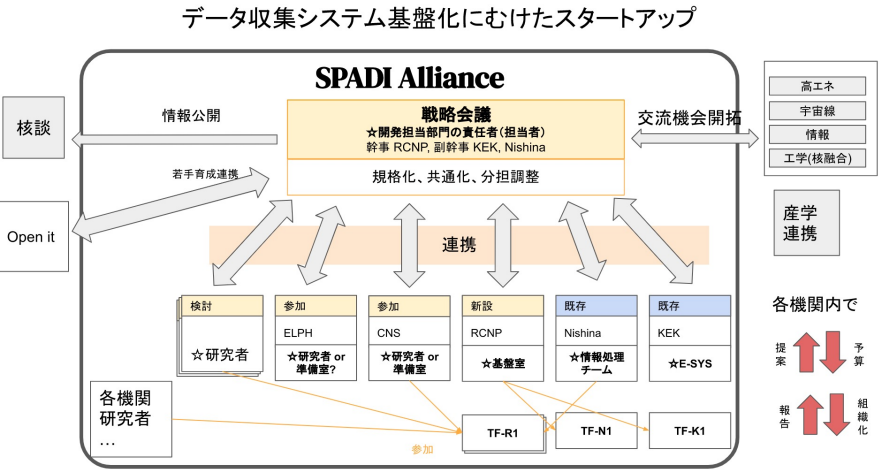
Model	Resolution [mrad]	Latency [ns]	DSP48	LUT	FF	BRAM
BL	1.9	-	-	-	-	-
QF7	2.0	69	1,389 (45%)	34,848 (8.0%)	5,433 (0.6%)	75 (2.8%)
QF5	2.2	69	88 (2.9%)	40,039 (9.3%)	3,419 (0.4%)	75 (2.8%)
QF3	2.8	56	2 (< 0.1%)	21,682 (5.0%)	2,242 (0.3%)	75 (2.8%)

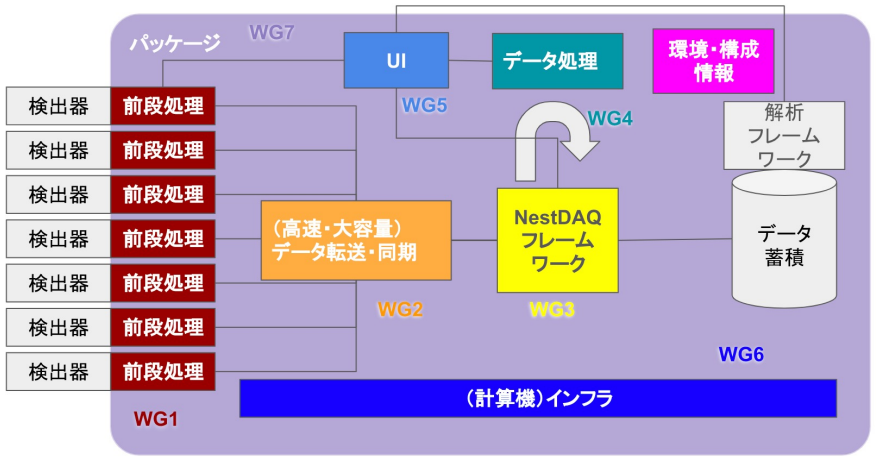
リソース使用率は、Super Logic Regionあたりの値

T. Gunji (CNS, Tokyo)

SPADI-Alliance

- "Signal Processing and Data Infrastructure – Alliance (SPADI-Alliance)" in Japan NP community to build common Front End and DAQ system.
  - https://www.rcnp.osaka-u.ac.jp/~spadi/
  - ~80 members



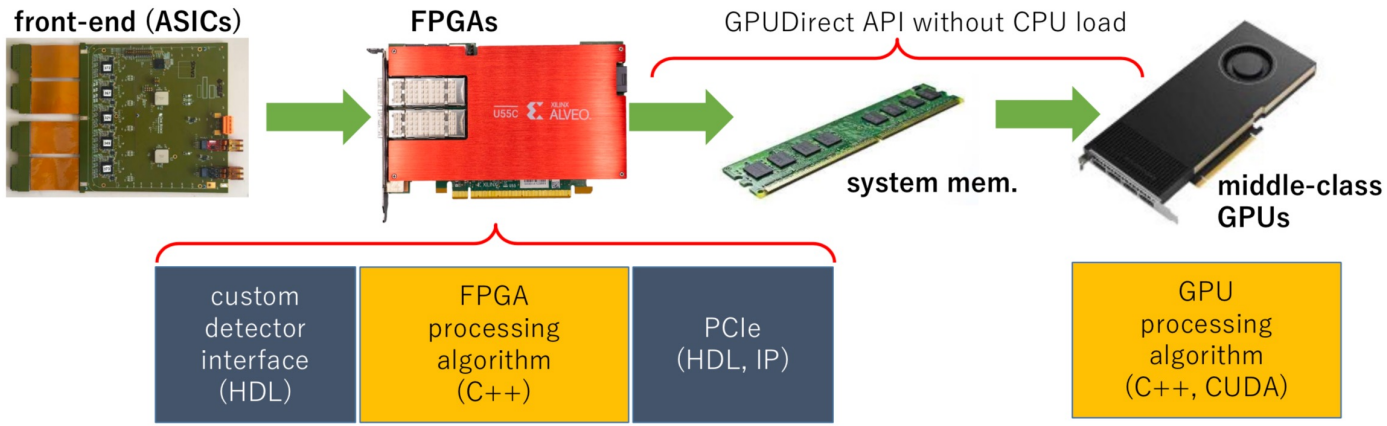


1. アナログ＋前段処理　（本多@KEK）
2. データ転送・同期（馬場@RNC）
3. NestDAQ フレームワーク（五十嵐@KEK）
4. データ処理（郡司@CNS）
5. ユーザーインターフェース (?)
6. インフラ（堀田@RCNP）
7. パッケージ・基盤化 (?)

T. Gunji (CNS, Tokyo)

Interest in contributing DAQ

- Plans for ePIC
  - Data processing and software trigger using hardware acceleration (FPGA, GPU, CPU)



EPIC Electronics / DAQ

Standard Component Names and Functions

Name	Sensor	Adapter	Front End Board (FEB)	Readout Board (RDO)	Data Aggregation Module (DAM)	Computing
Sharing	Detector Specific	Detector Specific	Detector Specific	Few Variants	Common	Common
Function	-Multi-Channel Sensor	-HV/Bias distribution -HV divider -Interconnect routing	-Amplification -Shaping -Digitization -Zero Suppression	-Communication -Aggregation -Formatting -Data Readout -Config & Control -Clock &Timing	-Computing Interface -Aggregation -Software Trigger -Clock & Timing -Config & Control	-Data buffering and sinking -Run Control -Calibration Support -QA / Scalers -Collider Feedback -Event ID/Building? -Software Trigger -Monitoring
Attributes	-MAPS -AC-LGAD -MCP-PMT -SiPM -LAPPD	-Sensor Specific -Passive	-ASIC/ADC -Discrete -Serial Link	-FPGA -Fiber Link	-Large FPGA -PCIe -Potentially Ethernet	