

第22回高エネルギーQCD・核子構造勉強会

📅 Friday 29 Mar 2024, 13:00 → 17:00 Asia/Tokyo

📍 東海1号館116号室 (KEK 東海キャンパス)

👤 Shinya Sawada (KEK), Shunzo Kumano (KEK), Yuji Goto (RIKEN)

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ePIC実験測定器の技術と応用

郡司 卓

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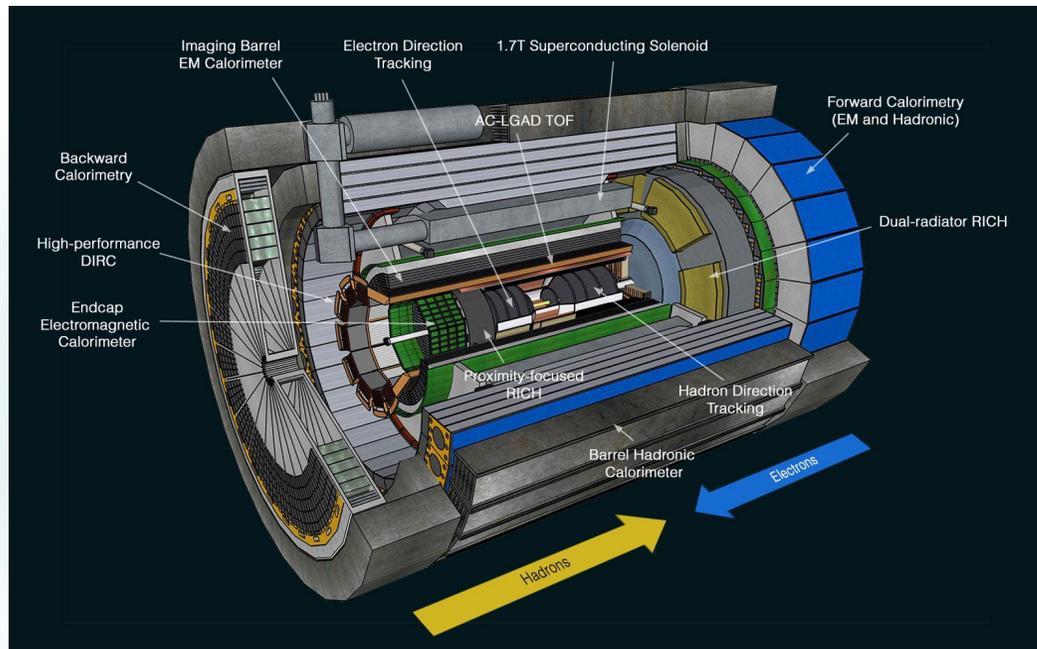
目次

- ▶ **高エネルギー原子核物理の将来実験と測定器**
 - ▶ ePIC実験とALICE3実験
- ▶ **今後の基盤となる測定器技術やシステム**
 - ▶ MAPS
 - ▶ LGAD
 - ▶ Streaming DAQ

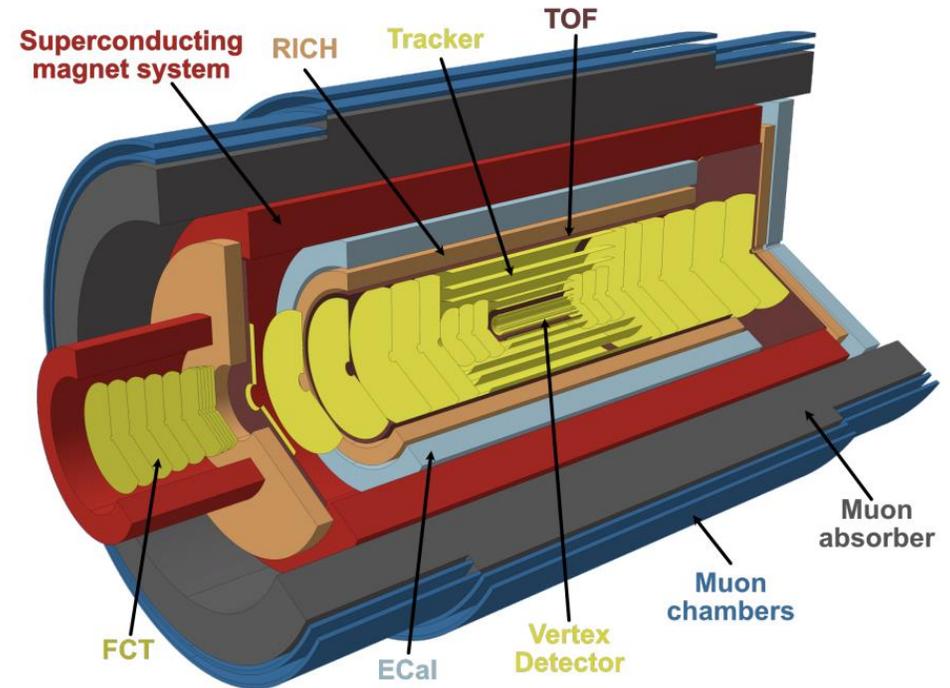
高エネルギー原子核物理の将来実験

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▶ ePIC実験@EIC (2030-)



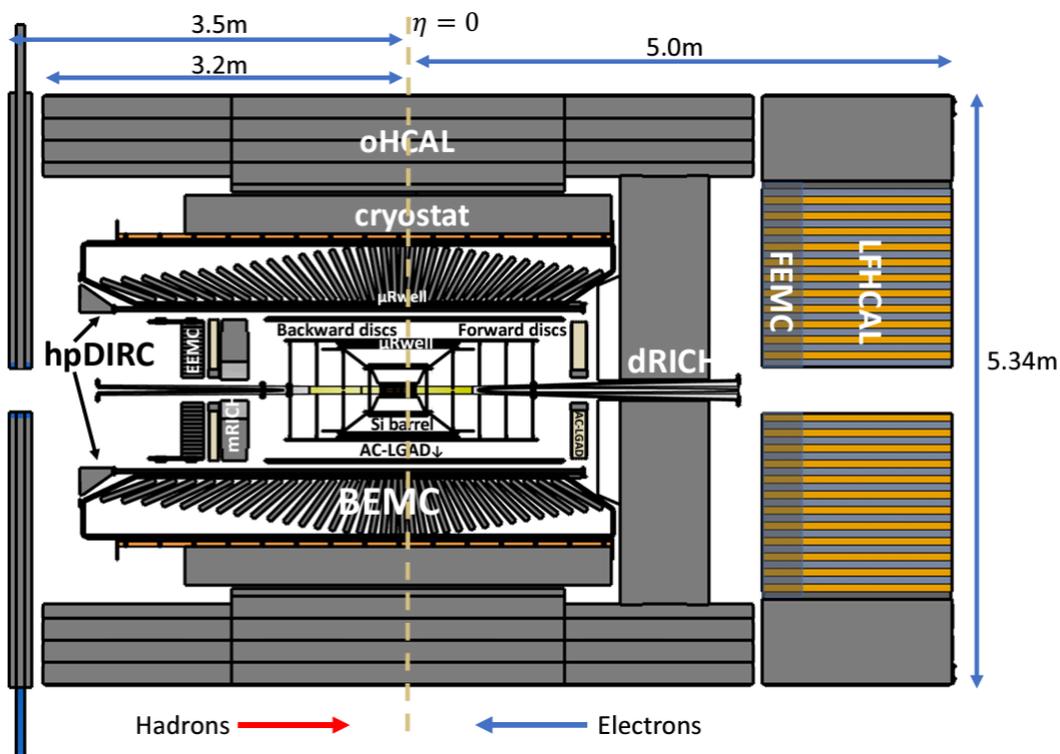
▶ ALICE3実験@CERN-LHC (2035-)



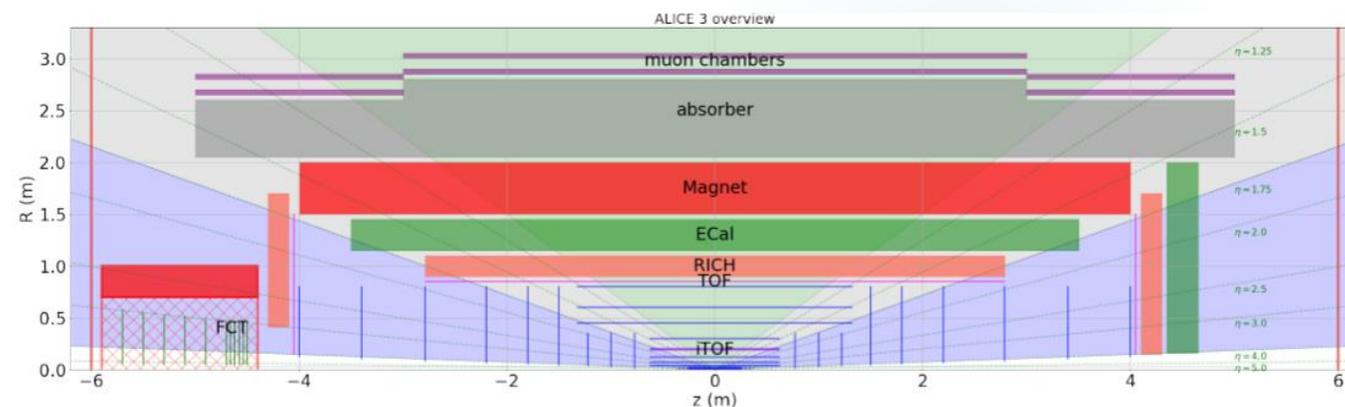
高エネルギー原子核物理の将来実験

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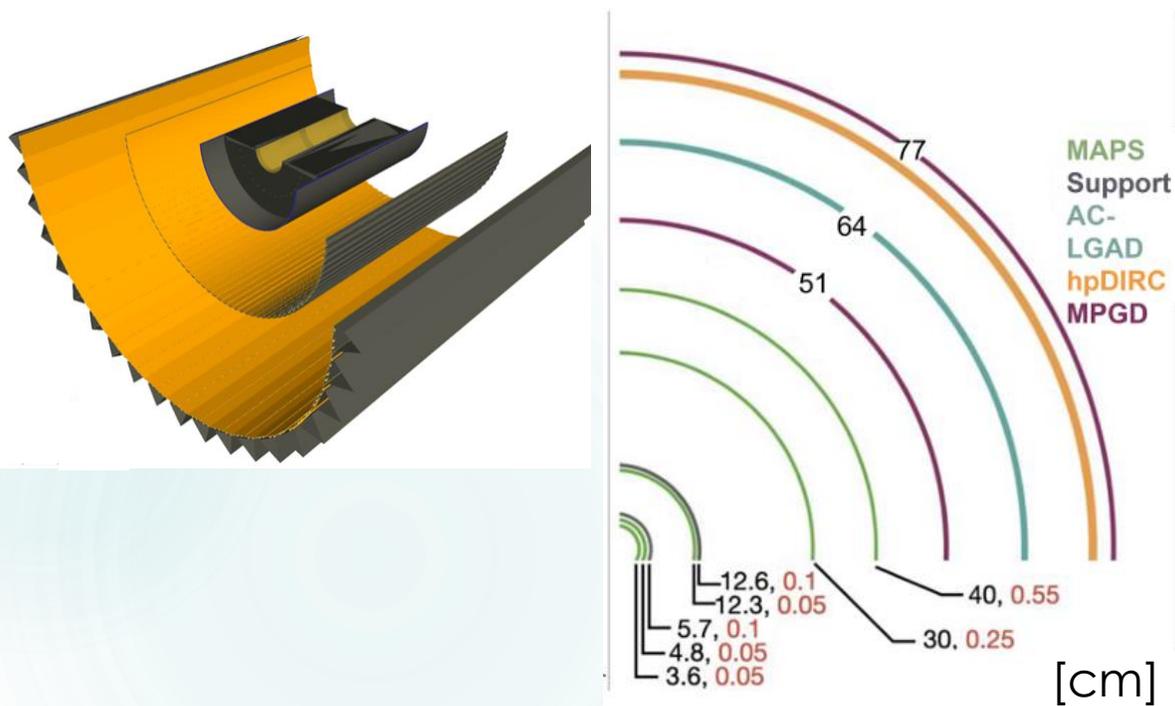
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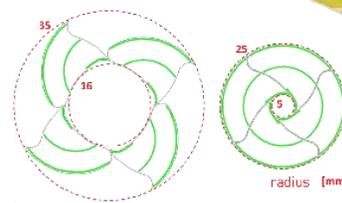
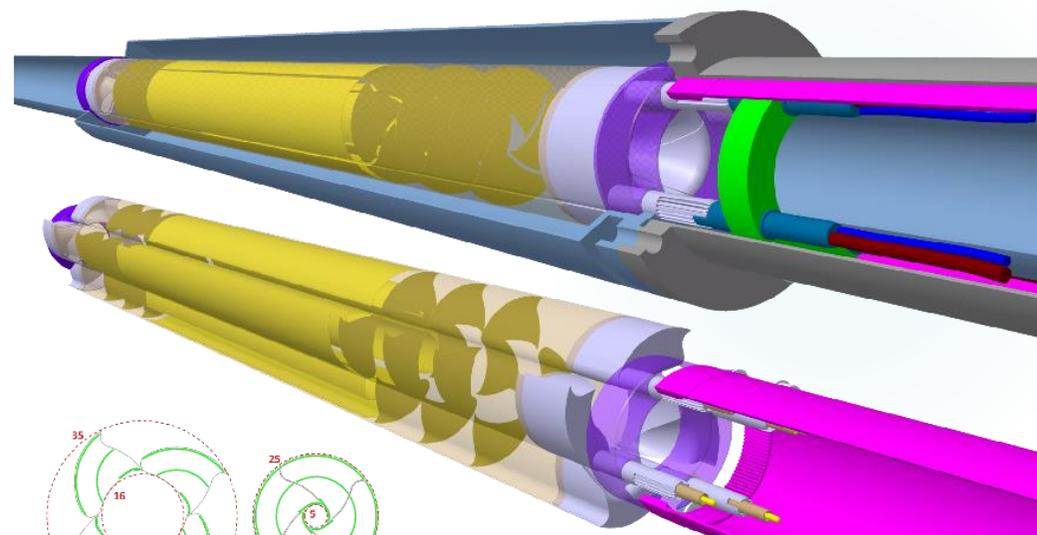
- 飛跡と衝突点同定のためのシリコンピクセル検出器
- PIDのための飛行時間検出器(TOF)
- PIDのためのRICH検出器
- 電磁カロリメーター
- (ハドロンカロリメーター)

高エネルギー原子核物理の将来実験

▶ ePIC実験@EIC (2030-)



▶ ALICE3実験@CERN-LHC (2035-)

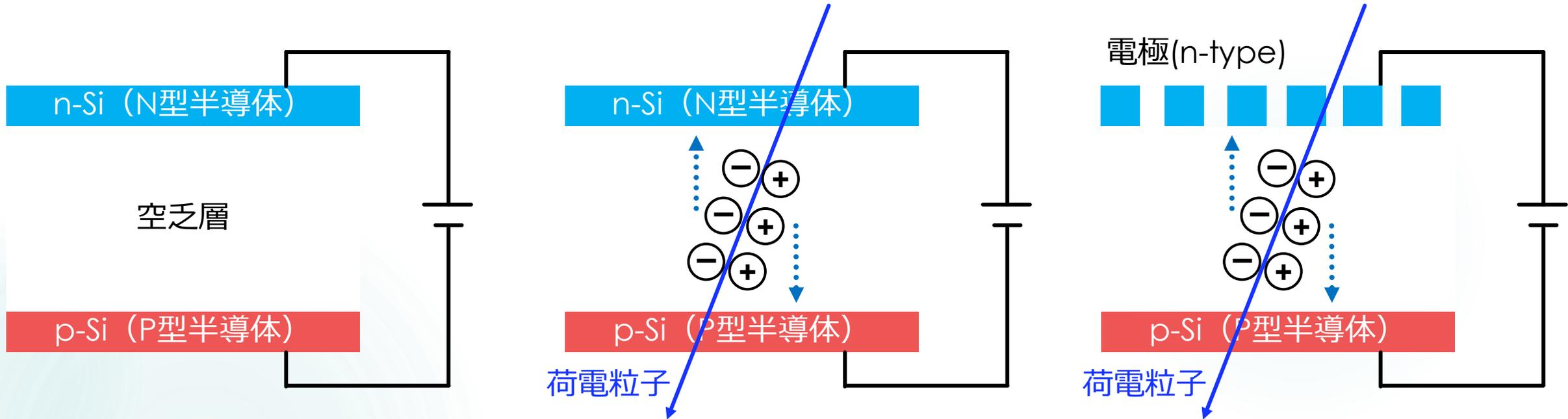


Layer	Material	Intrinsic thickness (% X_0)	Intrinsic resolution (μm)	Barrel layers		Forward discs		
				Length ($\pm z$) (cm)	Radius (r) (cm)	Position ($ z $) (cm)	R_{in} (cm)	R_{out} (cm)
0		0.1	2.5	50	0.50	26	0.50	3
1		0.1	2.5	50	1.20	30	0.50	3
2		0.1	2.5	50	2.50	34	0.50	3
3	1		10	124	3.75	77	5	35
4	1		10	124	7	100	5	35
5	1		10	124	12	122	5	35
6	1		10	124	20	150	5	80
7	1		10	124	30	180	5	80
8	1		10	264	45	220	5	80
9	1		10	264	60	279	5	80
10	1		10	264	80	340	5	80
11	1					400	5	80

- 飛跡と衝突点同定のためのシリコンピクセル検出器
- 出来るだけ衝突点近傍に置きたい。
- 高精細なシリコンピクセル検出器が必要

シリコン半導体検出器

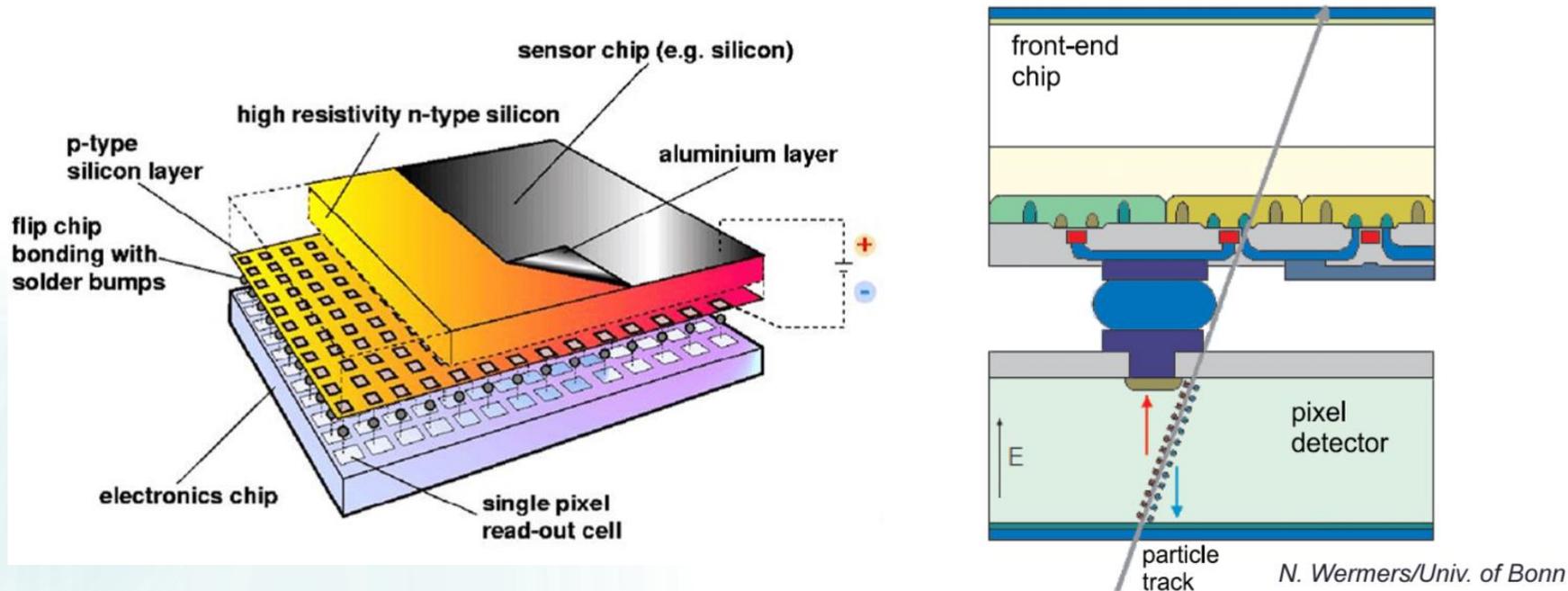
6



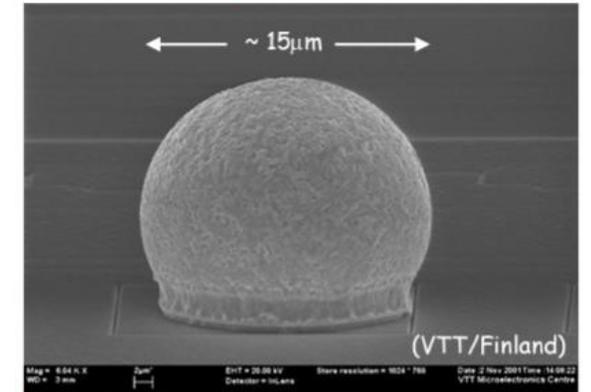
- ▶ pn 接合に逆バイアス電圧を印加すると空乏層ができる
- ▶ 荷電粒子が空乏層領域を通過すると飛跡に沿って 電子・ホール対を生成する
- ▶ 300 μm 厚センサー ~32,000 e-h ペア生成
- ▶ 電子とホールは電場に従って収集される
- ▶ 電荷を収集する電極を工夫すれば、一次元（ストリップ）、二次元（ピクセル）の位置情報を得ることができる

Hybrid ピクセルセンサー

現在の主流はハイブリッド型ピクセル検出器（ATLAS 実験など）

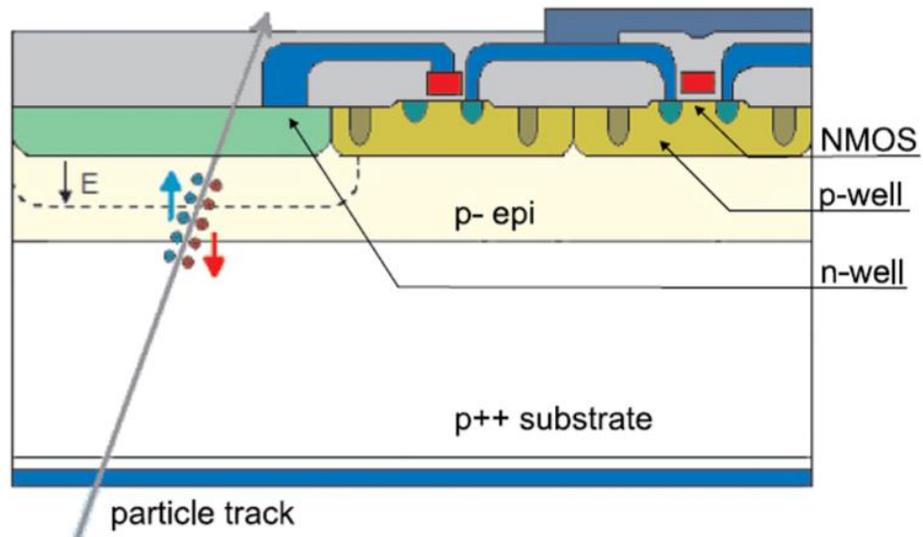


Solder Bump: Pb-Sn



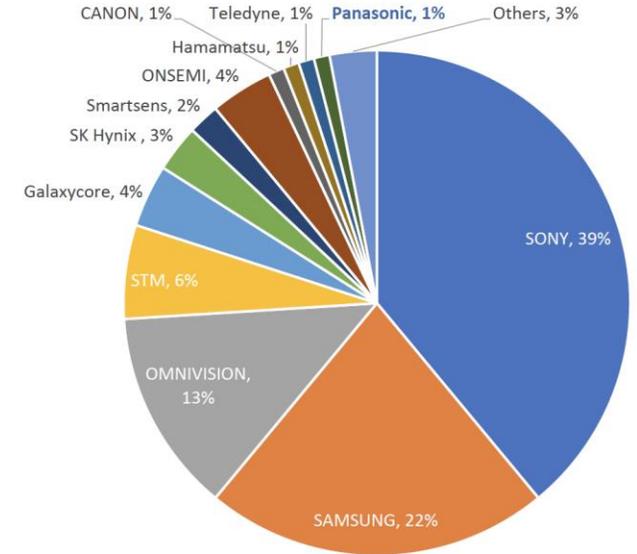
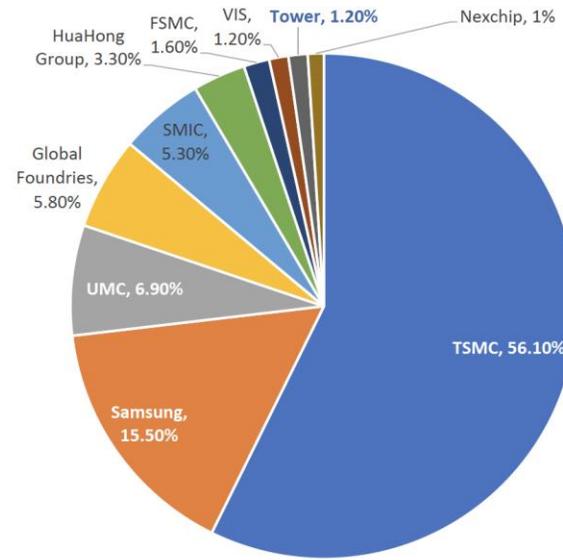
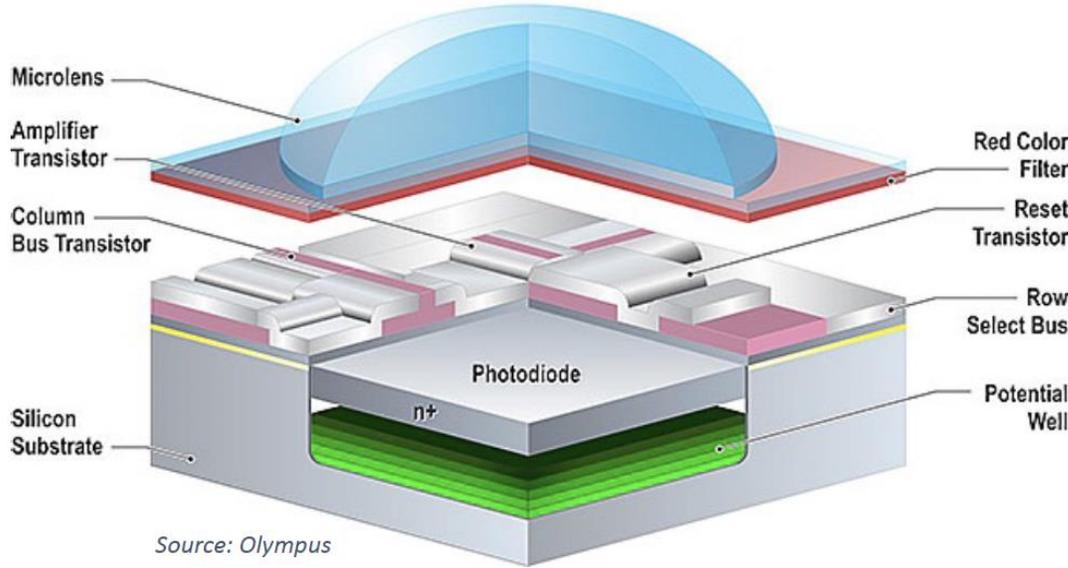
- ▶ センサーと信号読み出し回路を別々に作り、 bumps ボンディングにより接合する。
- ▶ bumps の大きさは数十 μ m 程度 → 最小のピクセルサイズは50 μ m程度

モノリシック ピクセルセンサー

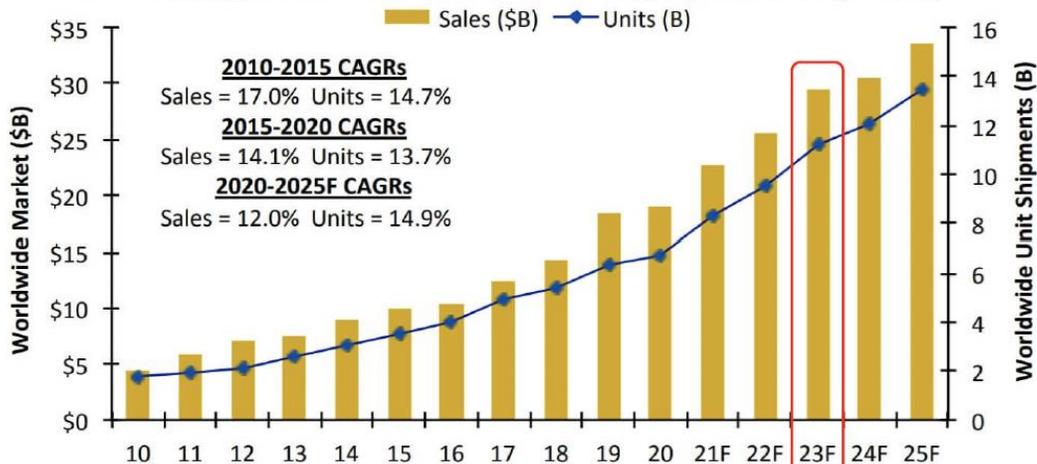


- ▶ 一枚のSiウェハーで、センサー部も読み出し回路も作ってしまう。
- ▶ バンプボンディングが不要なのでピクセルサイズを小さくできる
- ▶ しかし、ピクセル部の信号処理回路規模とトレードオフ。
- ▶ 簡単なアナログ回路だけならトランジスタ数個 ~ 10 個程度で実現可能。高度な信号処理回路（アナログとデジタルとか）を入れようとするとトランジスタ数は増える。

CMOS imaging sensor (CIS)



CMOS Image Sensors Return to Strong Upward Trajectory



Global Top 10 CMOS Foundries - Market Share

Global Top 10 CIS Companies - Market Share

- camera phones, vehicles, machine vision, human recognition and security, scientific/medical
- cellular camera phones account for 60% of the sales

CMOS imaging sensors

The inception of CMOS APS for charged particles



ELSEVIER

Nuclear Instruments and Methods in Physics Research A 458 (2001) 677–689

NUCLEAR
INSTRUMENTS
& METHODS
IN PHYSICS
RESEARCH
Section A

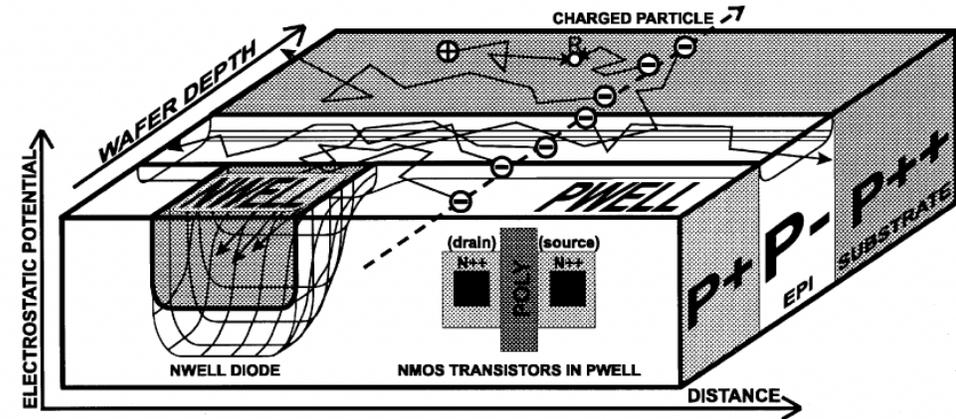
www.elsevier.nl/locate/nima

A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology

R. Turchetta^{a,*}, J.D. Berst^a, B. Casadei^a, G. Claus^a, C. Colledani^a, W. Dulinski^a, Y. Hu^a, D. Husson^a, J.P. Le Normand^a, J.L. Riester^a, G. Deptuch^{b,1}, U. Goerlach^b, S. Higuere^b, M. Winter^b

^aLEPSI, IN2P3/ULP, 23 rue du Loess, BP20, F-67037 Strasbourg, France

^bIReS, IN2P3/ULP, 23 rue du Loess, BP20, F-67037 Strasbourg, France



Since then, there have been a lot of developments. 100% efficiency and CMOS electronics integrated in the pixel matrix

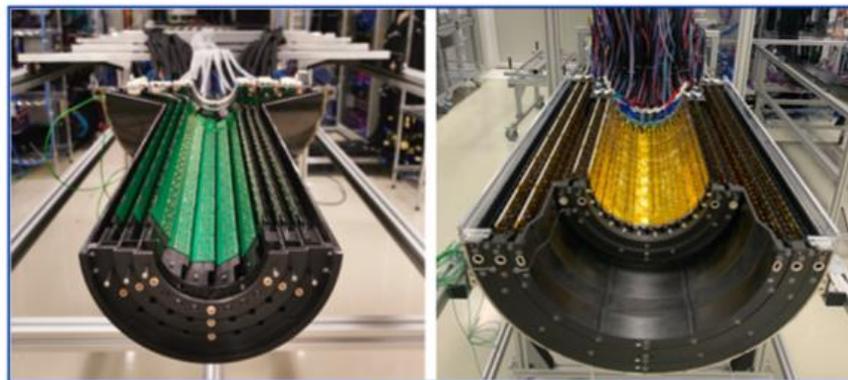
TPAC - for ILC ECAL (CALICE)	PIMMS – for TOF mass spectroscopy	CHERWELL – Calorimetry/Tracking	ALPIDE – Tracking
50µm pixel 2008	70µm pixel 2012	48 µm x 96 µm pixel 2013	27 µm x 29 µm pixel 2016

MAPSセンサーの大型実験応用

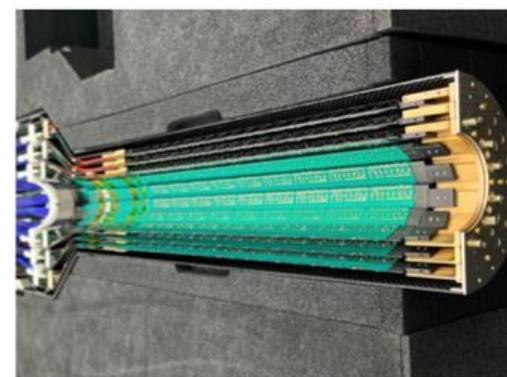
L. Musa, QM2023



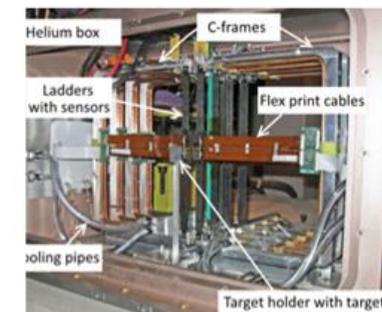
STAR HFT – 2014
ULTIMATE



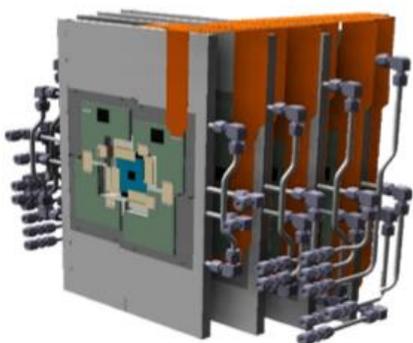
ALICE ITS2 – 2021
ALPIDE



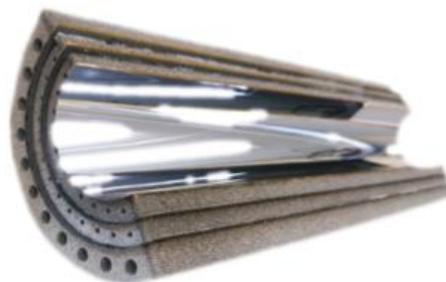
SPHENIX MVTX - 2023
ALPIDE



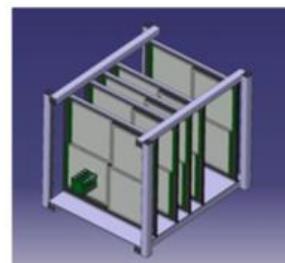
NA61 prototype
ALPIDE



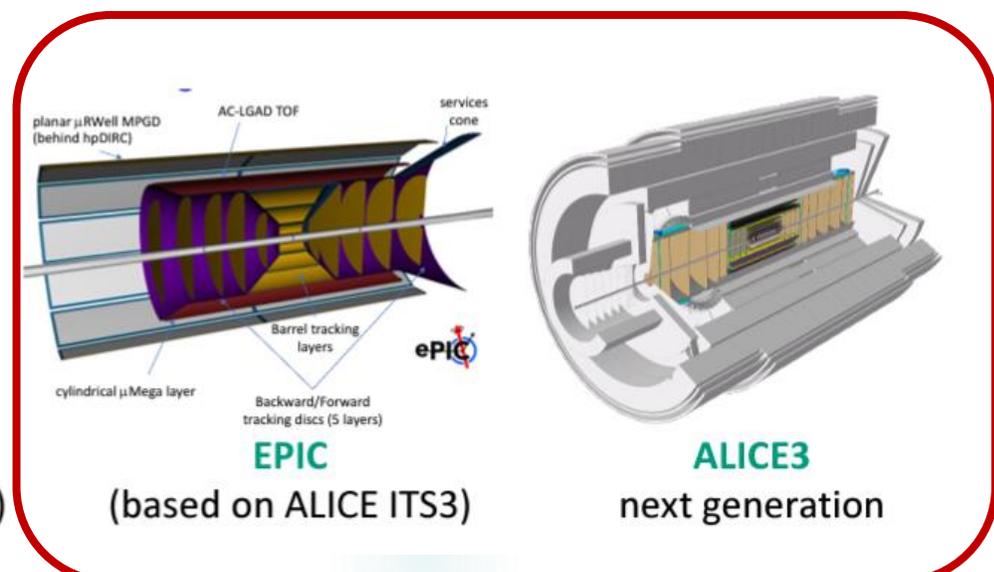
CBM MVTX – 2027
MIMOSIS



ALICE ITS3 – 2028
"Wafer-scale MOS"



NA60+ - 2028
(based on ALICE ITS3)



EPIC
(based on ALICE ITS3)

ALICE3
next generation

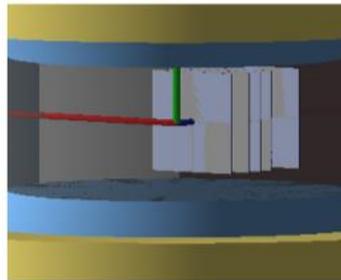
Beam energy scan ($\sqrt{s_{NN}}$: 6.3 – 17.3 GeV) for precision studies of: hard processes, electromagnetic

Roadmap

- Technical proposal: **2024-2025**
- Constr. & Installation: **2026-2028**
- Data taking: **2029 - 2037**

EoI in 2019 <https://cds.cern.ch/record/2673280>

Lol in 2022 [CERN-SPSC-2022-036](#) ; [SPSC-I-259](#)

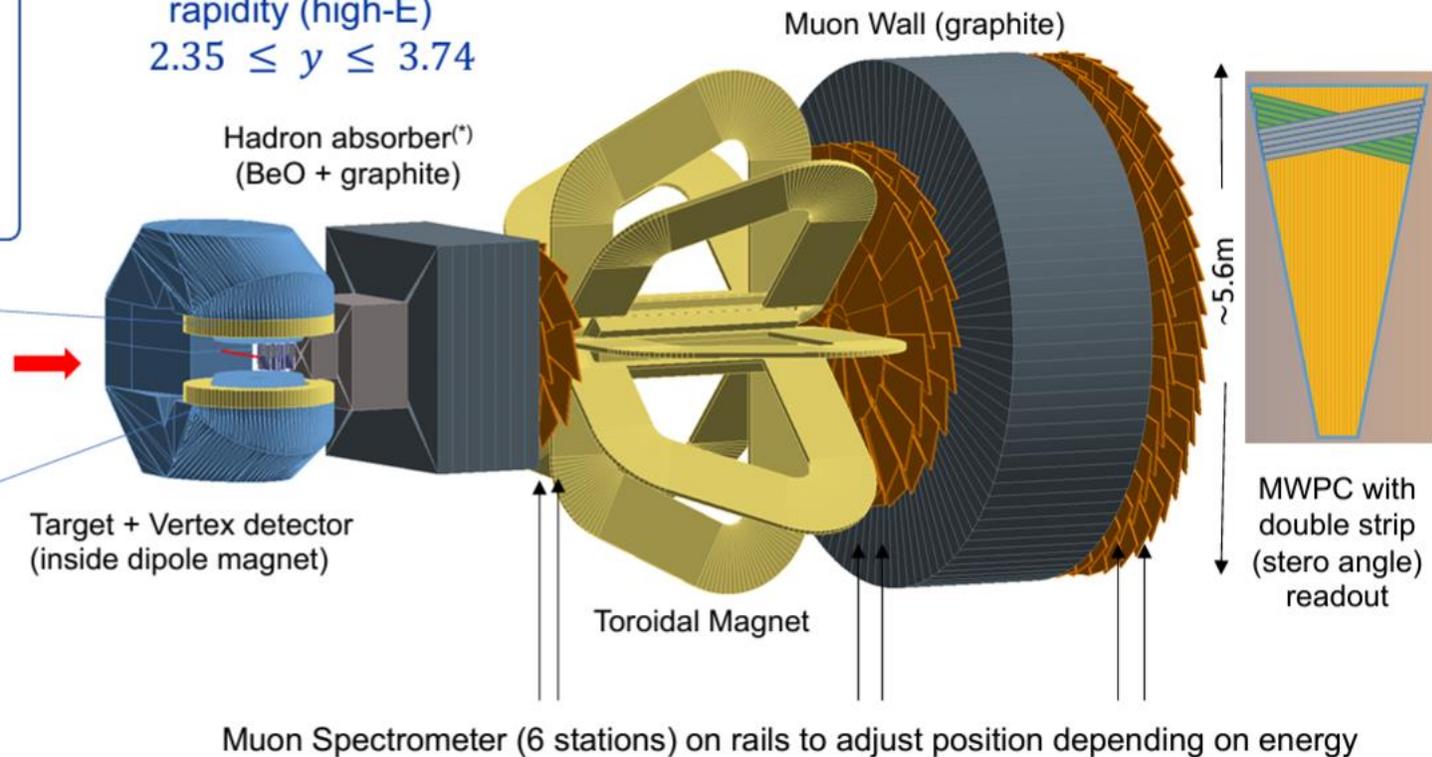


5-plane vertex detector based on MAPS (ALICE ITS3)

- Spatial resolution: $5\mu\text{m}$
- X/X_0 : 0.1% /plane

follows design of NA60 but with better-performing detectors

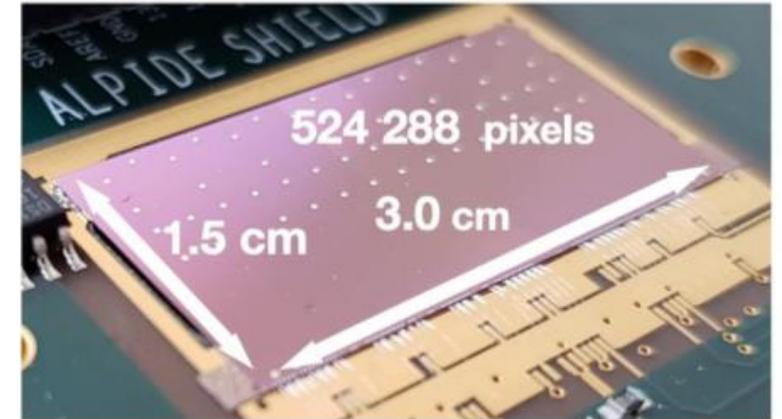
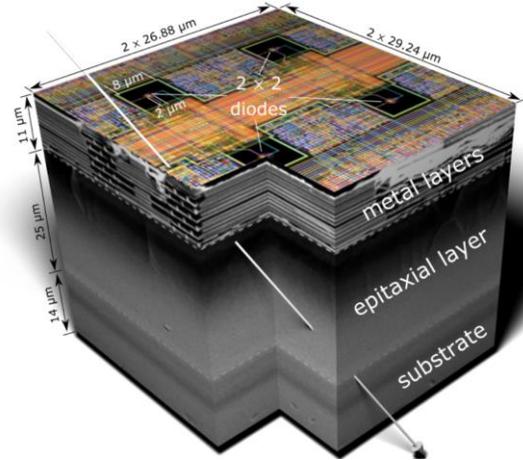
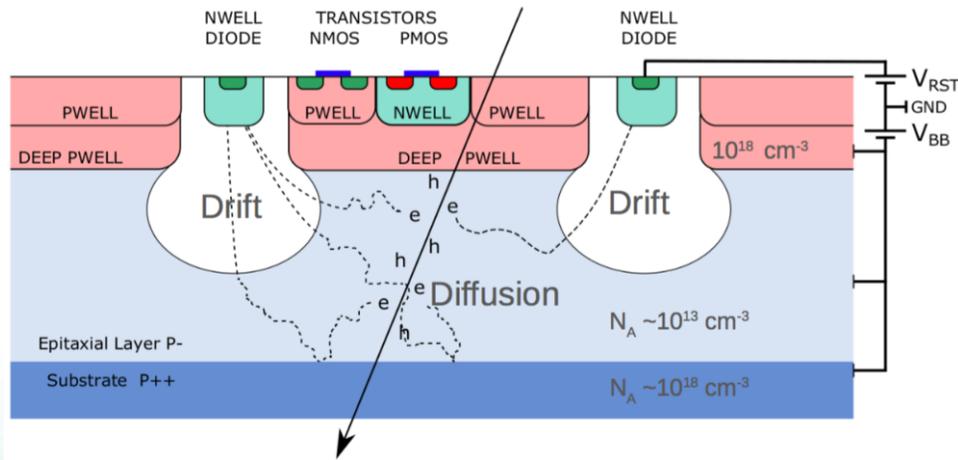
rapidity (high-E)
 $2.35 \leq y \leq 3.74$



Muon tracking stations: **MPGD** (GEM, MicroMeegas) or **MWPC** (baseline) with total active area 100m^2 , spatial resolution (radial direction) $\sim 200\mu\text{m}$, max particle flux $\sim \text{kHz}/\text{cm}^2$

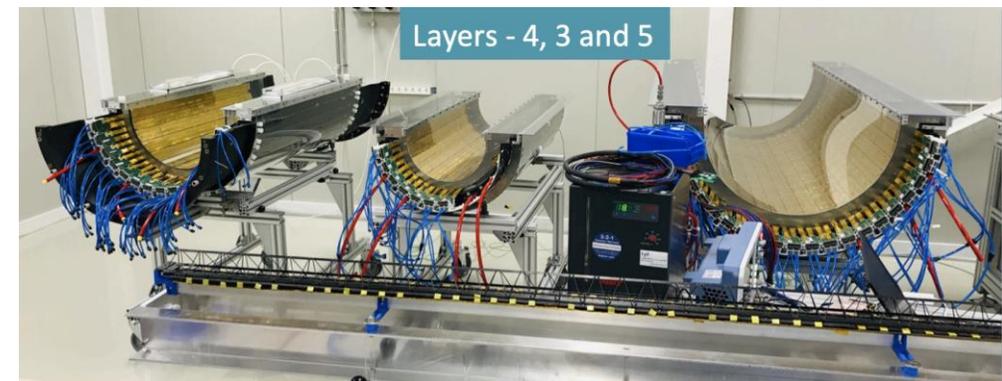
ALPIDEチップ (ALICE-ITS2)

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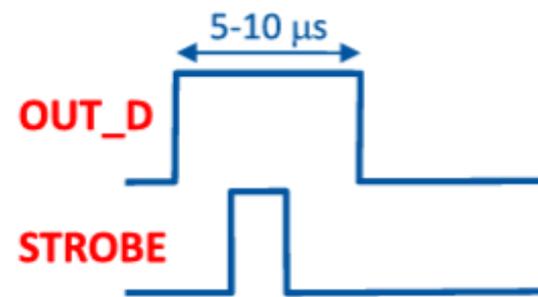
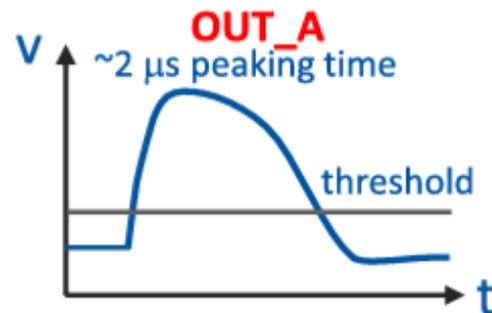
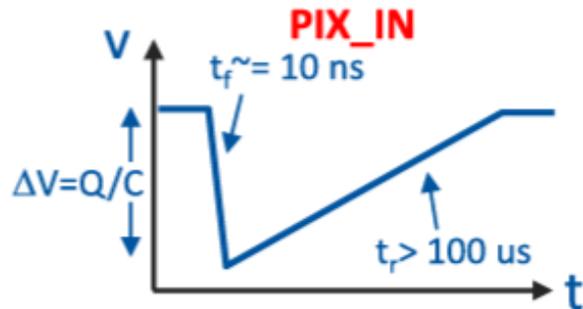
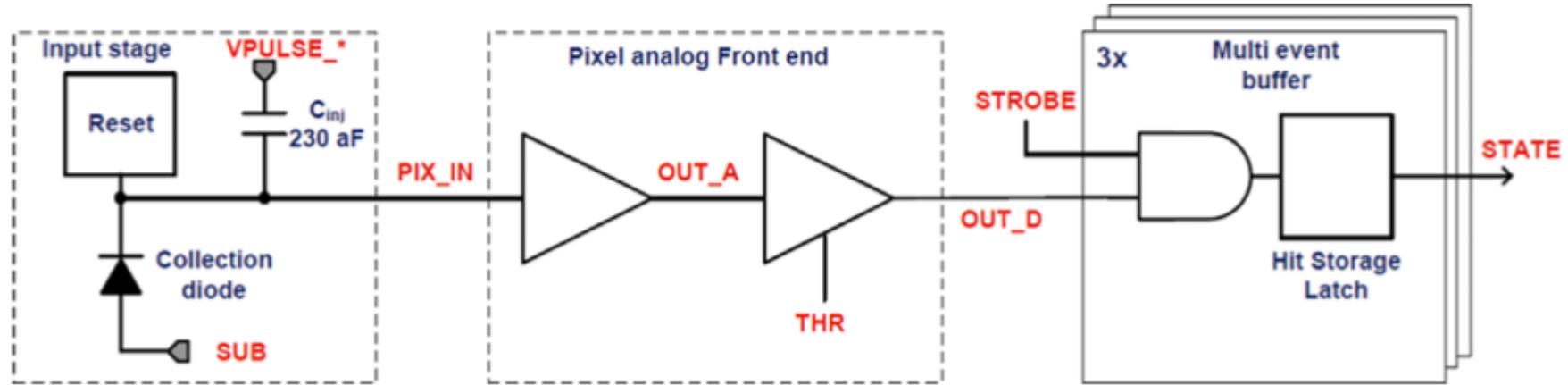


Based on MAPS technology (ALPIDE)

- ▶ 180nm technology (Tower Jazz)
- ▶ Thinner: for innermost layers $\sim 0.30\% X_0$
- ▶ Smaller pixels: $27 \times 29 \mu\text{m}^2$
- ▶ **Maximum readout rate: 200 kHz**
- ▶ 130 000 pixels/ cm^2
- ▶ Max. particle rate: $\sim 100 \text{ MHz}/\text{cm}^2$
- ▶ Spatial resolution: $\sim 5 \mu\text{m}$
- ▶ Thickness: $50 \mu\text{m}$ for the inner layers
- ▶ Fake-hit rate: $< 10^{-9}$ per pixel per event



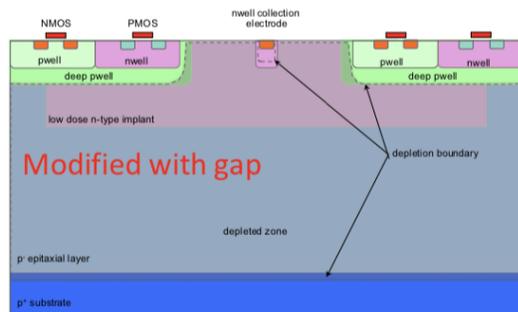
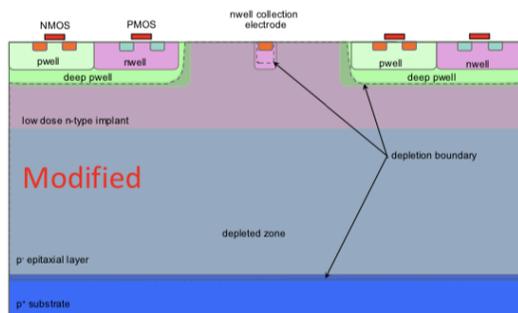
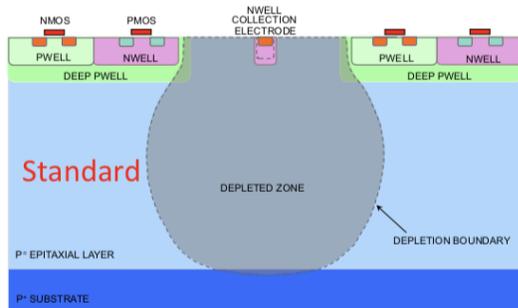
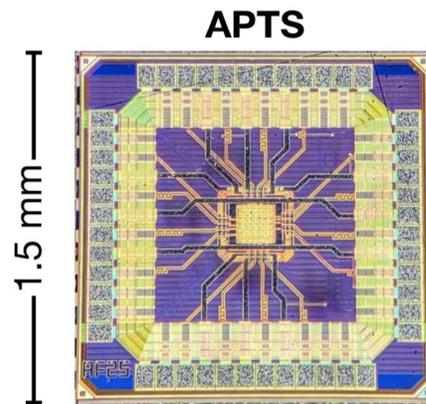
ALPIDEチップ (ALICE-ITS2)



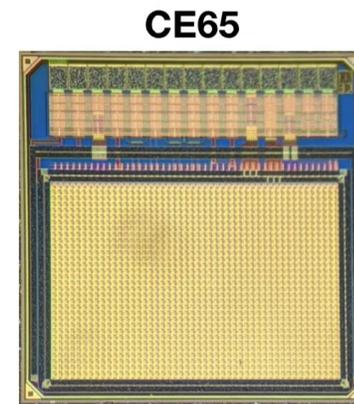
ePIC/ALICE-ITS3 : 65nm

180 nm → 65 nm technology development

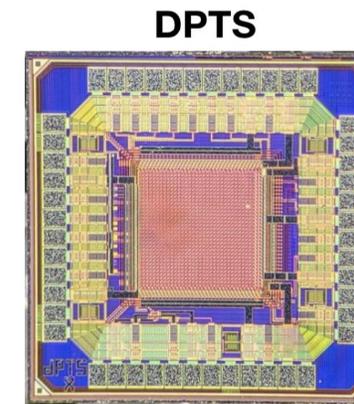
TPSCo 65 nm CMOS Imaging Technology

- ▶ **matrix:** 6x6 pixels
- ▶ **readout:** direct analog readout of central 4x4
- ▶ **pitch:** 10, 15, 20, 25 μm
- ▶ **total:** 34 dies



- ▶ **matrix:** 64x32, 48x32 pixels
- ▶ **readout:** rolling shutter analog
- ▶ **pitch:** 15, 25 μm
- ▶ **total:** 4 dies

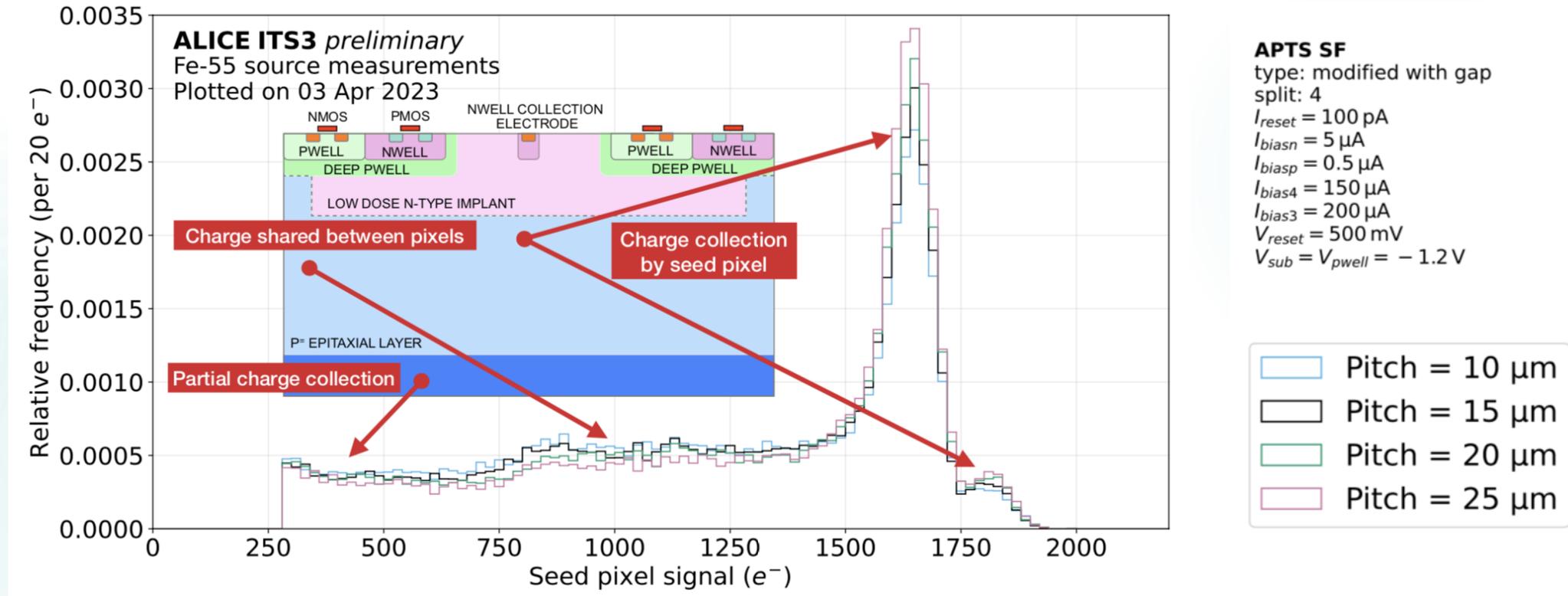


- ▶ **matrix:** 32x32 pixels
- ▶ **readout:** async. digital with ToT
- ▶ **pitch:** 15 μm
- ▶ **total:** 3 dies

ePIC/ALICE-ITS3 : 65nm

APTS – Fe-55 lab tests

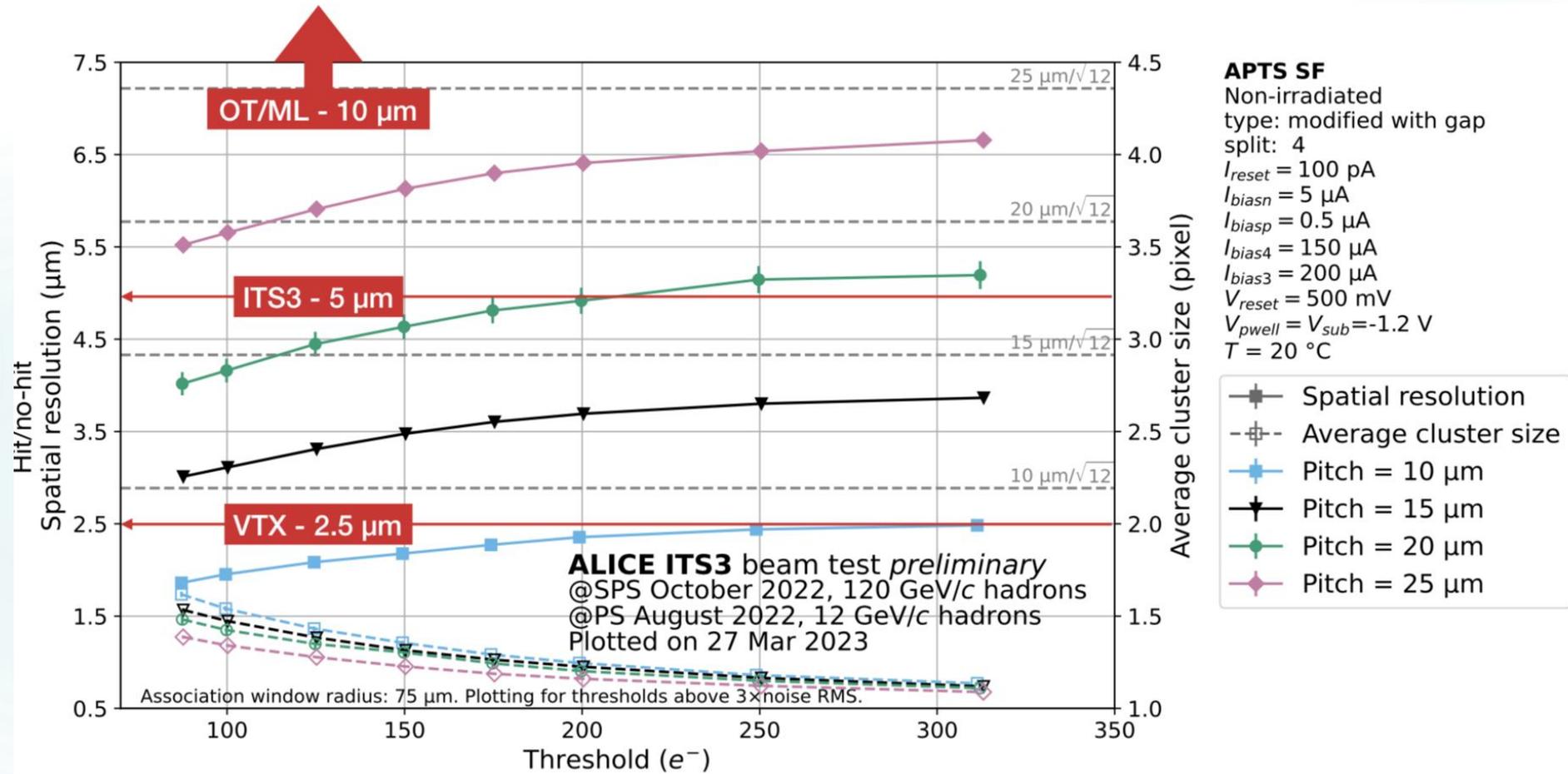
Modified with gap



Pixels of pitches of 10-25 μm show similar results indicates that the charge collection is very efficient

ePIC/ALICE-ITS3 : 65nm

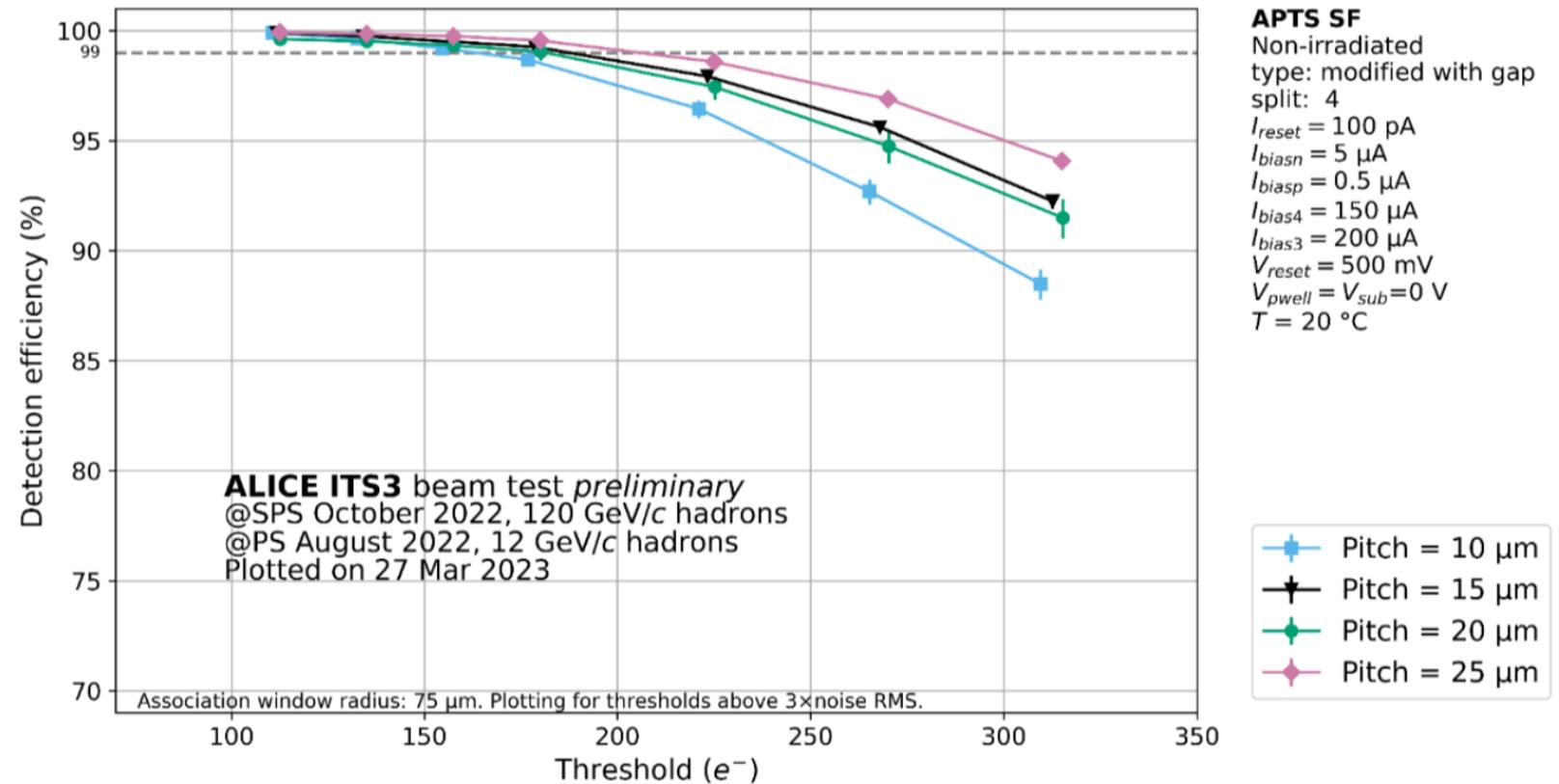
APTS – beam tests



ePIC/ALICE-ITS3 : 65nm

APTS – beam tests

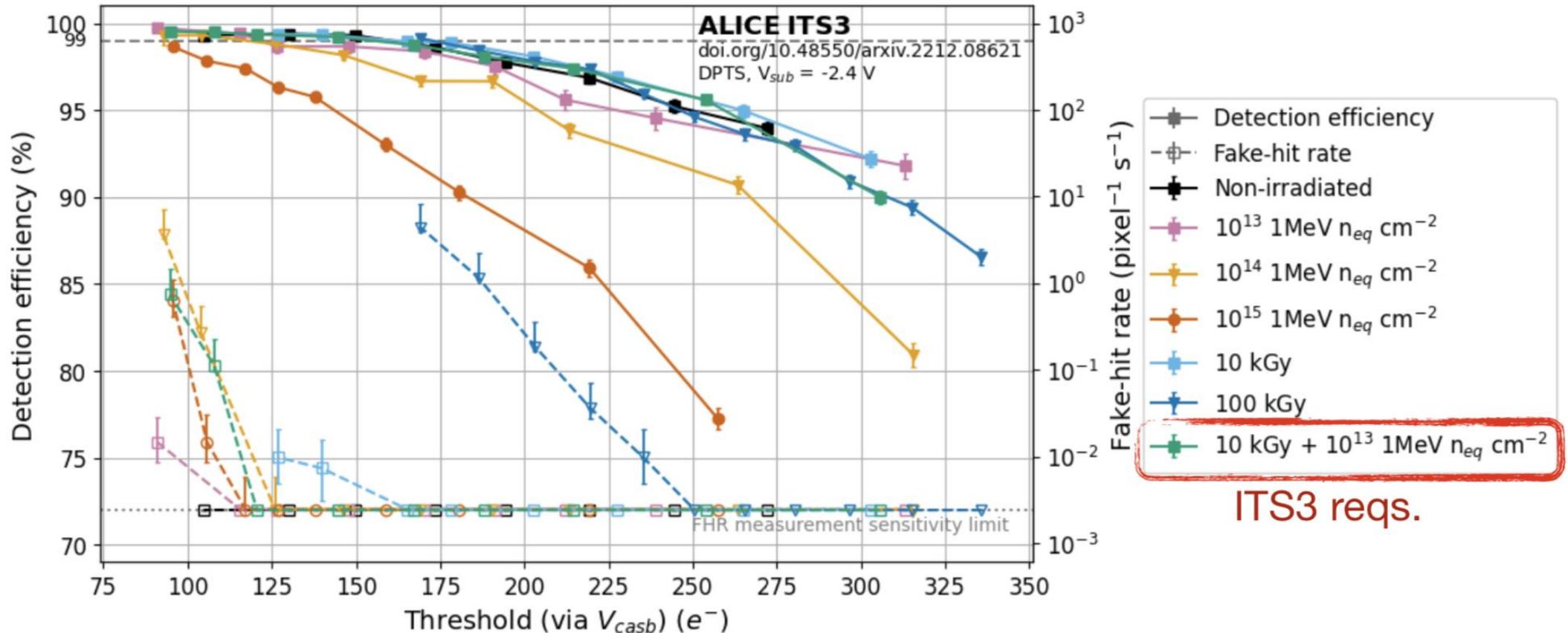
- Detection efficiency increases with pixel pitch
- Interplay between:
 - Less efficiency at pixel border
 - Less border contribution for larger pixels



ePIC/ALICE-ITS3 : 65nm

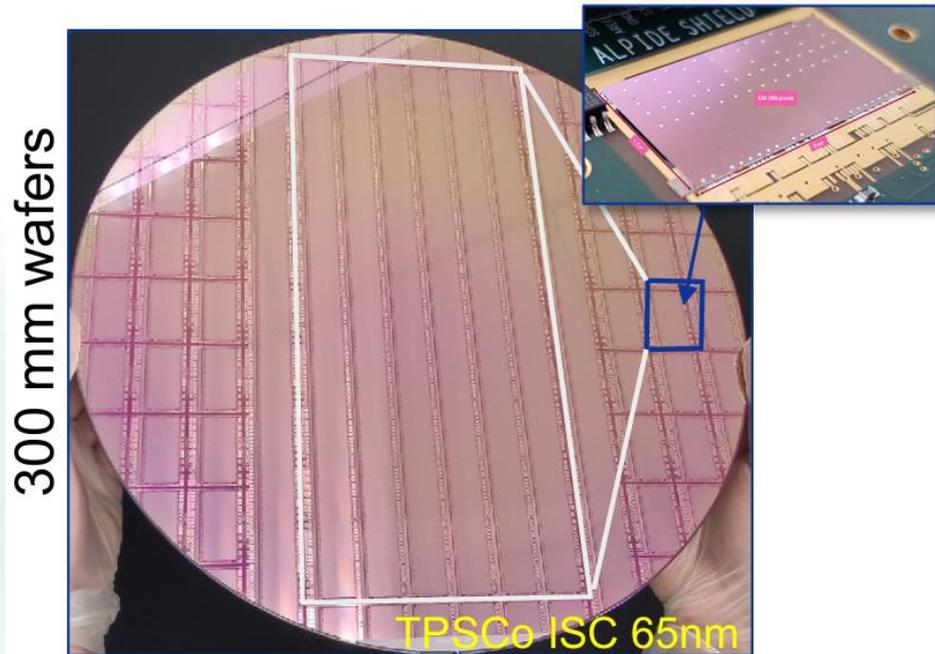
DPTS – Detection efficiency

[doi:10.48550/arXiv.2212.08621]



ePIC/ITS3: Wafer-size sensor

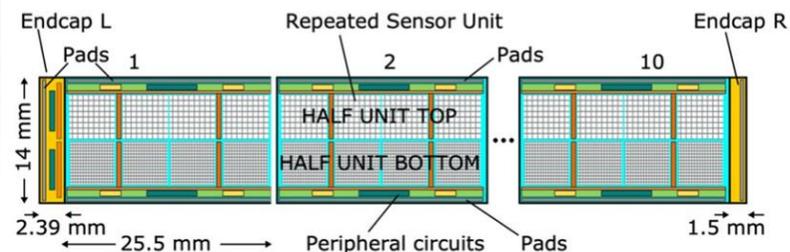
Wafer-size curved sensors → Nearly massless truly cylindrical detectors
TPSCo ISC 65nm CMOS Imaging 300mm wafers + stitching



from reticle-size to wafer-size



thin (<math><50\mu\text{m}</math> CMOS can be curled)

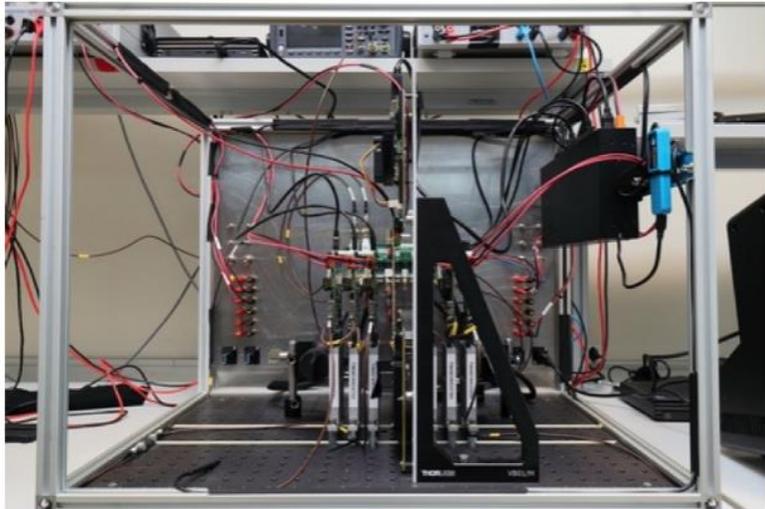


“**MOSS**”: 14 x 259 mm, 6.72 MPixel
(22.5 x 22.5 and 18 x 18 μm^2)

- conservative design, different pitches

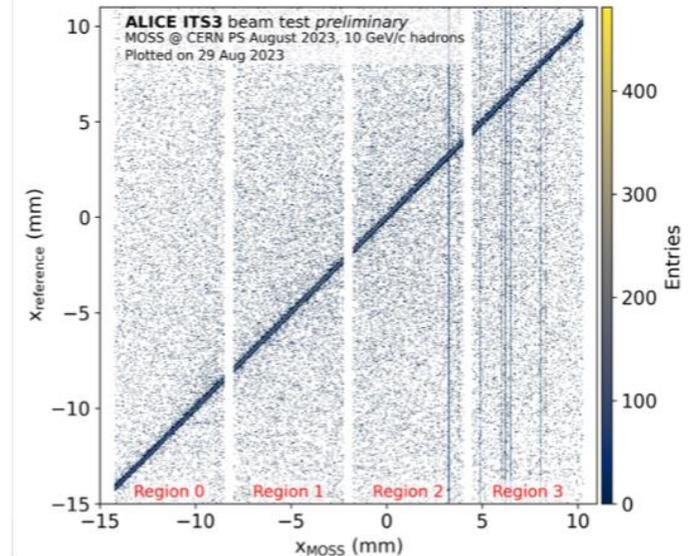
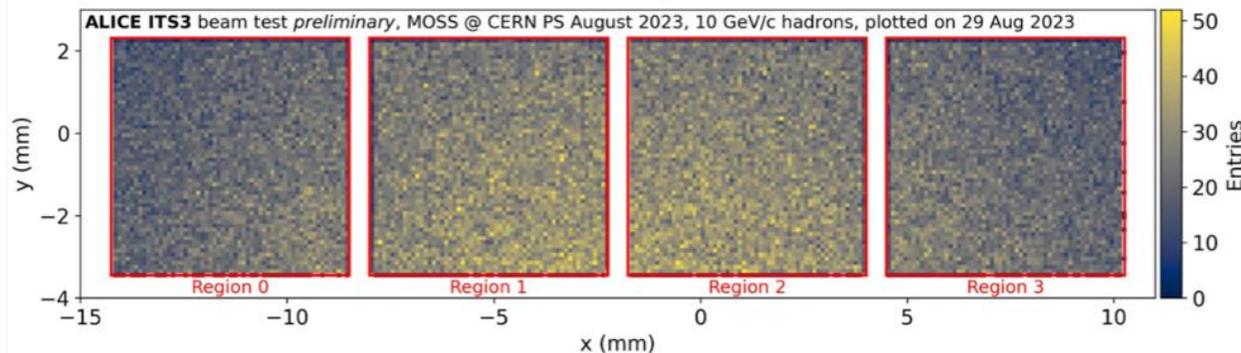
ePIC/ITS3: MOSS testing

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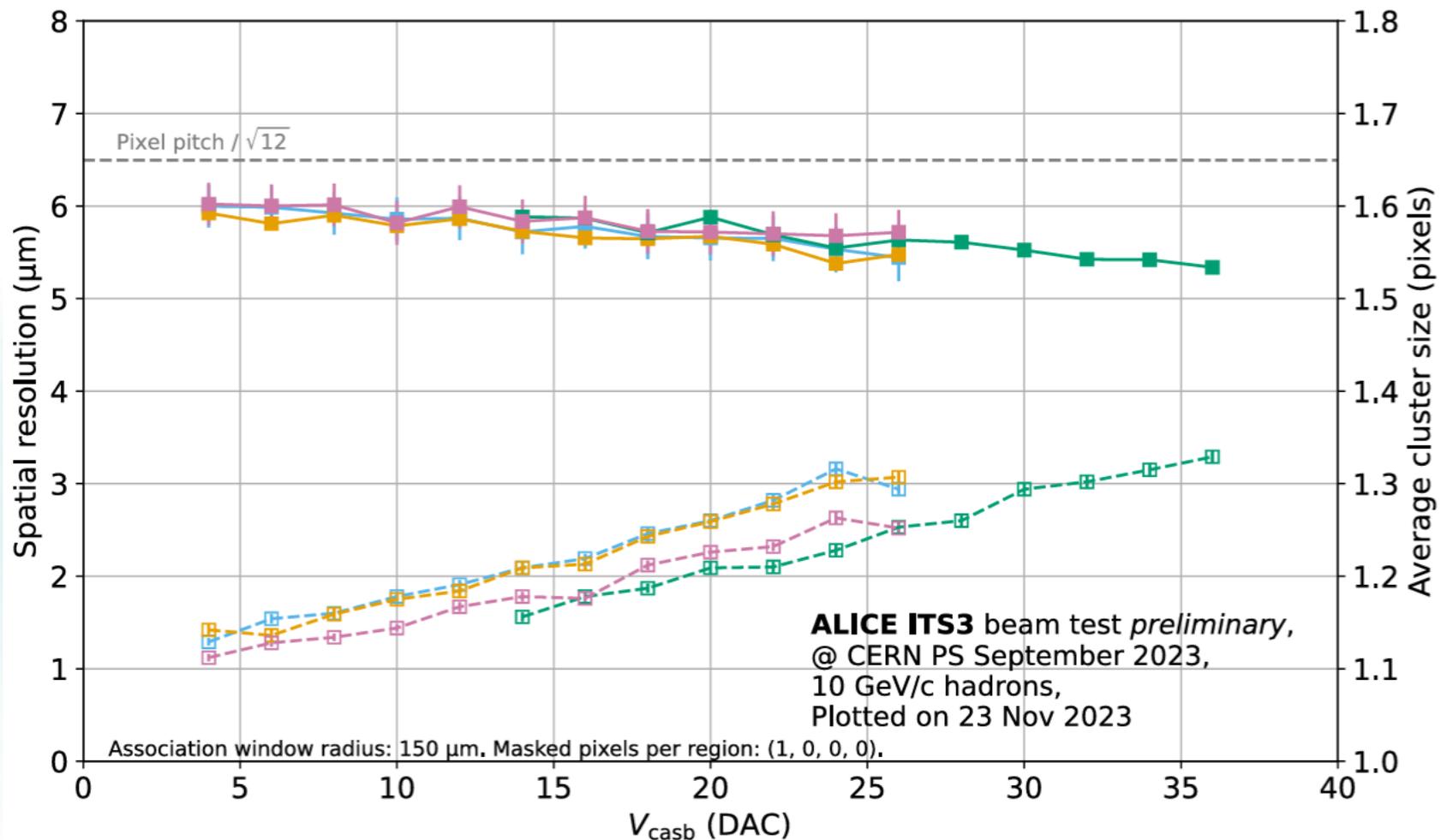
- Confirmed basic functionalities at lab
 - ✓ Careful and gentle powering
 - ✓ Yield assessment by baby MOSS too
- 3 beam test campaigns at PS
 - ✓ 3 ALPIDEs + MOSS + 3 ALPIDEs

Hit map



ePIC/ITS3: MOSS testing

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MOSS-4_W24B5_T6

Pitch: 22.5 μm
Type: 5 μm gap
 $I_{bias} = 62$ DAC
 $I_{biasn} = 100$ DAC
 $I_{reset} = 10$ DAC
 $I_{db} = 50$ DAC
 $V_{shift} = 192$ DAC
 $V_{casn} = 64$ DAC
 $V_{psub} = 0$ V (via 0 Ω)
Strobe length: 6 μs
 $T = 30^\circ\text{C}$

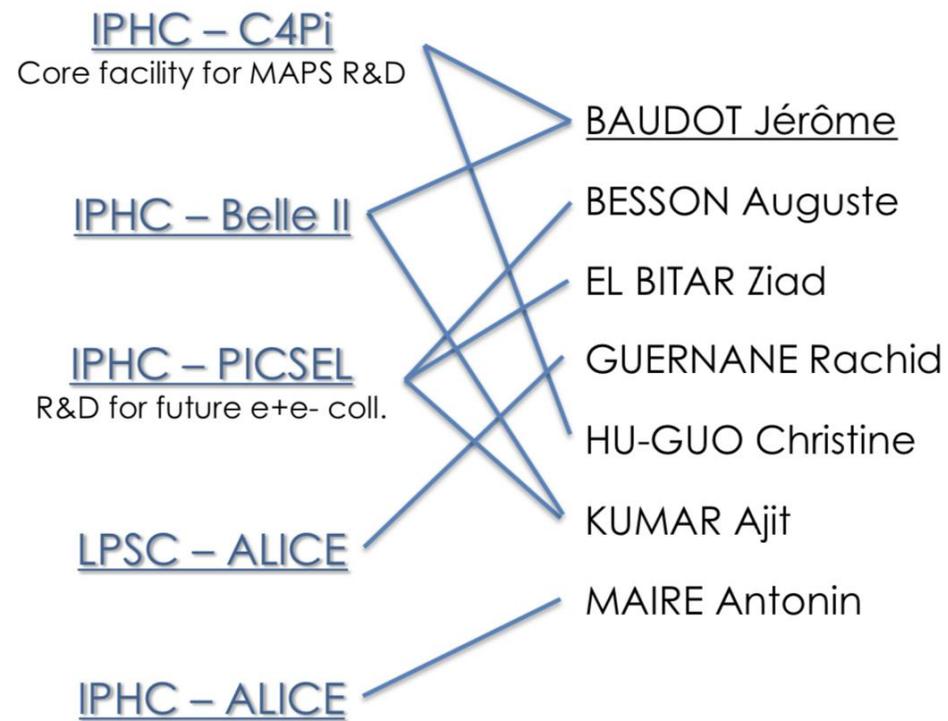
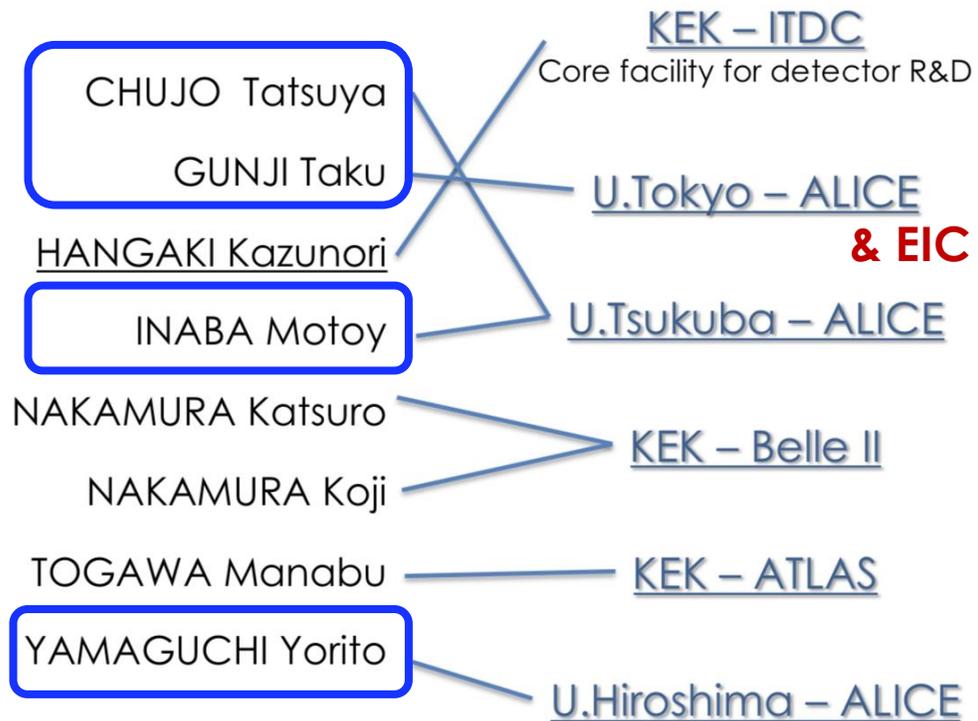
- Spatial resolution
- Average cluster size
- Region 0
- Region 1
- Region 2
- Region 3

ALICE ITS3 beam test *preliminary*,
@ CERN PS September 2023,
10 GeV/c hadrons,
Plotted on 23 Nov 2023

Association window radius: 150 μm . Masked pixels per region: (1, 0, 0, 0).

日本グループの活動

R_DR_29 Collaboration

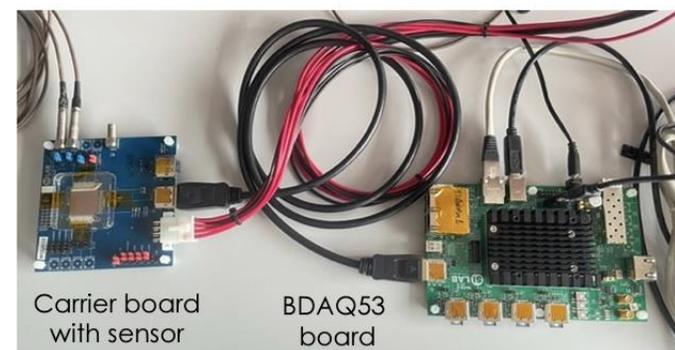


Short-term activities



- Contribution to OBELIX-1 design
 - Still possibilities in analogue parts: DAC, ADC
- Tests of TJ-Monopix2
 - Same DAQBoard53 system than OBELIX-1 will use
 - IPHC can provide its own system for Summer (more systems to be produced soon)
 - **Goals: learn how to tune the thresholds over the matrix start thinking integration in beam line (telescope?)**
 - Reporting on VTX Monday meeting 9:00 PM (JST)

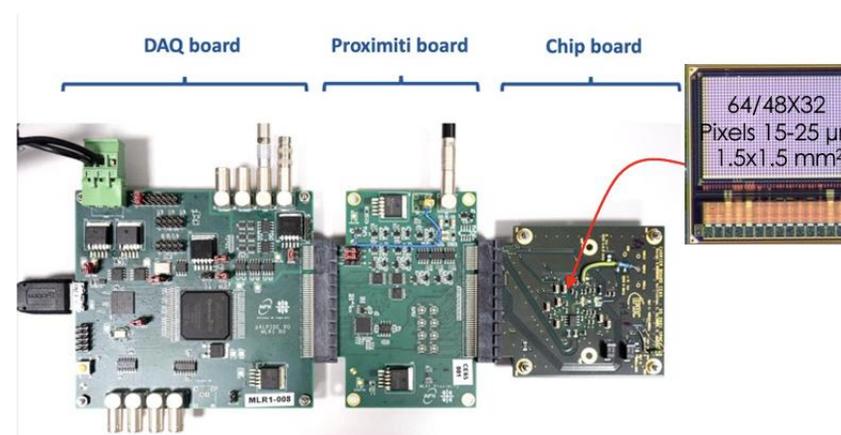
- Tests of CE-65v1 or v2
 - System distributed by ALICE-ITS3 (availability to be checked)
 - **Goals: learn analogue output characterisation (calib...) specific measurements on v2 not yet performed**
 - Reporting in ALICE-WP3 Tuesday meeting 4:00 PM (JST)
 - **MOSS characterization**
 - **Allpix2 simulation**



Carrier board with sensor

BDAQ53 board

=> PC



DAQ board

Proximiti board

Chip board

64/48X32
Pixels 15-25 μm
1.5x1.5 mm²

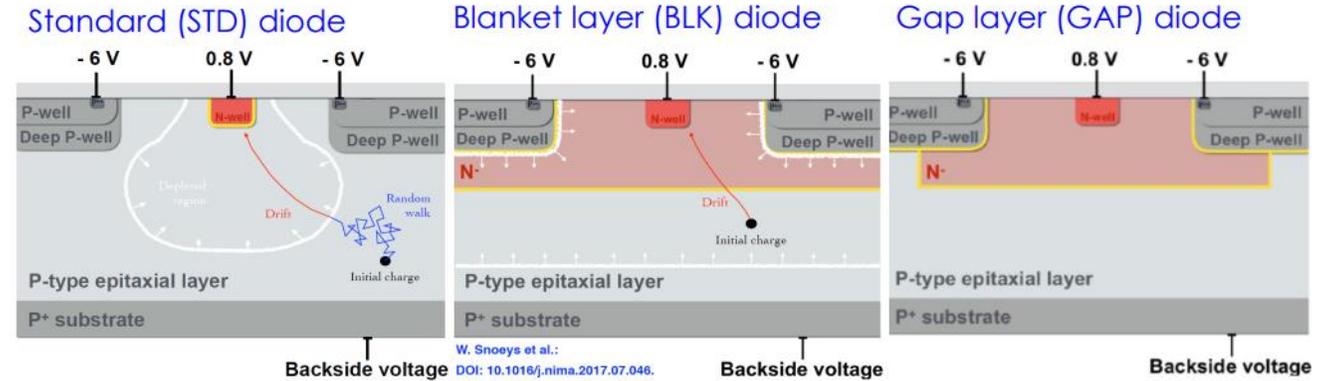
CE65 variants

Reference configuration

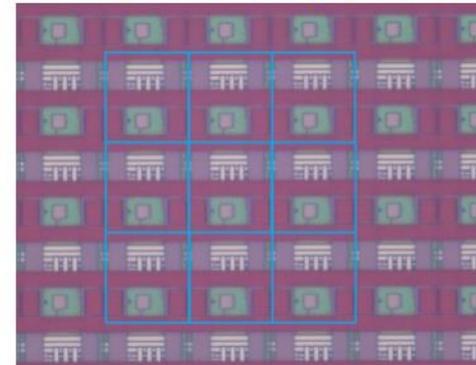
- 22.5 SQ GAP

Specific studies

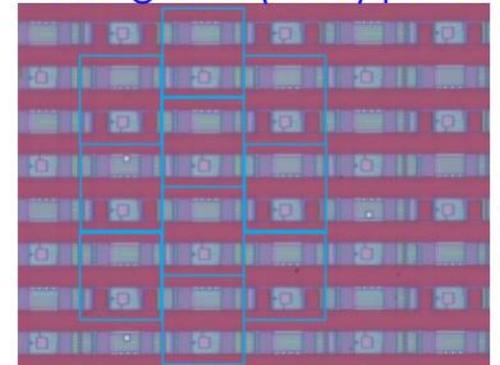
1. Influence of diode conf on baseline 22.5 SQ.
 - 22.5 SQ STD, 22.5 SQ BLK, 22.5 SQ GAP
2. Influence of pitch in SQ pixels in GAP.
 - 15 SQ GAP, 18 SQ GAP, 22.5 SQ GAP
3. Influence of HSQ vs SQ in GAP.
 - 18 SQ GAP, 18 HSQ GAP, 22.5 SQ GAP, 22.5 HSQ GAP
4. Influence of pitch in SQ pixels in STD.
 - 15 SQ STD, 18 SQ STD, 22.5 SQ STD
5. Influence of HSQ vs SQ in STD.
 - 18 SQ STD, 18 HSQ STD, 22.5 SQ STD, 22.5 HSQ STD
6. Influence of pitch in SQ pixels in BLK.
 - 15 SQ BLK, 18 SQ BLK, 22.5 SQ BLK
7. Influence of HSQ vs SQ in BLK.
 - 18 SQ BLK, 18 HSQ BLK, 22.5 SQ BLK, 22.5 HSQ BLK



Square (SQ) pixels

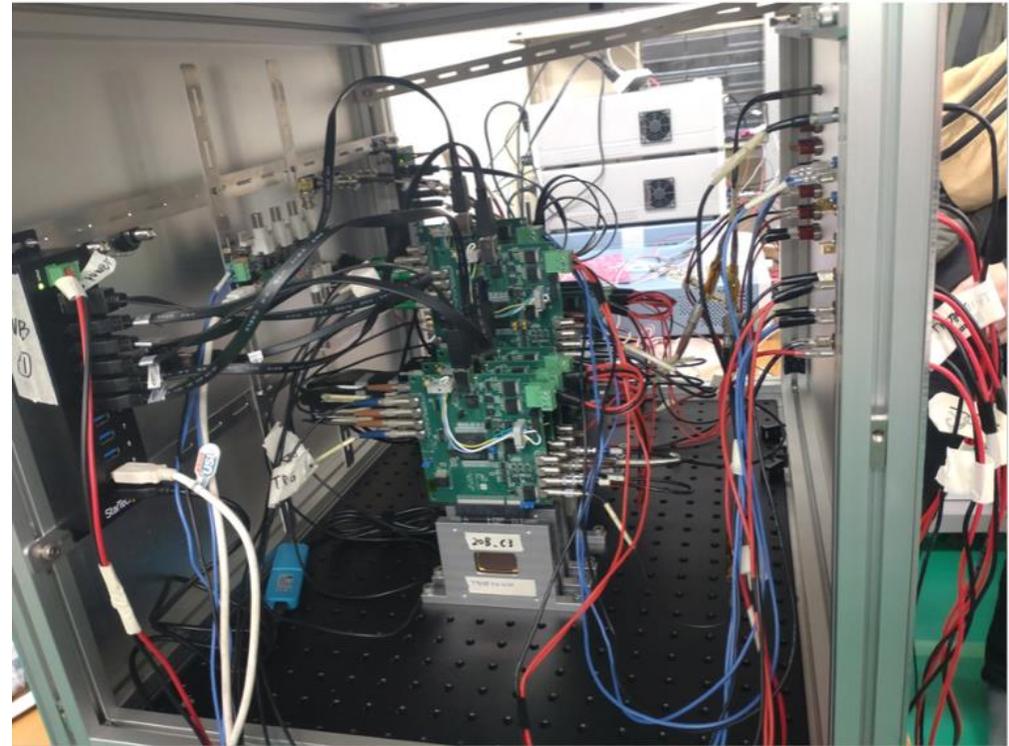
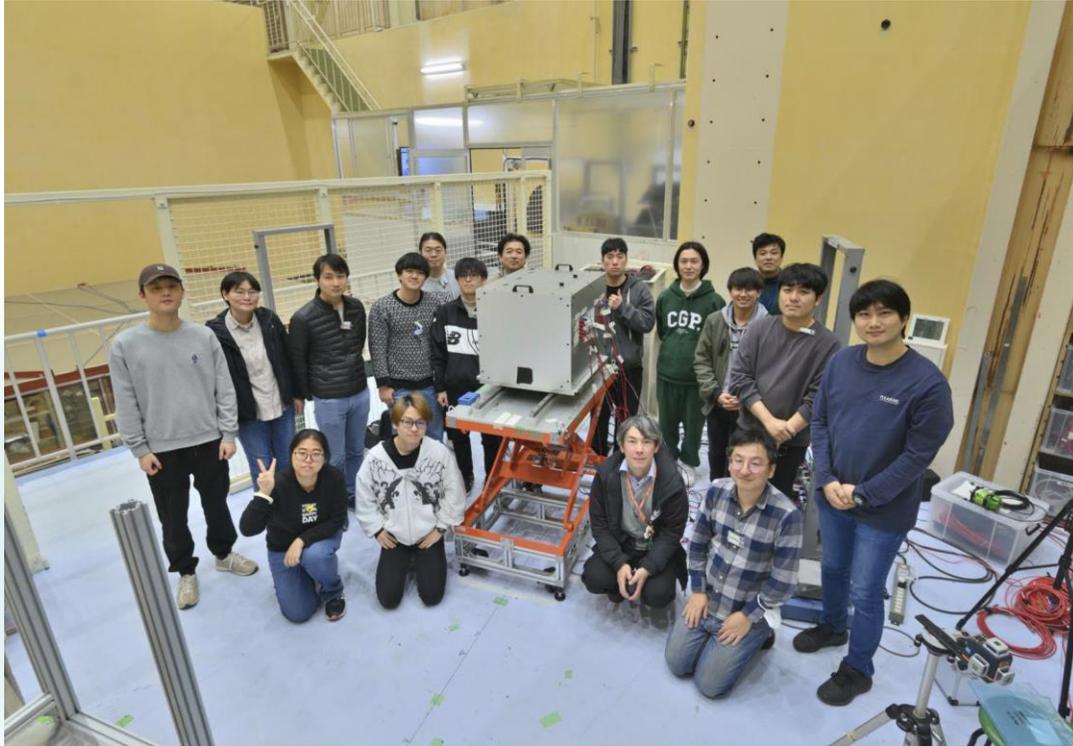


Hexagonal (HSQ) pixels



MAPS testbeam at KEK

26



**Beamtests for CE65 chip validation & performance check
Collaboration with ALICE-Korea team (ALPIDE telescope and APTS, Bent-ALPIDE)**

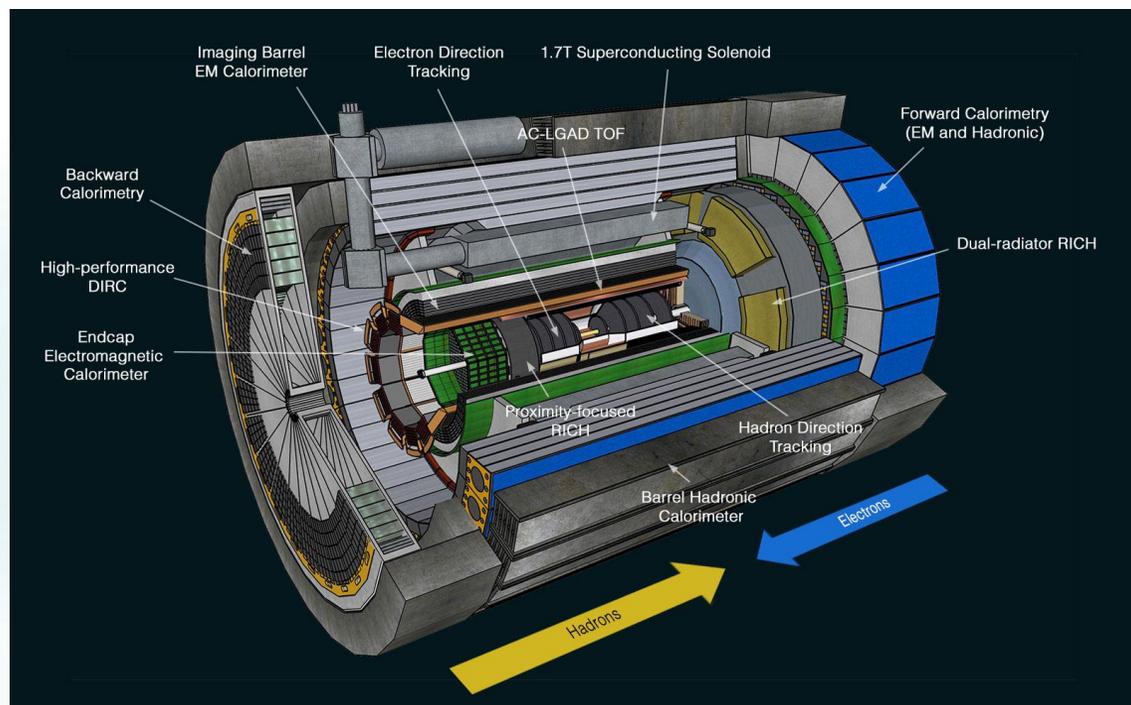
今後の目標

- ▶ ALICE3のouter trackerやePIC実験のVTXのupgrade (2040-)を狙う
- ▶ CE65、MOSS、APTSのテストを通じて、基本的な動作を理解
- ▶ TCAD, AllPix2などのsimulation studies
- ▶ **自分たちでデザインできるように技術を身につけたい**
 - ▶ ePIC VTXのupgrade
 - ▶ J-PARCのハドロン実験、E16 upgrade?
 - ▶ J-PARC-HI

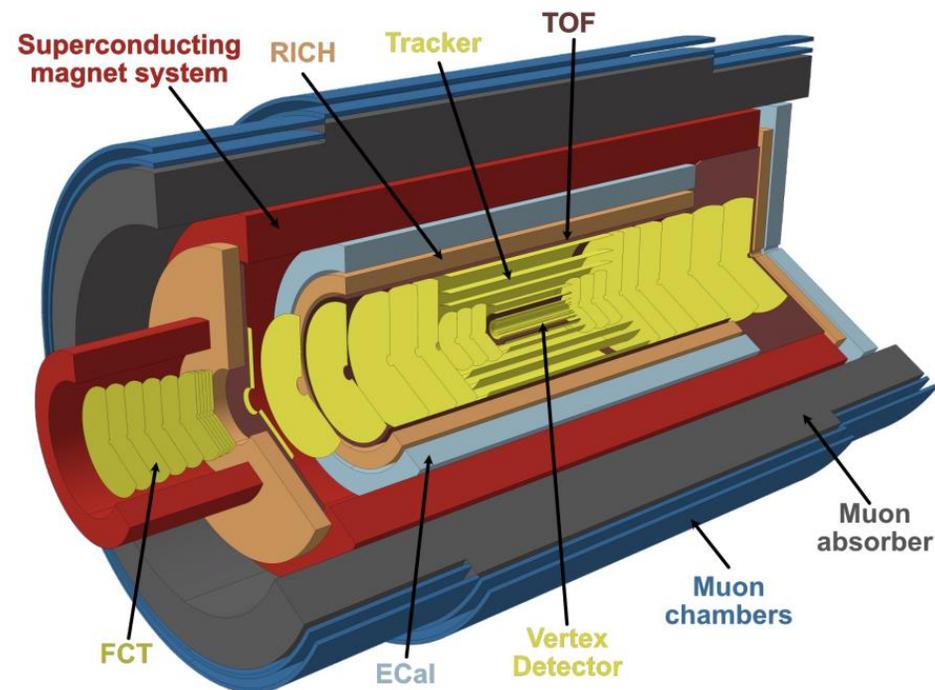
ePIC/ALICE3でのPID

28

▶ ePIC実験 (2030-)



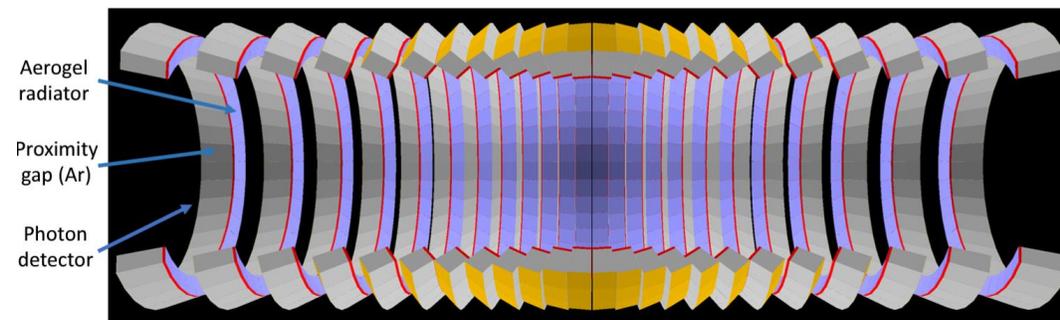
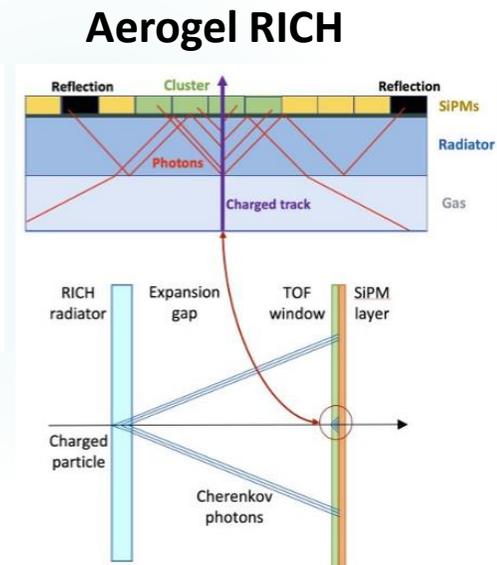
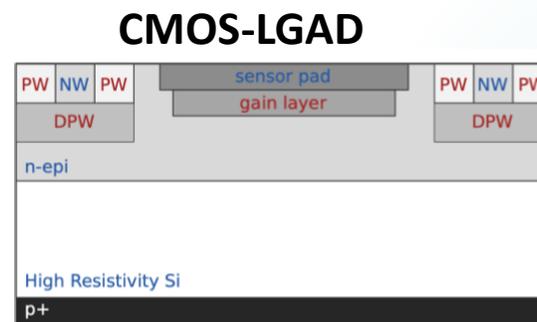
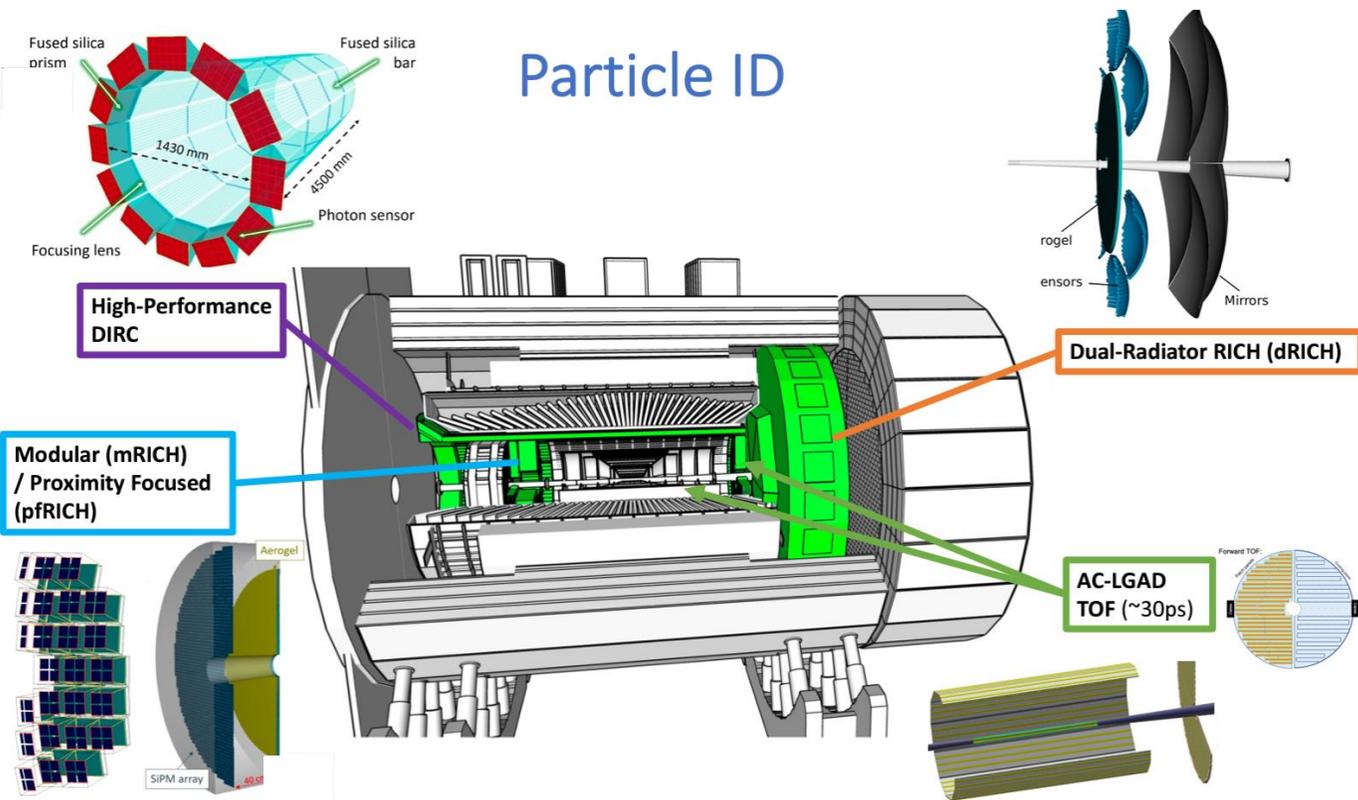
▶ ALICE3実験 (2035-)



ePIC/ALICE3でのPID

▶ ePIC実験 (2030-)

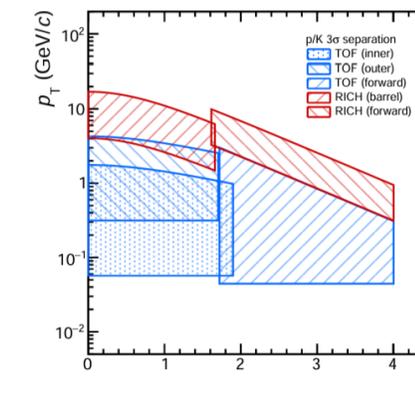
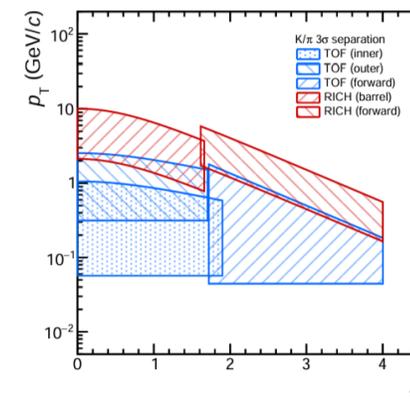
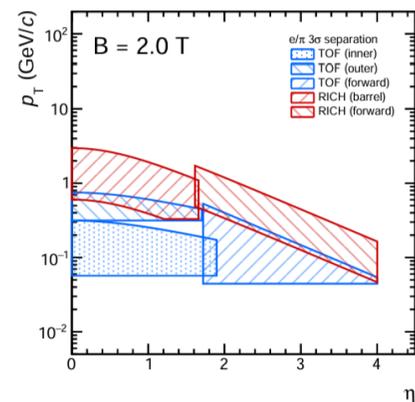
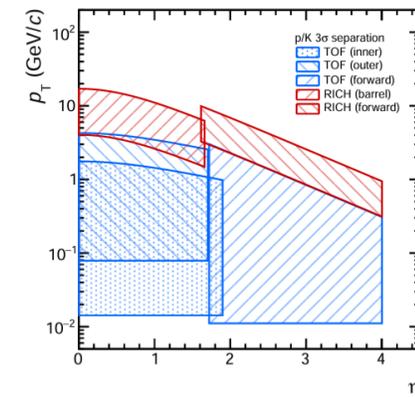
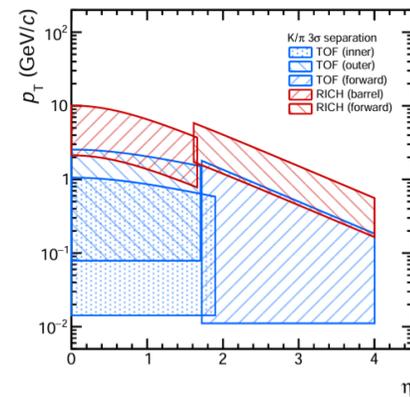
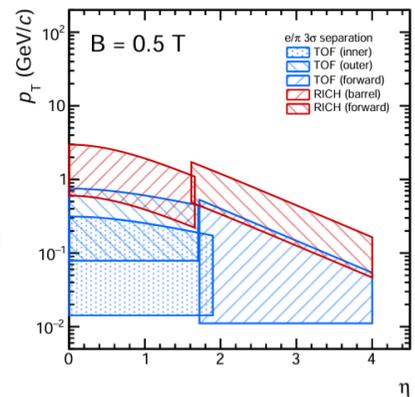
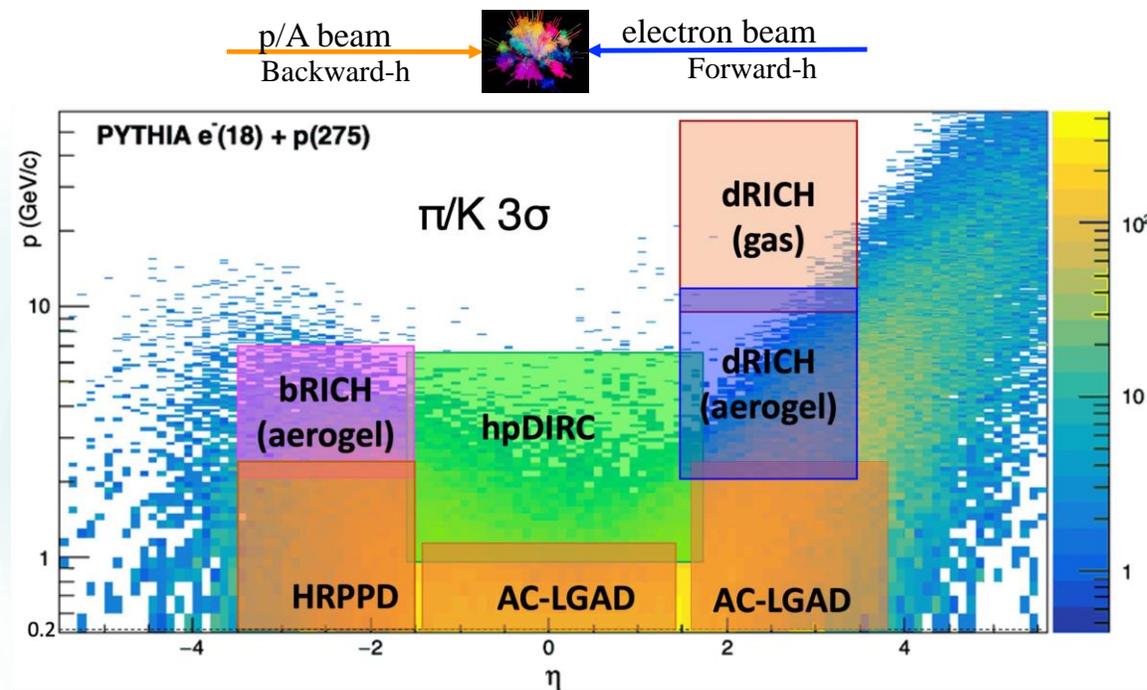
▶ ALICE3実験 (2035-)



ePIC/ALICE3でのPID

▶ ePIC実験 (2030-)

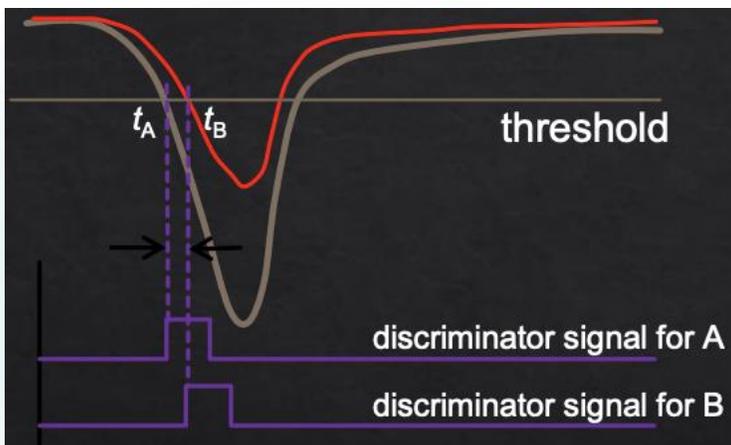
▶ ALICE3実験 (2035-)



シリコン検出器の時間分解能

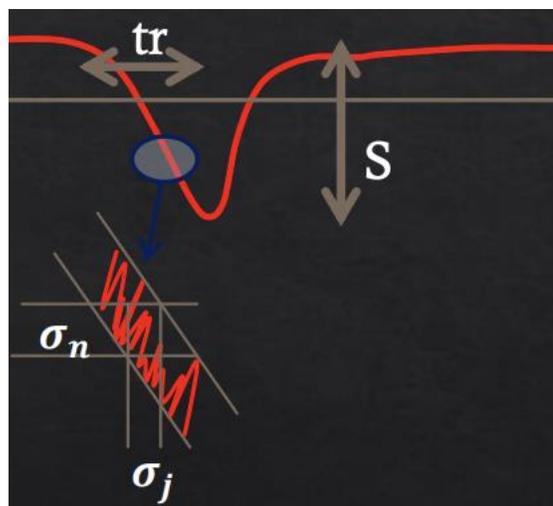
$$\sigma^2 = \sigma_{tw}^2 + \sigma_j^2 + \sigma_L^2$$

タイムウォーク



信号の大きさのばらつきによる Over-thresholdのタイミングのずれ。CFDで補正可能

ジッター



信号に乗るノイズによる影響
ノイズの大きさと立ち上がりの速さに依存

ランダウノイズ

- 電子が励起する際の確率的なばらつき
- Padから遠い電子ほど信号の遅れが出る

検出器の厚さに依存

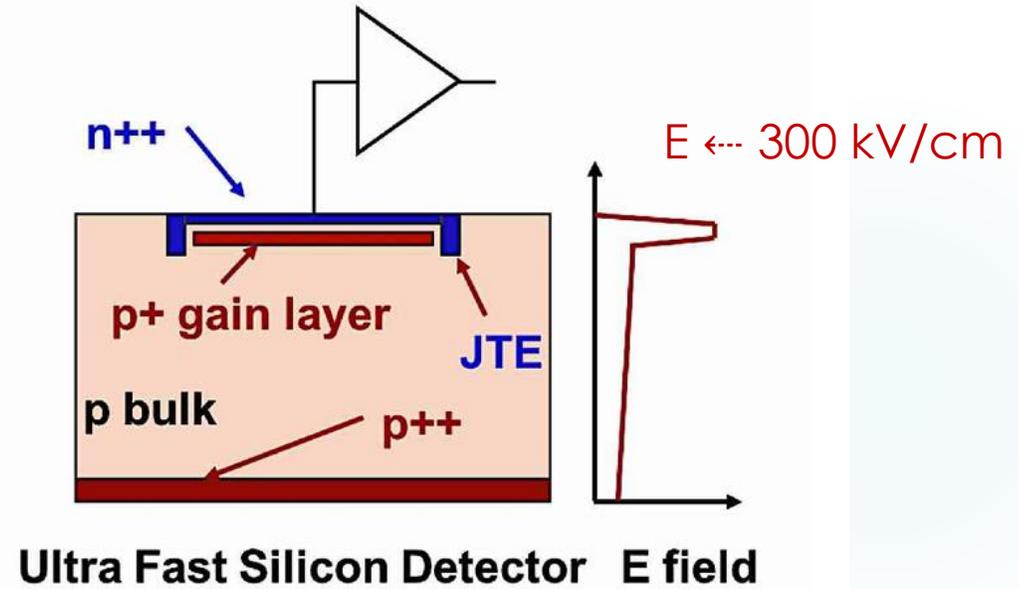
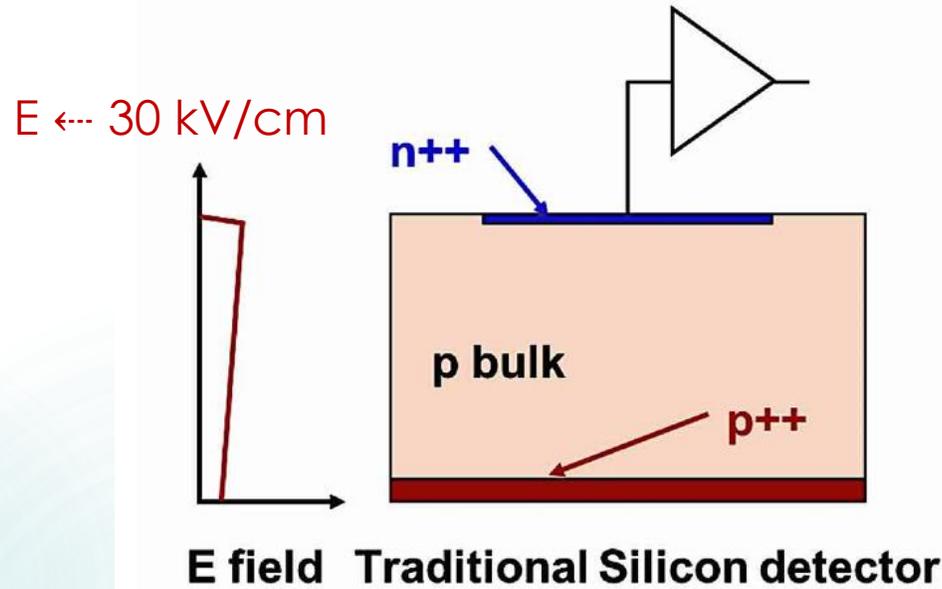
ジッターとランダウノイズの改善が必要

**信号の立ち上がりが速いほど
時間分解能がよい。
低ノイズである必要がある。**

$$\sigma_{TimeSlewing} = [t_d]_{RMS} \propto \left[\frac{N}{dV/dt} \right]_{RMS}$$

$$\sigma_{Jitter} = \frac{N}{|dV/dt|_{V_{th}}} = \frac{t_r}{S/N}$$

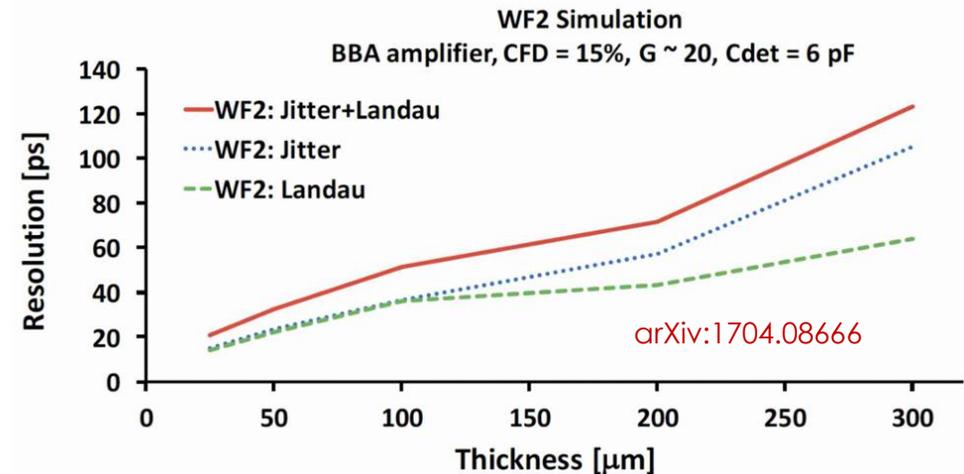
LGAD検出器



- ▶ ゲインレイヤー(濃いpn接合)をPad付近に入れることで強い電場を形成
- ▶ ゲインレイヤーの強い電場で電子雪崩が起き、信号の立ち上がりが速くなる

Ramo's theorem

$$\frac{di_G}{dt} \propto \frac{G}{d}$$

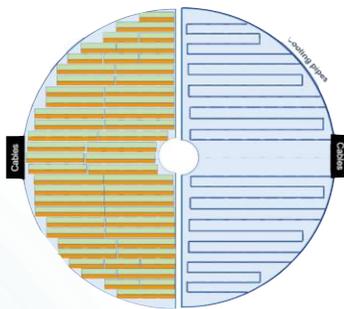
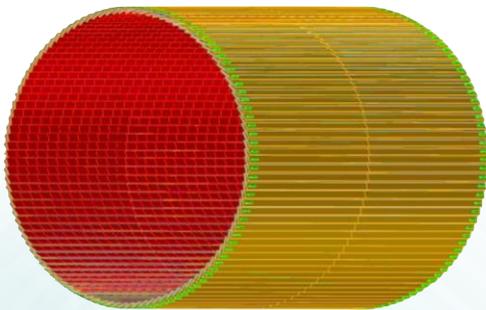


LGAD検出器

▶ ePIC実験では、様々なシステムがAC-LGAD検出器を使用予定

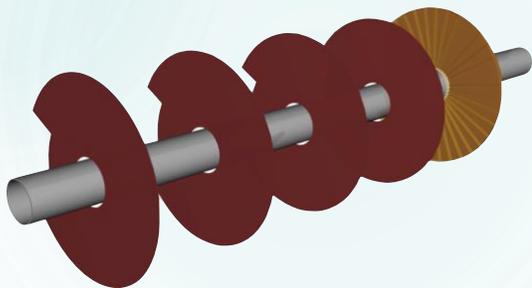
バレル ToF (ストリップ)

前方 ToF (ピクセル)

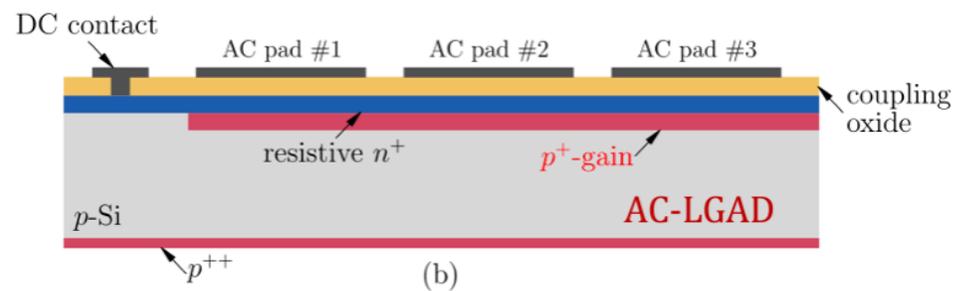
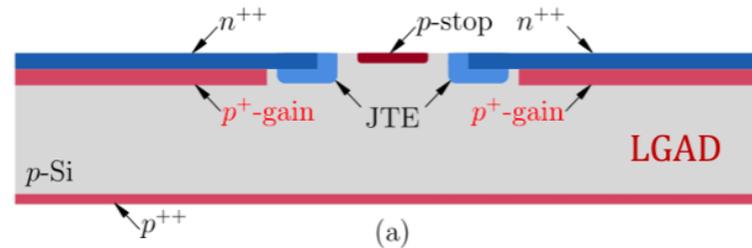


超前方飛跡検出器 (ピクセル)

ローマンポット (ピクセル)



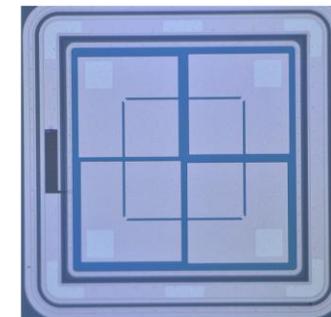
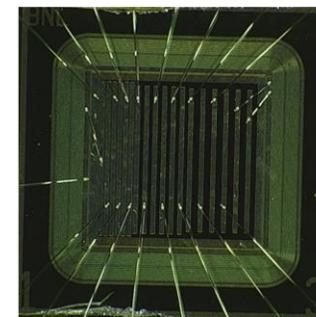
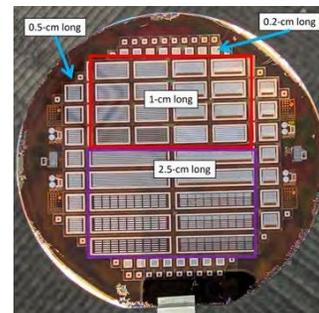
▶ BNLとHPK (eRD112 – LGAD consortium) で製作



BNL 4" wafer

Strip type by BNL

Pad type by HPK



3x3 mm²
Sensor size

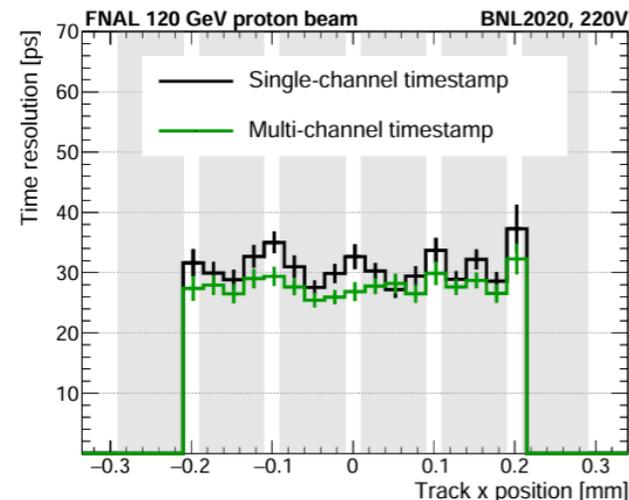
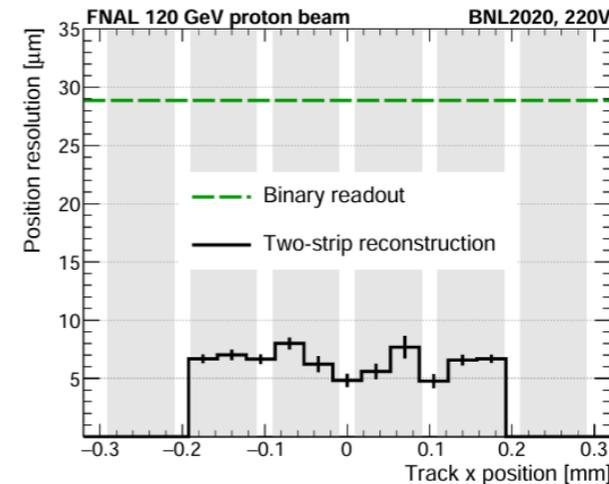
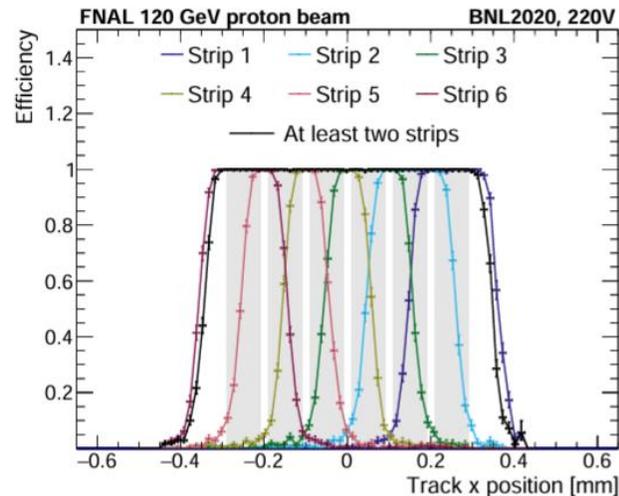
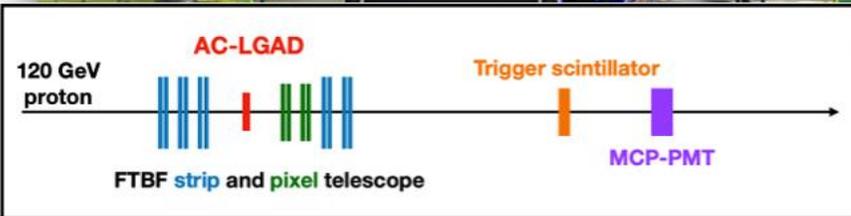
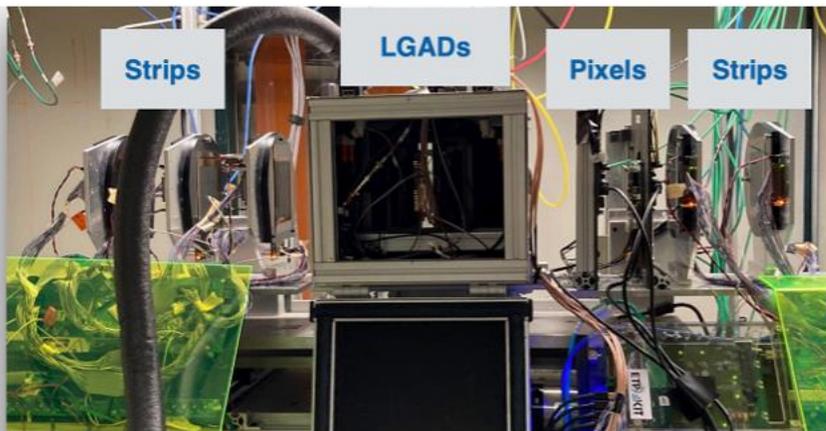
100μm, 150 μm, 200 μm

3x3 mm²
Sensor size

AC-LGADの性能

▶ Permanent setup in FNAL test beam facility (FTBF)

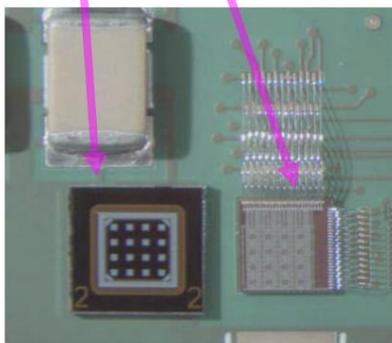
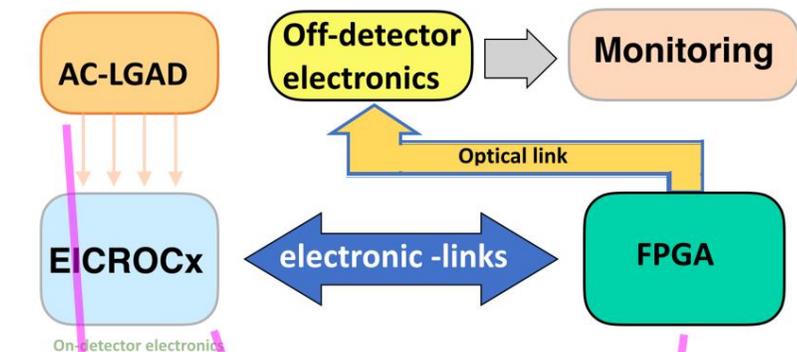
R. Heller *et al.*,
JINST 17 P05001 (2022)



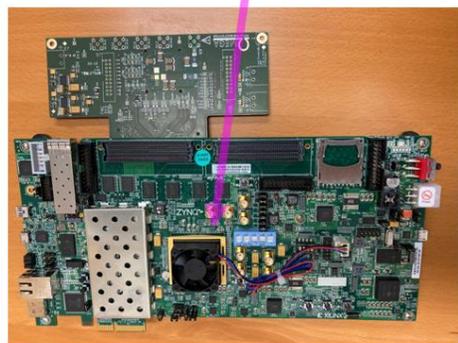
Name Unit	Pitch μm	Primary signal amp. mV	Position res. μm	Time res. ps
BNL 2020	100	101 ± 10	≤6	29 ± 1
BNL 2021 Narrow	100	104 ± 10	≤9	32 ± 1
BNL 2021 Medium	150	136 ± 13	≤11	30 ± 1
BNL 2021 Wide	200	144 ± 14	≤9	33 ± 1
HPK C-2	500	128 ± 12	22 ± 1	30 ± 1
HPK B-2	500	95 ± 10	24 ± 1	27 ± 1

Designed and produced by
KEK/Tsukuba with HPK

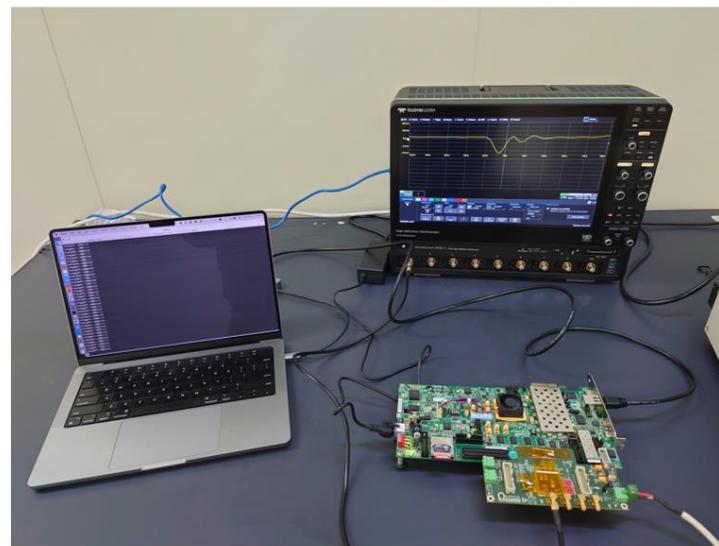
- 米国 BNL, 広島大学, ... (IJCLab/Omega と協力)
- AC-LGAD 素子 + 読出 ASIC (EICROC)



拡張基板に載った AC-LGAD と EICROC



プロトタイプ読出基板 (Xilinx 開発キット = FPGA + ZYNQ プロセッサ)



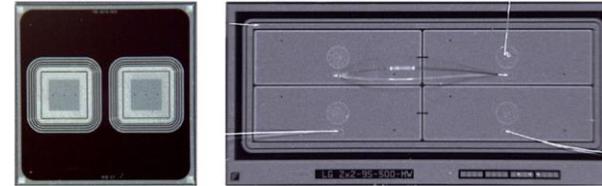
広島大学テストベンチ (一部)

- 多種アセンブリのチェーン性能評価
 - 形状などを変更した複数の BNL / 浜松製 AC-LGAD 素子
 - TCAD シミュレーションによる検出素子内部構造最適化
 - ASIC(s) + 読出基板試作機
 - ストリップ形状などの調整も含めた適合性
 - 要求性能 ~ 30 ps, ~ 30 μ m 堅持
- β 線, IR レーザー, 陽子線 (FNAL), 電子線 (ELPH)
 - 時間 / 位置分解能
 - 電荷収集効率, 電極間共有
- 日本国内におけるストリップ型 AC-LGAD 技術確立
 - 設計, シミュレーション, 製作, システム統合, データ解析

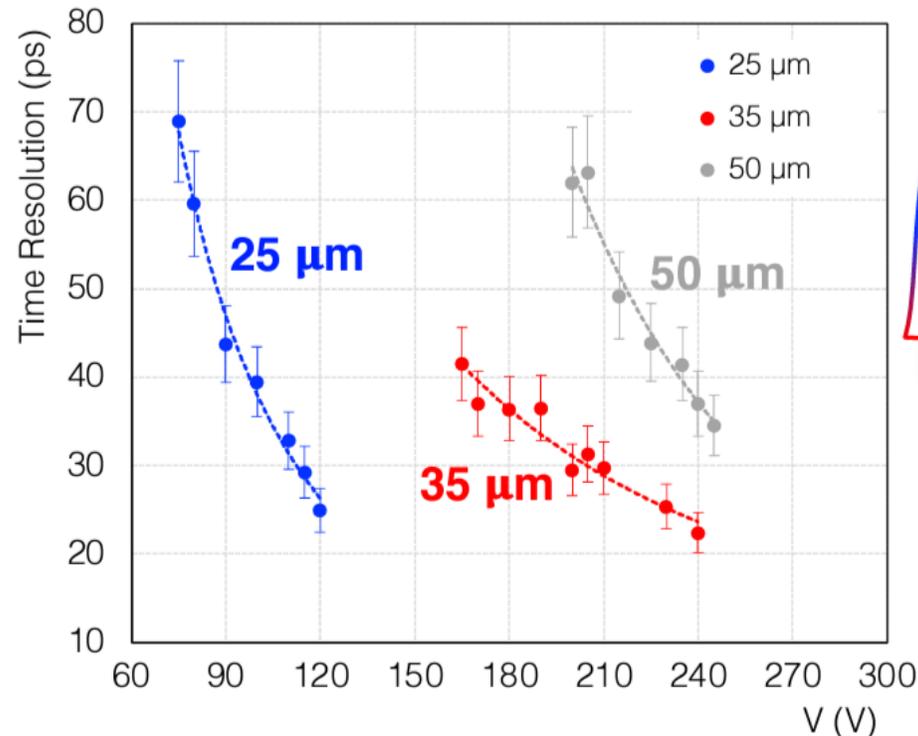
LGAD R&D for ALICE3

- ▶ First beam test 2021 on very thin FBK LGAD: 25 and 35 μm thick

<https://link.springer.com/article/10.1140/epjp/s13360-022-03619-1>



	Area	Thickness	V_{bd}	Voltage applied	Gain
FBK25	$1 \times 1 \text{ mm}^2$	25 μm	$127.3 \pm 0.1 \text{ V}$	75-120 V	13-57
FBK35	$1 \times 1 \text{ mm}^2$	35 μm	$260.7 \pm 0.2 \text{ V}$	165-240 V	10-49
HPK50	$1 \times 3 \text{ mm}^2$	50 μm	$253.0 \pm 0.2 \text{ V}$	200-245 V	26-61



Improved time resolution with thinner LGAD with respect to the standard 50 μm

Standard LGAD (50 μm) in line with the expectations

- ▶ Validation of the setup and the analysis procedure

35 μm

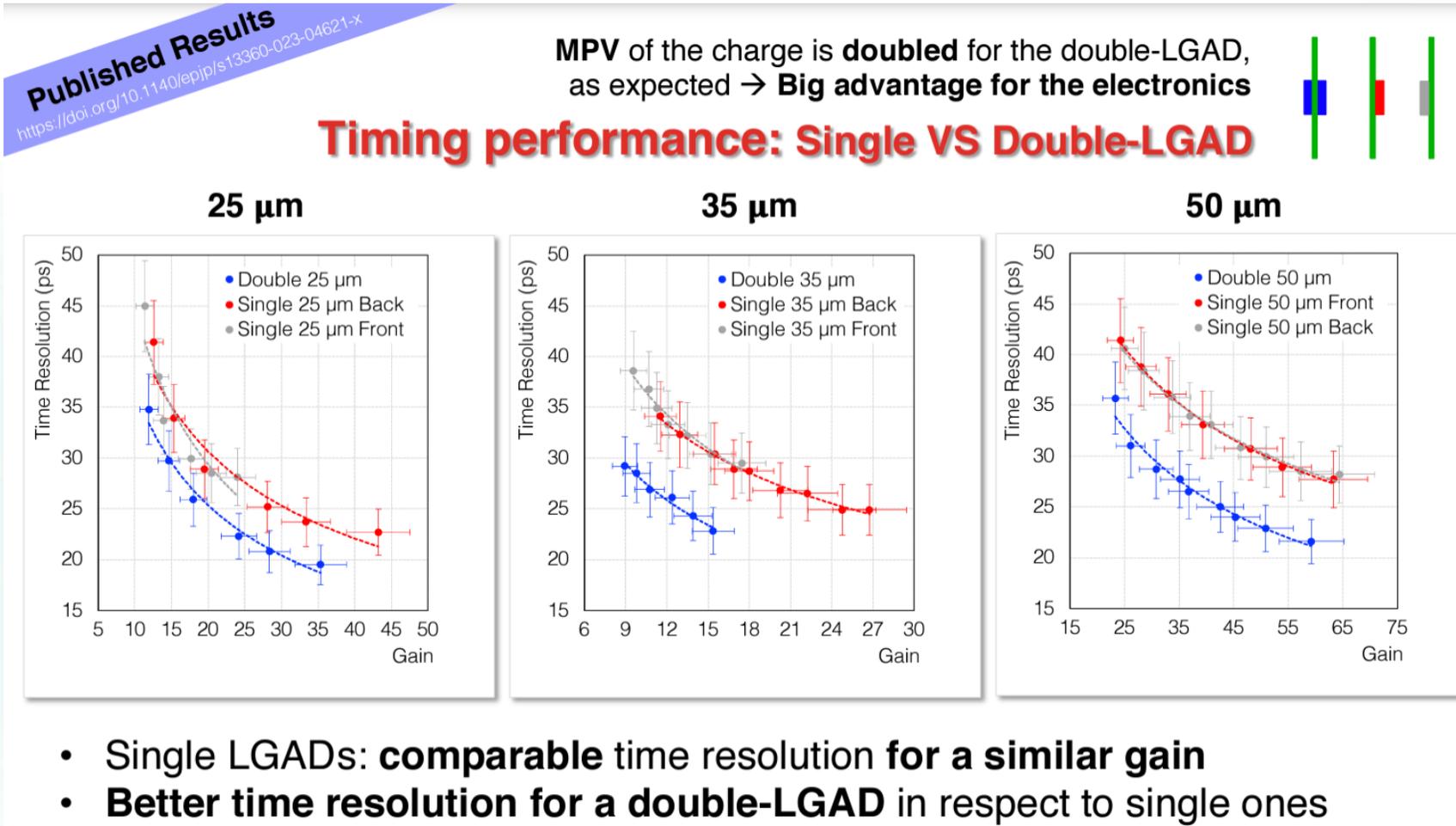
22 ps : In agreement with MC simulations

25 μm

25 ps : Slightly worse time resolution than what foreseen from simulations (worse S/N)

LGAD R&D for ALICE3

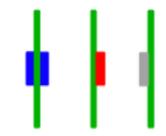
► Double LGAD



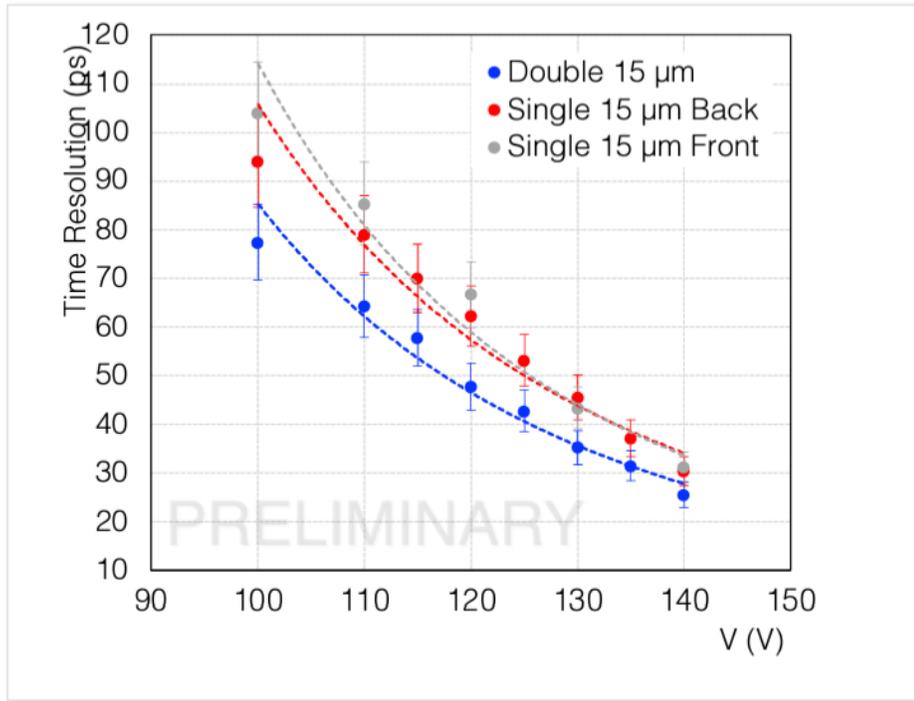
LGAD R&D for ALICE3

New Results

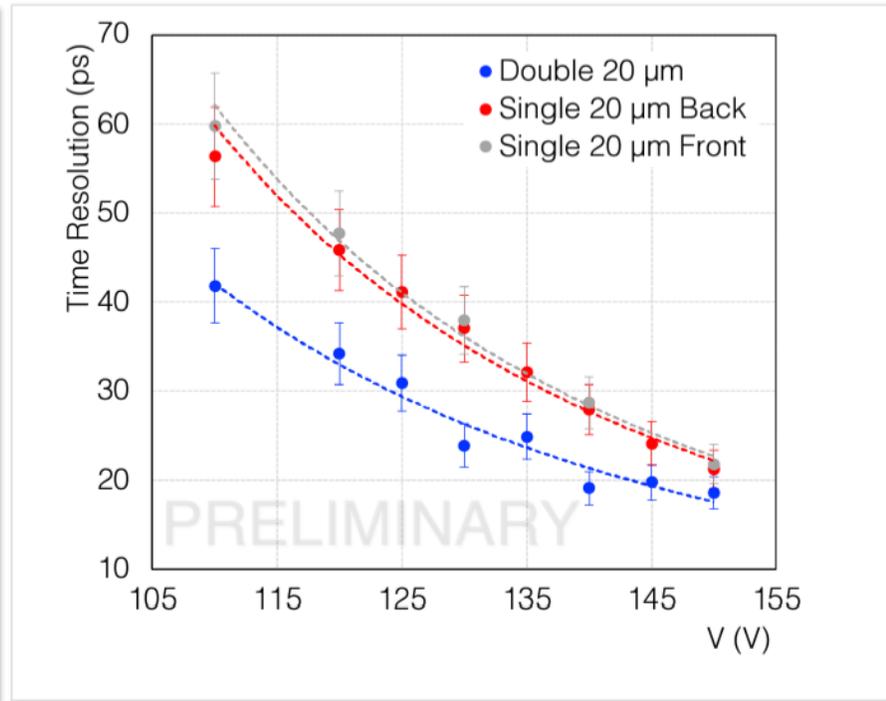
Timing performance VS Voltage Single & Double-LGAD



15 μm



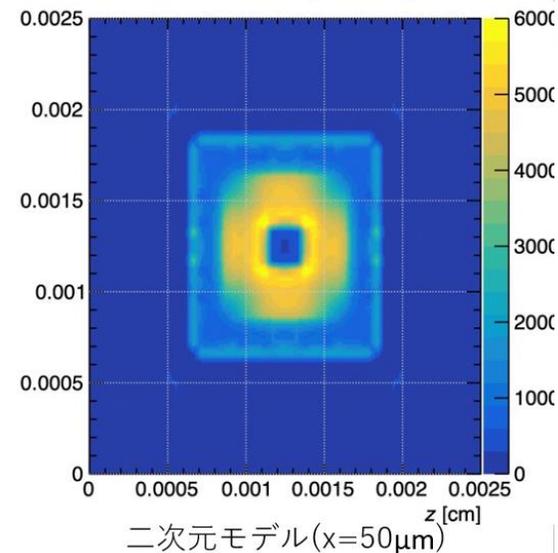
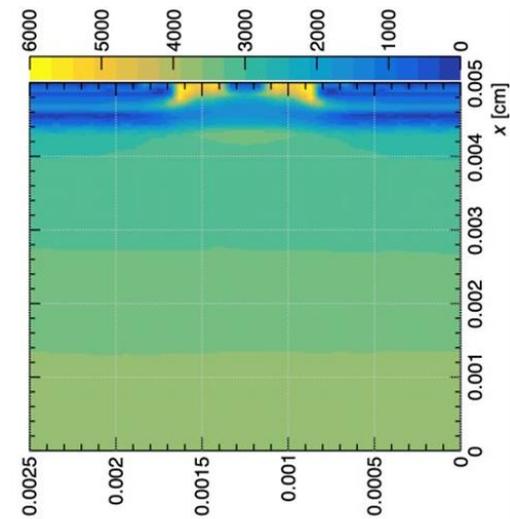
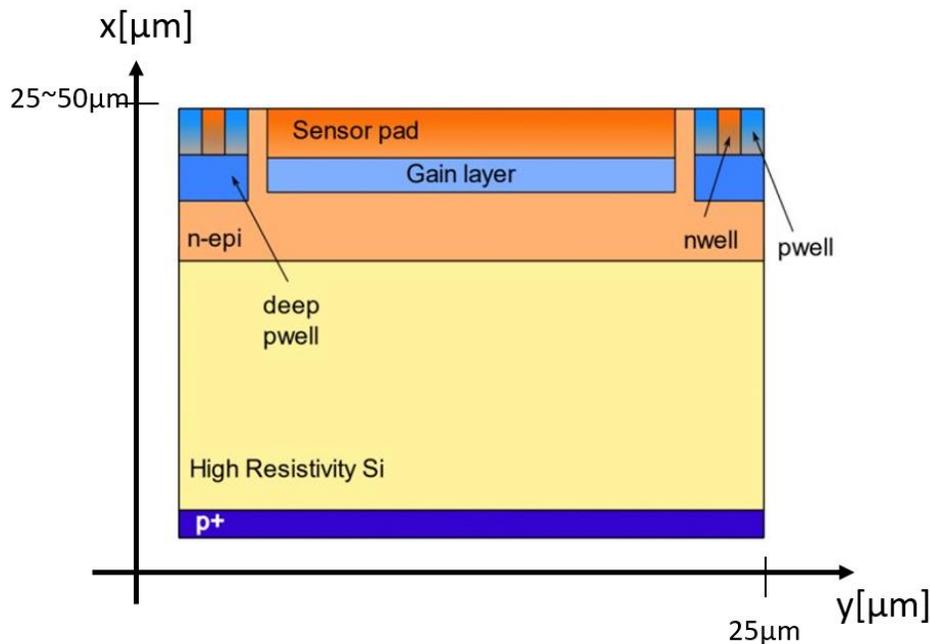
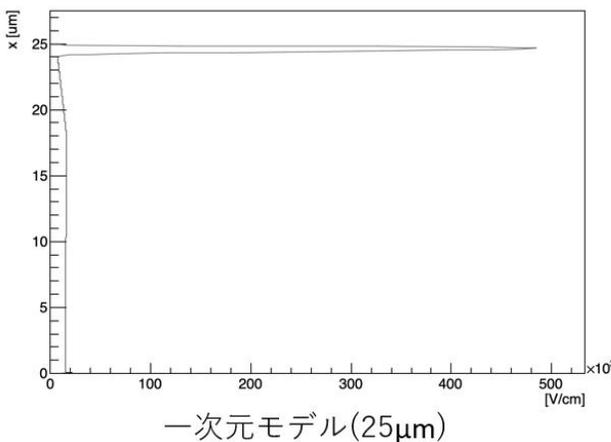
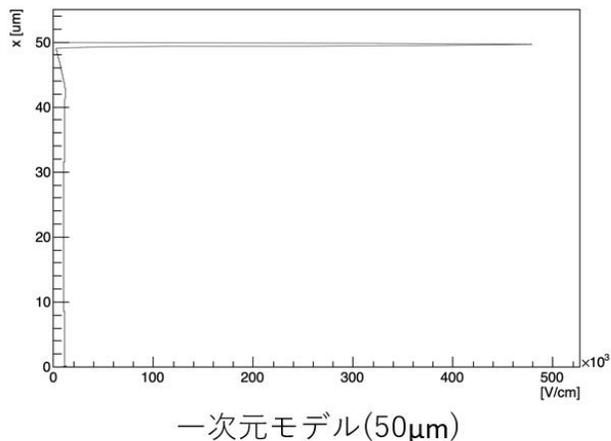
20 μm



- Single LGADs: **comparable** time resolution for a similar voltage
- **Better** time resolution for a **double-LGAD** in respect to single ones

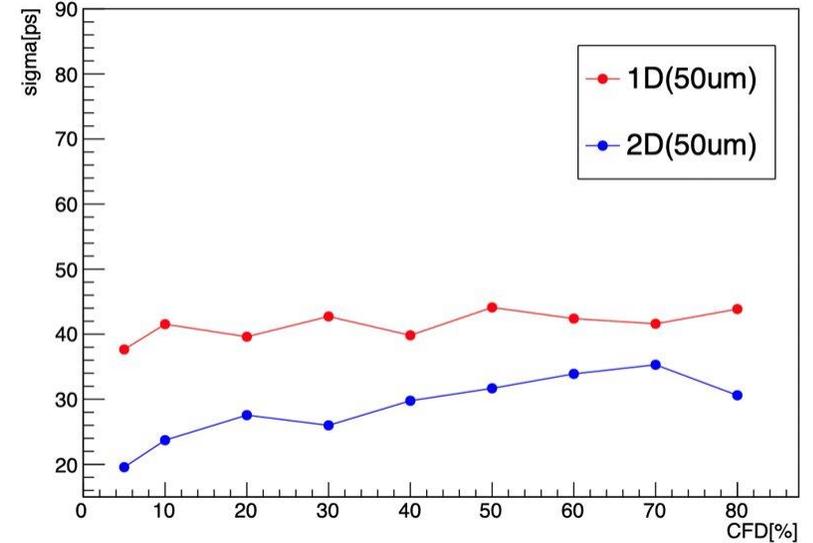
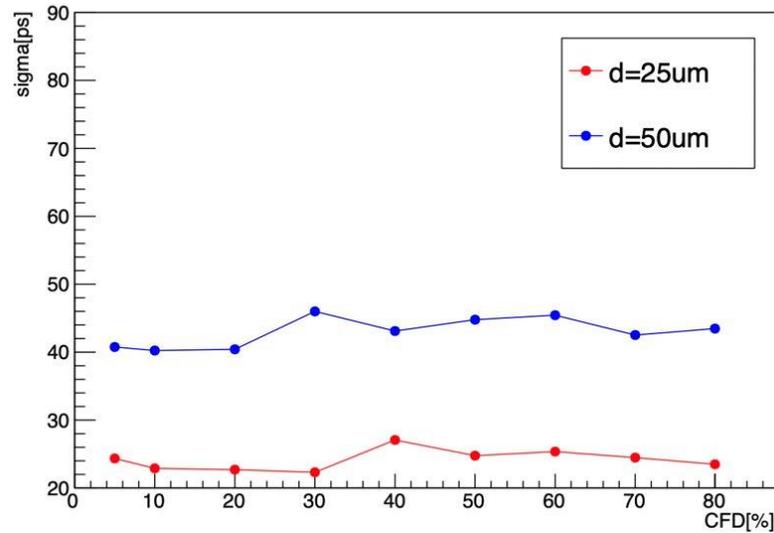
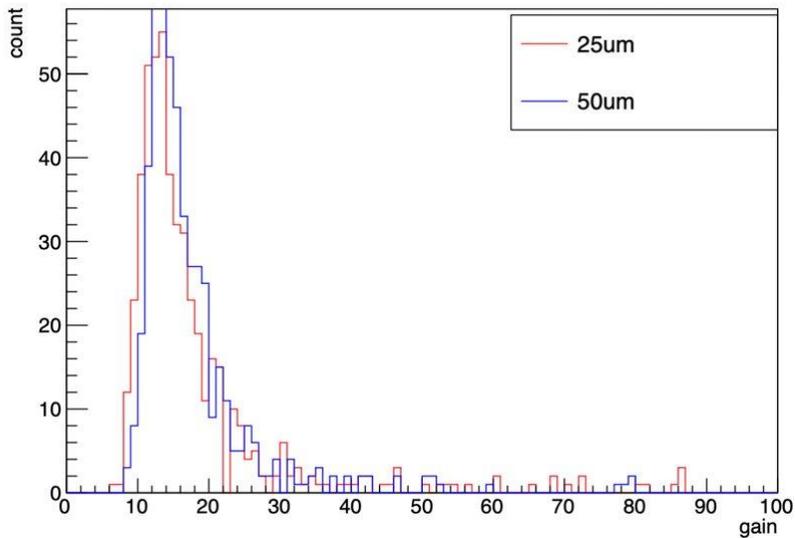
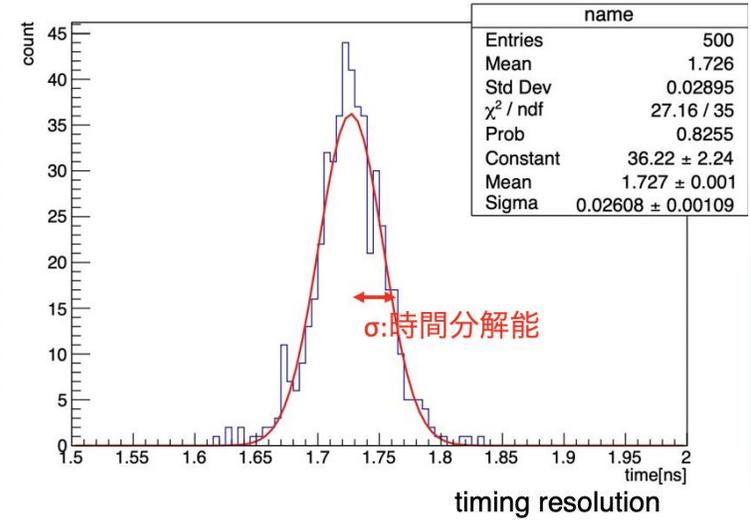
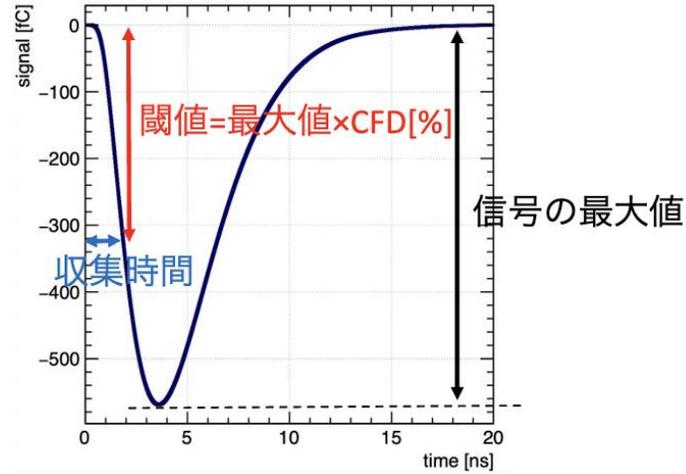
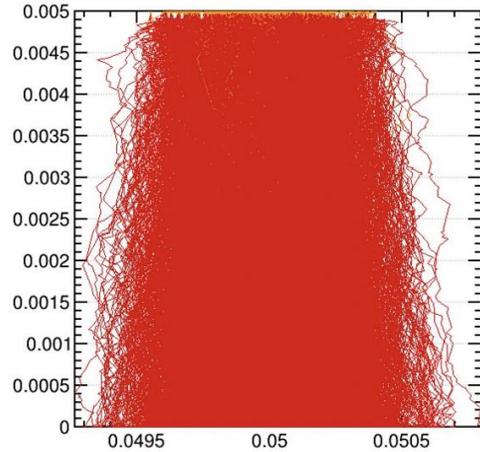
CMOS-LGADに向けたGarfield simulation

電場



CMOS-LGADに向けたGarfield simulation

$$f(t) = g \exp(n) \left(\frac{t}{t_p}\right)^n \exp(-t/\tau), \quad t_p = n\tau, \quad (n=2.5 \tau=1.5 \ g=50)$$



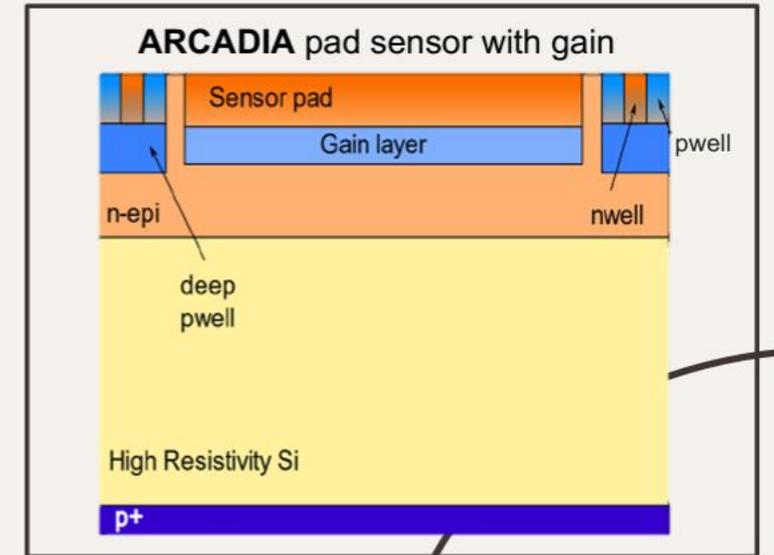
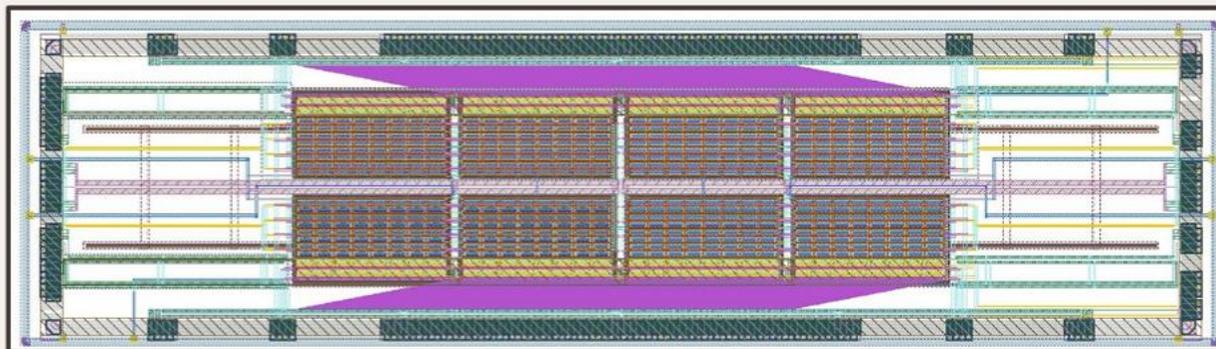
MadPix

*Monolithic CMOS Avalanche Detector **PIX**elated Prototype for ps Timing Application*

First prototype with **integrated electronics** (LFoundry 110 nm) and **sensor gain**

Active thickness: 48 μ m

- **Backside HV:** allow full depletion \rightarrow -25 V to -40 V
 - **Topside HV:** manage the gain \rightarrow 30 V to 50 V
- » 8 matrices of 64 pixels each » 64 x 2 analogue outputs
- » 4 flavours » Pixels of 250 μ m x 100 μ m



Symmetrical

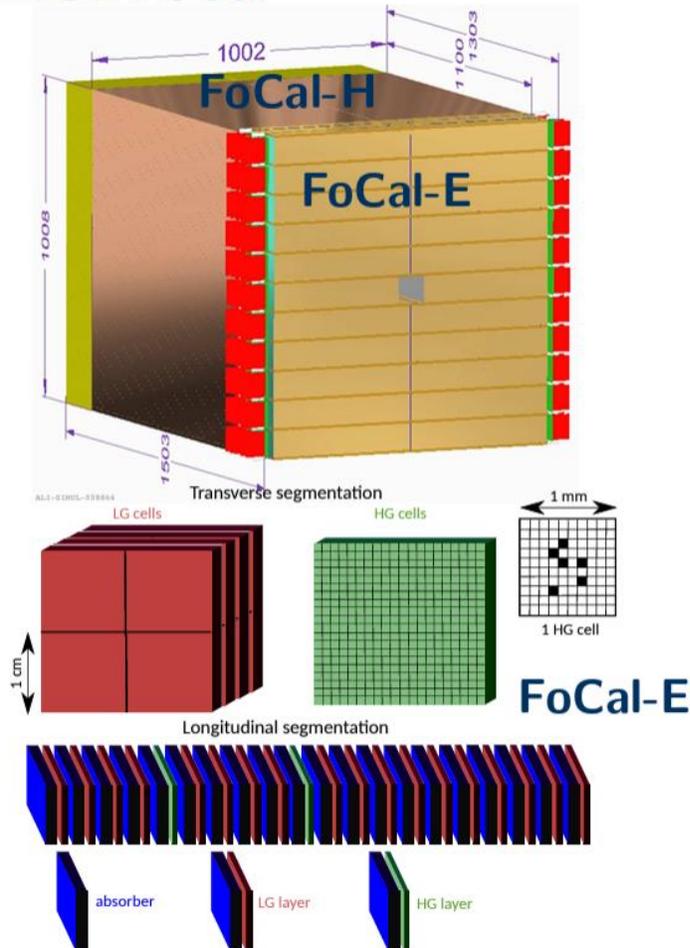
Lucio Panheri

CMOS-LGADの今後

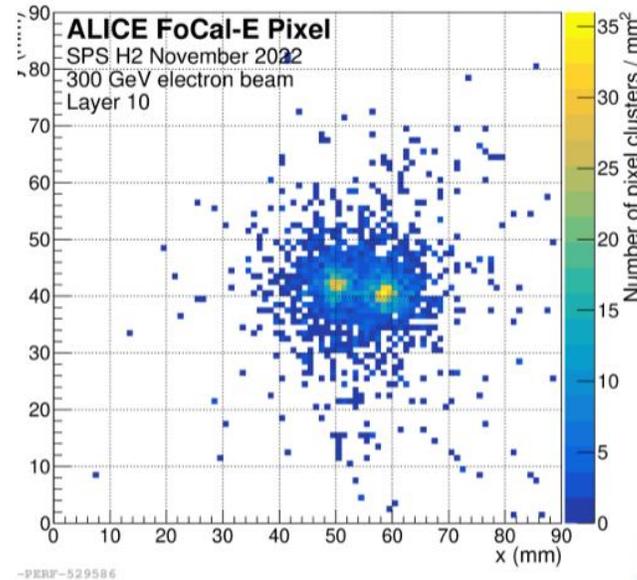
- ▶ レートが高い実験では、時間分解能の良い検出器がないと大変
 - ▶ しかも、ストリーミングで読んでしまうと、どのイベントからくるのか、同定が難しい
- ▶ LGADがCMOSで読み出しと一体化できれば、究極の検出器になると思う
- ▶ CMOS-LGADの開発を継続したいが（東大はGarfield simulationでのstudyをやっていたが、人がいないので継続するのが難しくなってきた）、マンパワーがない
- ▶ 何とか継続したいが、興味があればぜひ！

CMOS sensor imaging calorimeter

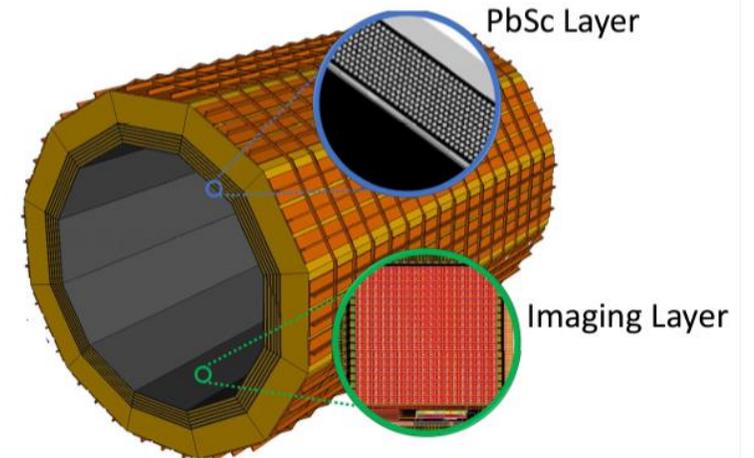
ALICE FoCal



Shower separation in FoCal-E pixels



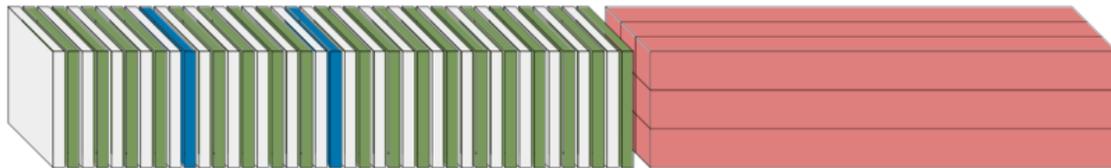
Similar approach is also considered for the EPIC BECAL



Pixel layers (ALPIDE) interleaved with Si PAD

ePIC ZDCとALICE-FOCAL

▶ ALICE-FOCAL



FoCal-E

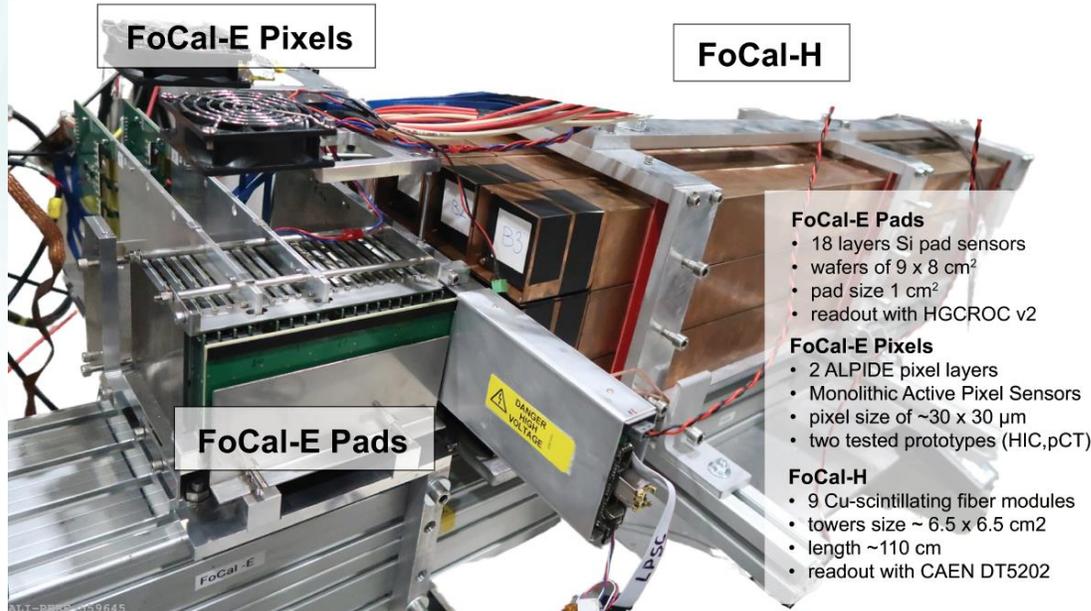
- 20 tungsten layers, with thickness of 3.5 mm = $1 X_0$
- 18 layers of silicon pad sensors, pad size $\approx 1 \times 1 \text{ cm}^2$
- 2 layers of silicon pixel sensors, pixel size $\approx 30 \times 30 \mu\text{m}^2$

FoCal-H

- length of 110 cm
- copper "strawtubes" with 2.0 mm diameter
- scintillating fibre with $\approx 1.1 \text{ mm}$ diameter

FoCal-E Pixels

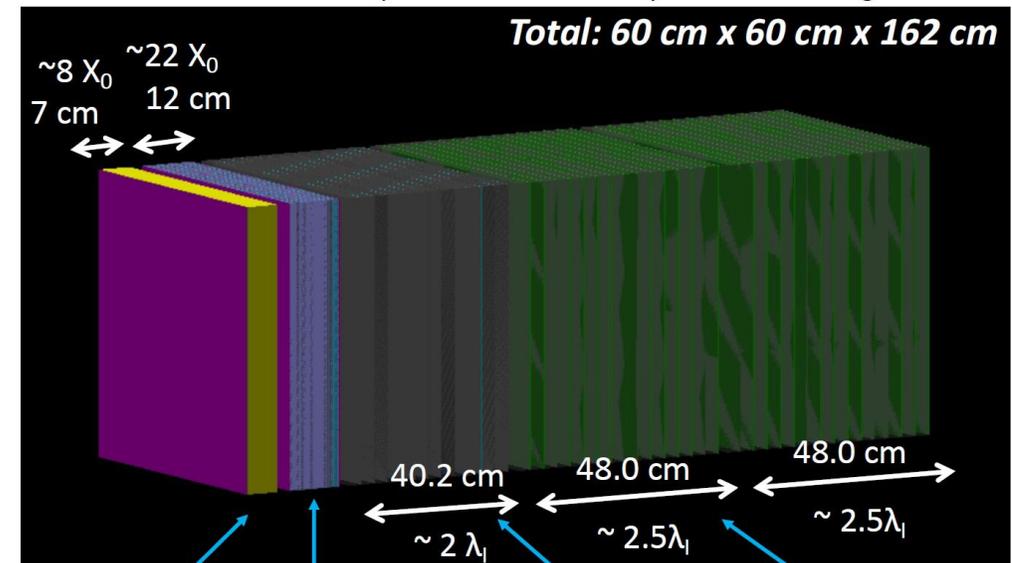
FoCal-H



- FoCal-E Pads**
 - 18 layers Si pad sensors
 - wafers of $9 \times 8 \text{ cm}^2$
 - pad size 1 cm^2
 - readout with HGCR0C v2
- FoCal-E Pixels**
 - 2 ALPIDE pixel layers
 - Monolithic Active Pixel Sensors
 - pixel size of $\sim 30 \times 30 \mu\text{m}$
 - two tested prototypes (HIC,pCT)
- FoCal-H**
 - 9 Cu-scintillating fiber modules
 - towers size $\sim 6.5 \times 6.5 \text{ cm}^2$
 - length $\sim 110 \text{ cm}$
 - readout with CAEN DT5202

▶ ZDC

*note: space for readout may extend the longitudinal length.



Crystal (PbWO_4) + Silicon Pixel layer W/Si calo. 3 Pixel layers are inserted. Pb/Si calo. Pb/Sci. calo.

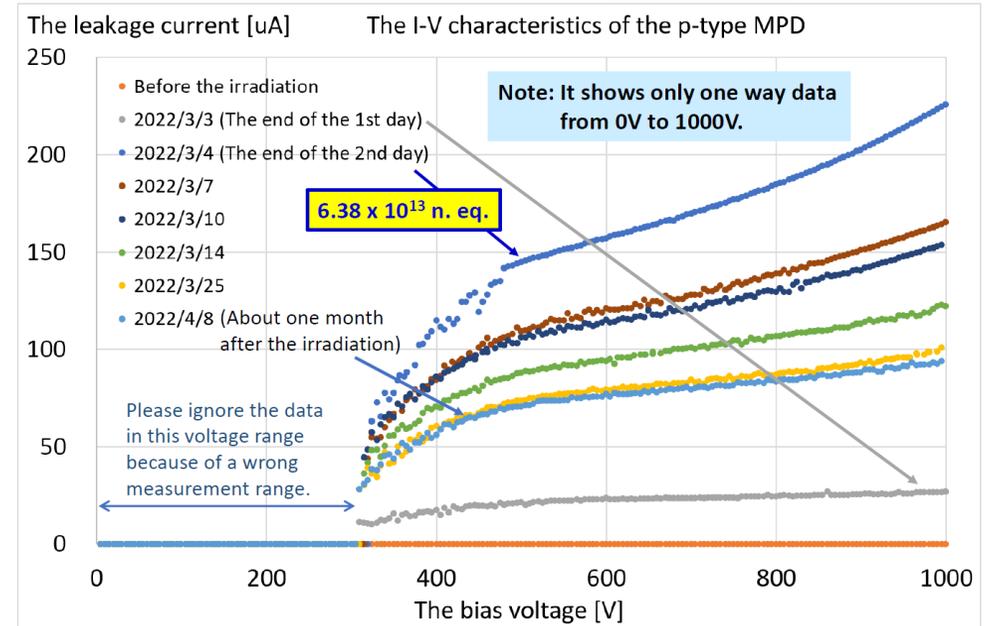
中性子照射テスト@理研RANS

▶ 放射線耐性

- ▶ ePIC-ZDCでは、1年間で $10^{11} - 10^{12}$ neutron/cm² 以上の放射線量
- ▶ ALICE-FoCal実験と同程度の放射線量

▶ 理研RANS

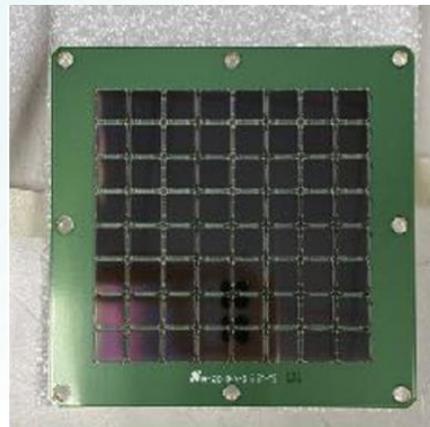
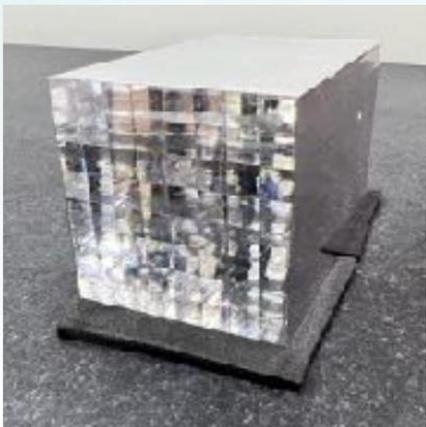
- ▶ 7MeV陽子、100 μ A、 6×10^{13} proton/s
 - ▶ 安定して出せる最大電流は40 μ A程度
 - ▶ Be標的から最大5MeVの中性子、標的から2cmで 10^8 neutron/cm²/s程度
- ▶ FoCal-E padのp-type/n-typeのbaby-chip/MPD、ePIC結晶カロリメータ読み出し用のAPD/SiPMをテスト
 - ▶ MPD (九州大提供)、インジウム箔、温度計でモニター



LYSO結晶の製作

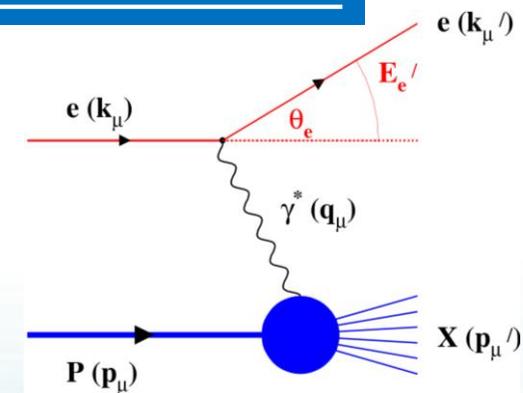
- ▶ 台湾グループがLYSO結晶のプロトタイプ検出器を製作
 - ▶ LYSO結晶、SiPM読出し
 - ▶ 今年2月テストビーム@東北大ELPH
 - ▶ 50 – 800 MeV 陽電子
 - ▶ 今年中に第2回テストビーム
 - ▶ LYSOとPWOの比較
 - ▶ SiPMとAPDの比較
 - ▶ FoCal-E Pad と組み合わせ

	X ₀	LY (ph/MeV)	T dep. of LY (%/K)	Decay time (ns)	λ _{em} nm
PbWO ₄ (CMS)	0.89 cm	200	-1.98	5 (73%) 14 (23%) 110 (4%)	420
LYSO	1.14 cm	30,000 (market standard)	-0.28	36	420
GAGG	1.59 cm	40,000 – 60,000		50 – 150	520
SciGlass	2.4-2.8 cm	>100		22 – 400	440-460



Coverage of ePIC

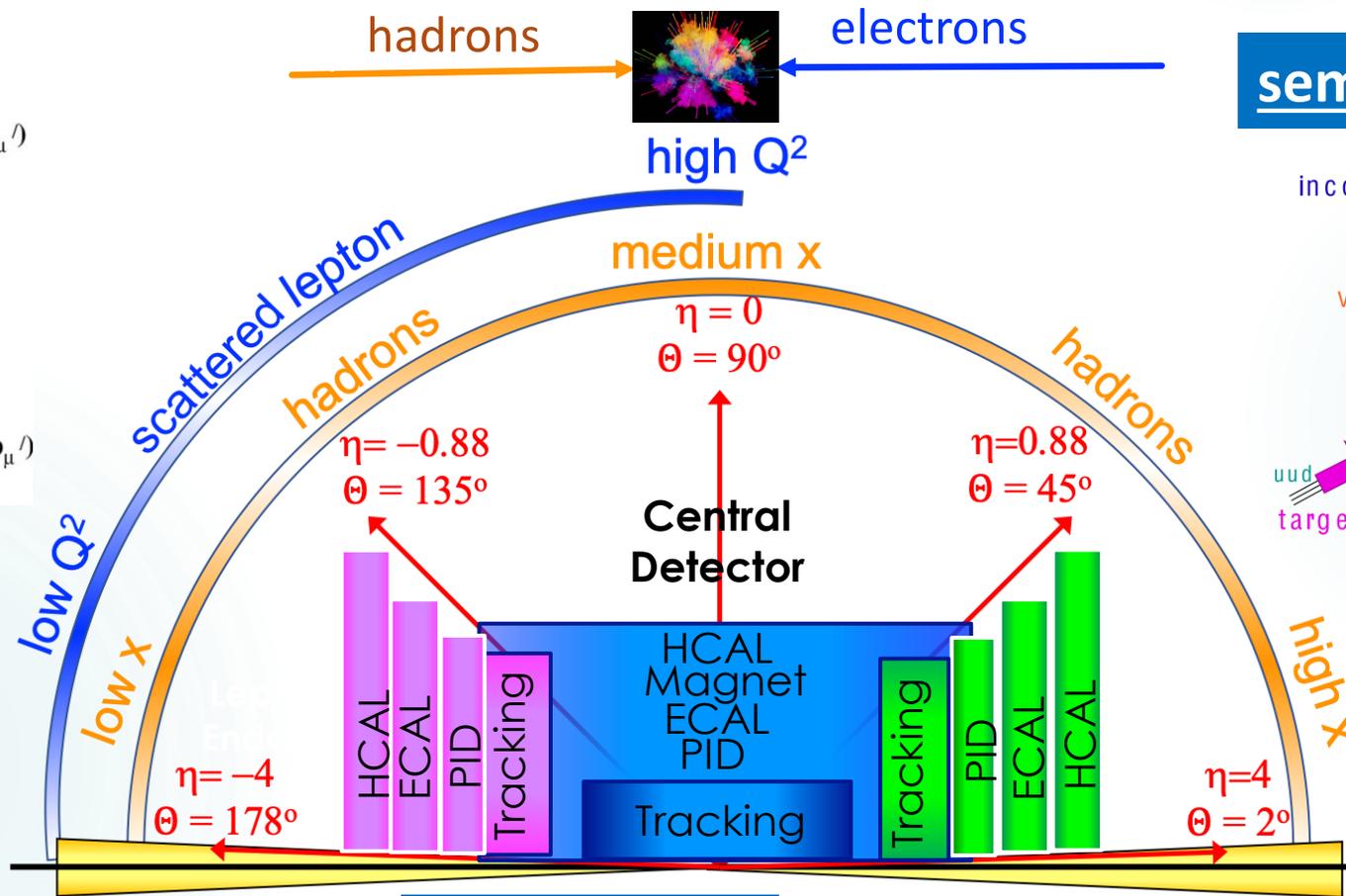
inclusive DIS:



Detect only the scattered lepton in the detector

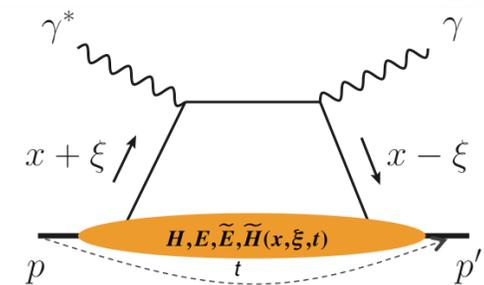
very low Q^2
scattered lepton
Bethe-Heitler photons
for luminosity

Luminosity Detector
Low Q^2 -Tagger

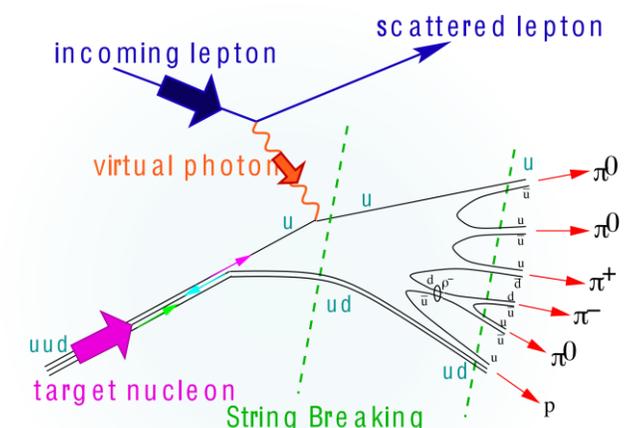


exclusive DIS

Detect scattered lepton, identify produced hadrons/jets and target remnants



semi-inclusive DIS



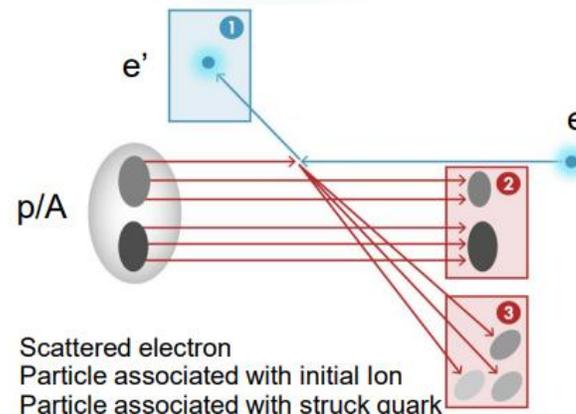
Detect the scattered lepton in coincidence with identified hadrons/jets

particles from nuclear breakup and from diffractive reactions

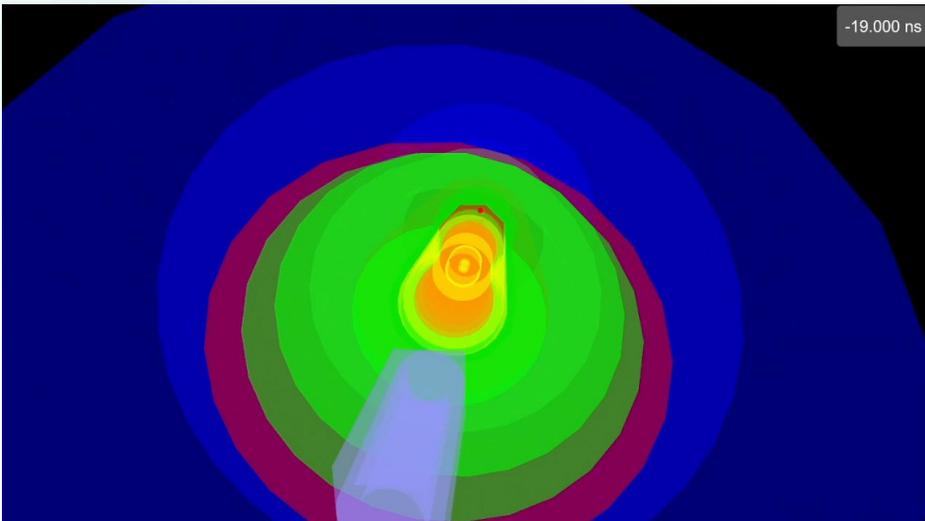
ZDC
Forward Tracking

Triggerless DAQ

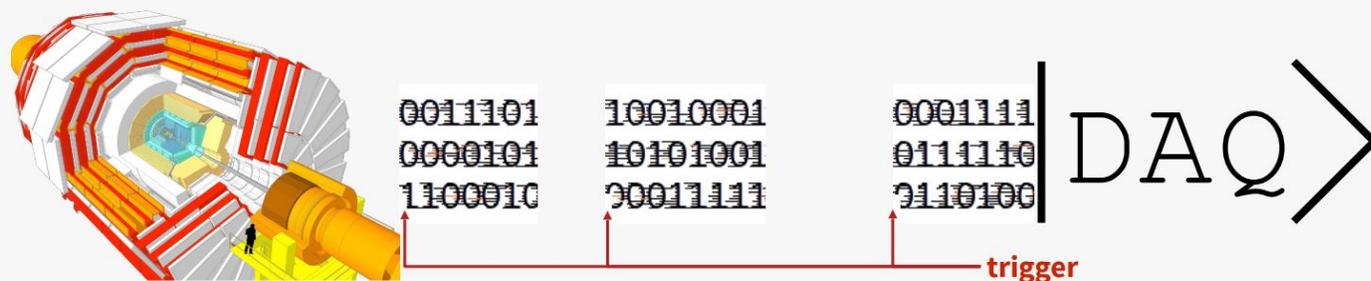
EIC Physics demands ~100% acceptance for all final state particles (including particles associated with initial ion)



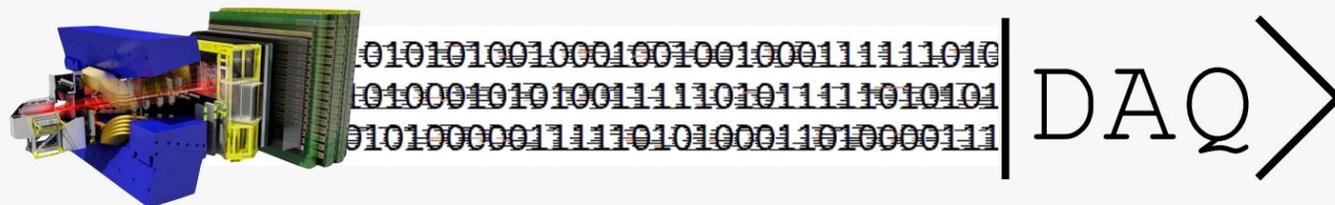
Bunch Crossing ~ 10.2 ns/98.5 MHz
Interaction Rate ~ 2 μs/500 kHz



Triggered: data is readout from detector only when a trigger signal is raised

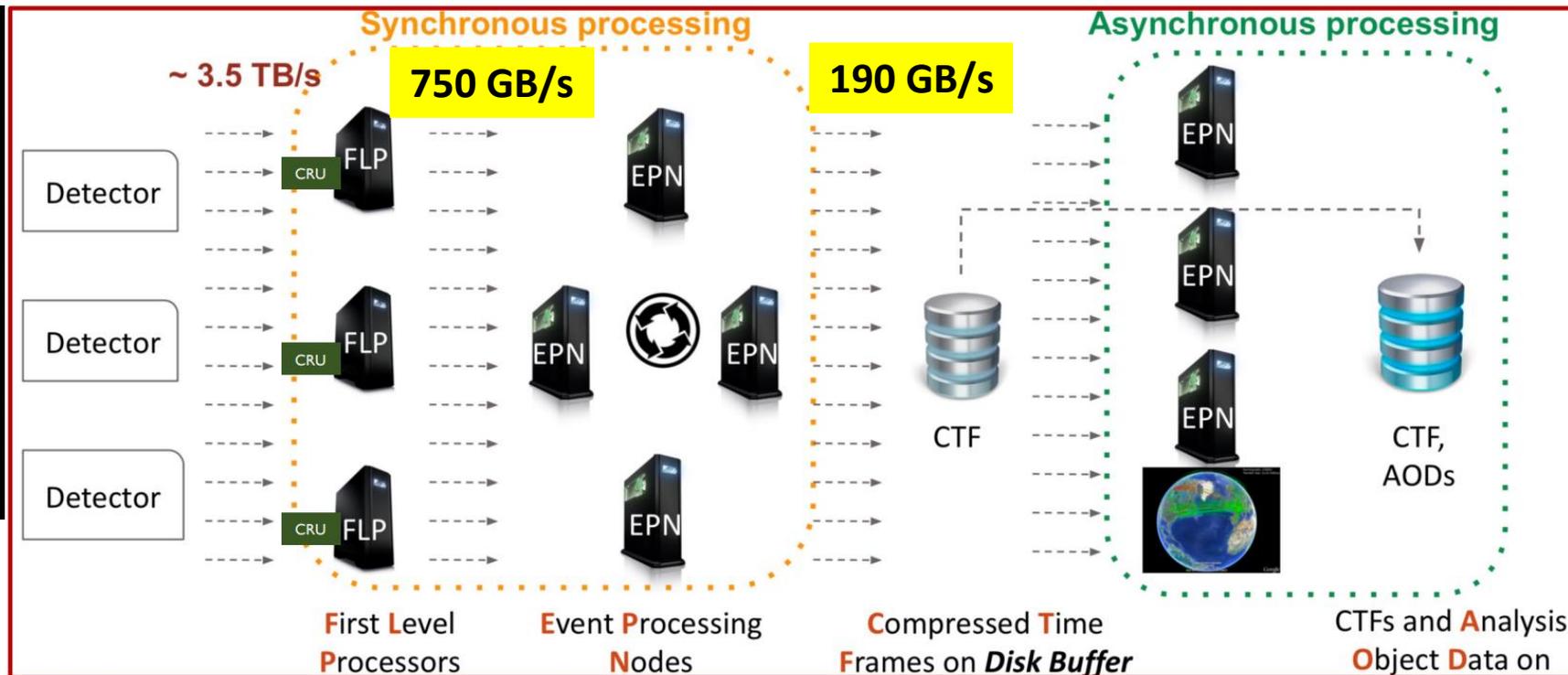
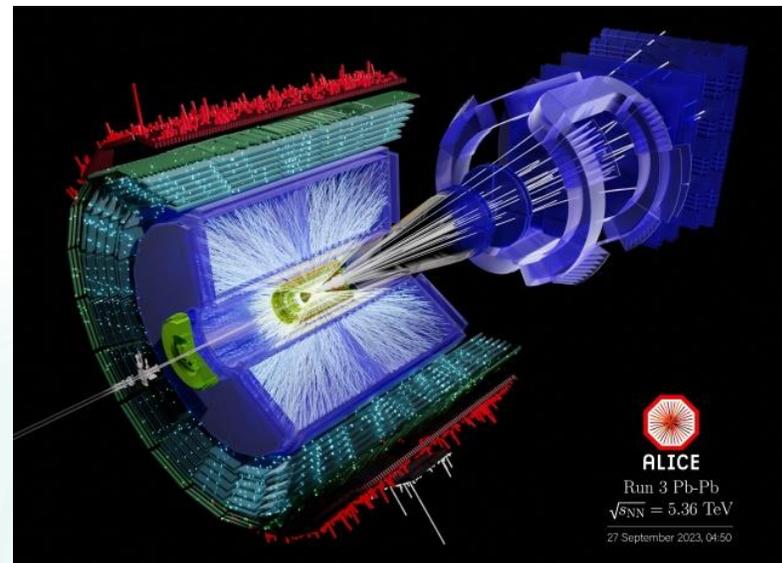


Triggerless: the detector push data at its speed and the downstream DAQ must keep the pace



Triggerless DAQ@ALICE

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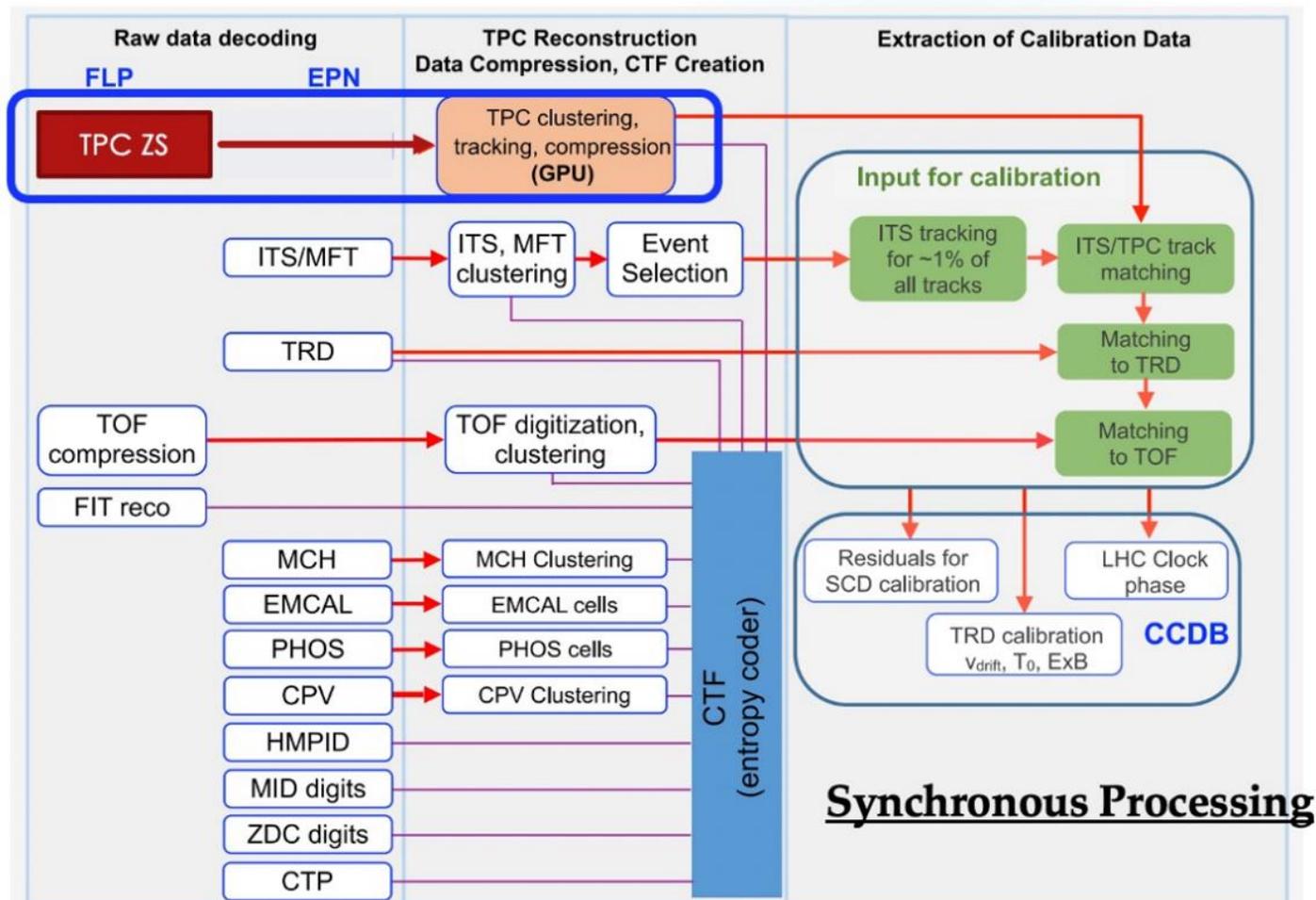
15 detectors
Data Volume as predicted
Acquisition with 364
equivalent MI50 EPNs

2023-10-06 19:21:39	StfBuilder	StfSender	TFBuilder	DPL in	CTF Writer
2i6Y3Bq7ENV			744 GB/s	747 GB/s	186 GB/s
544167					
PHYSICS					
747 GB		747 GB			

Triggerless DAQ@ALICE

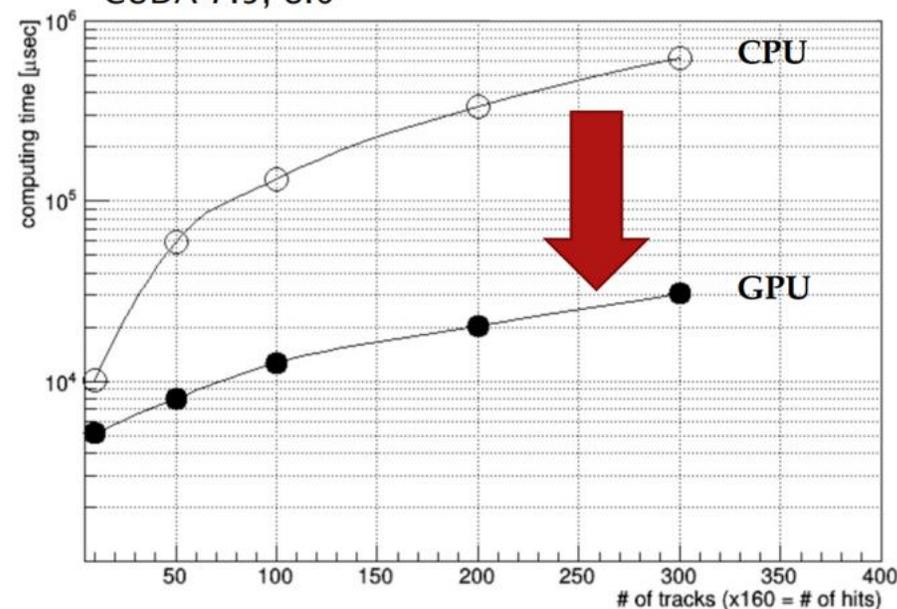
51

Synchronous processing of TFDData in EPN (250 EPNs, 2000 GPU's)

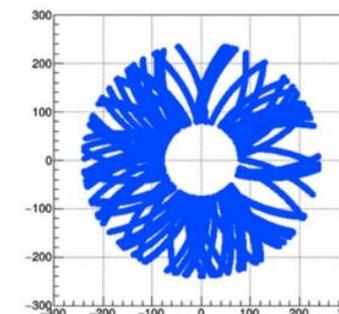
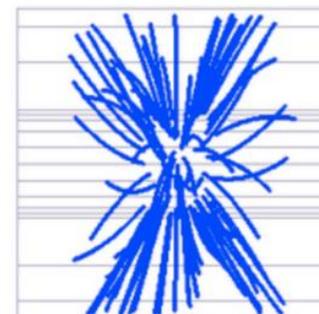


GPU = NVIDIA GTX970
 CUDA 7.5, 8.0

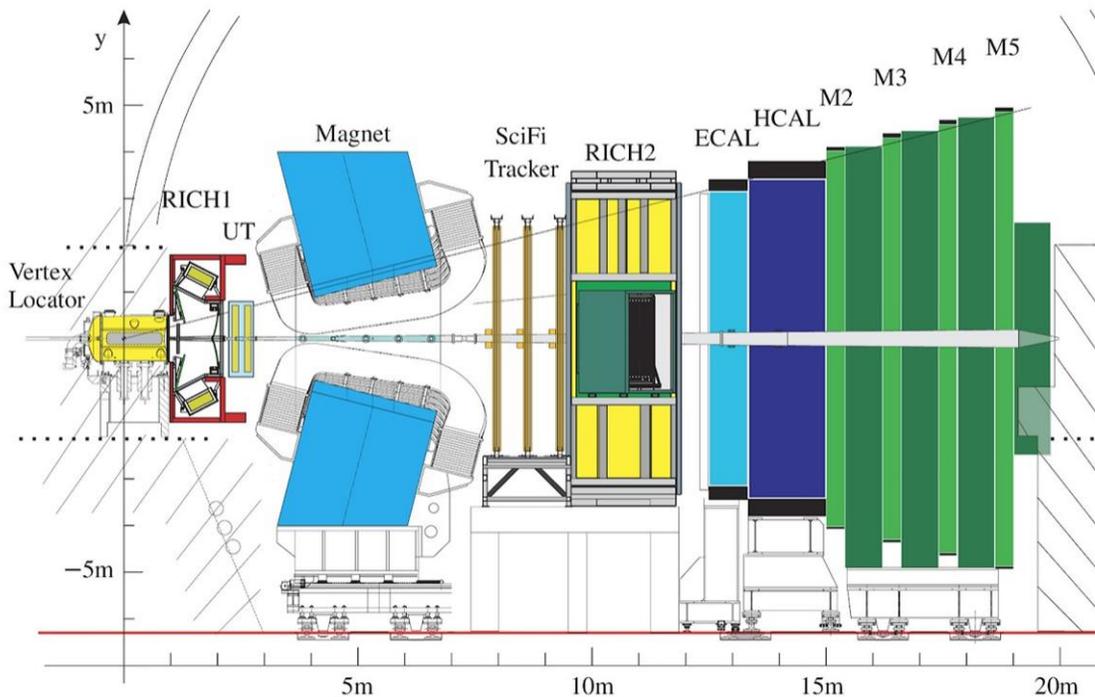
TPC tracking in GPU (2015)



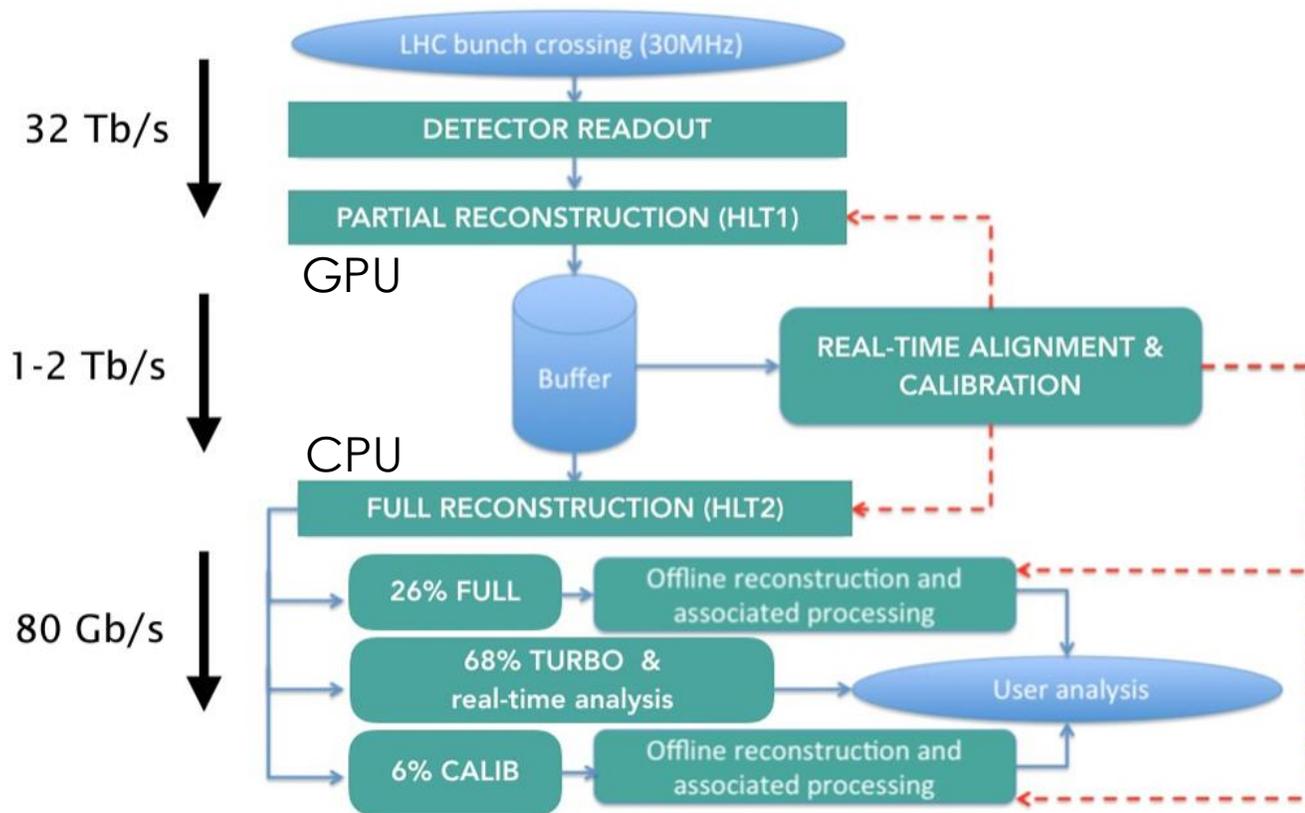
TPC Tracking



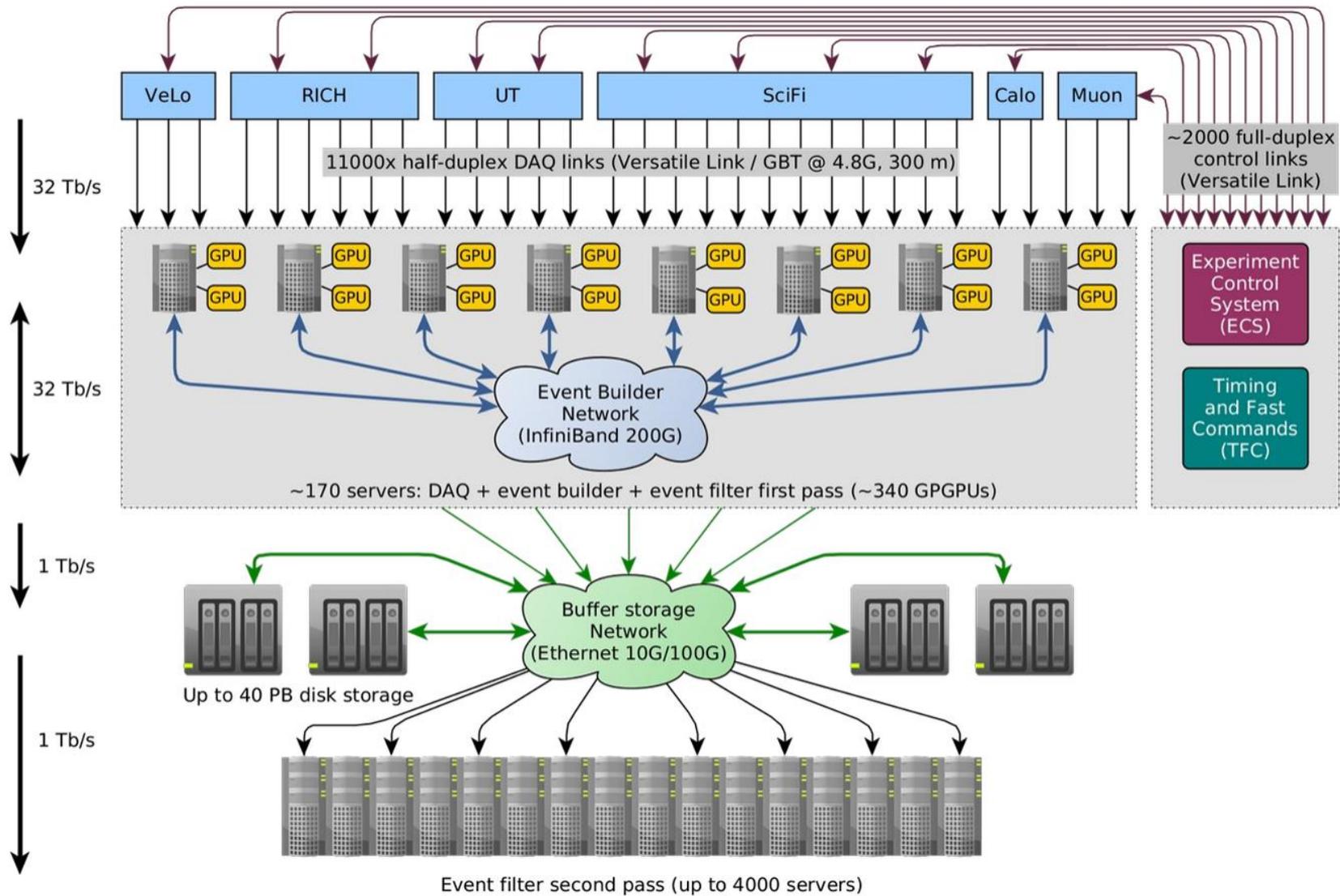
Triggerless DAQ@LHCb



p-p bunch crossing rate: 30 MHz



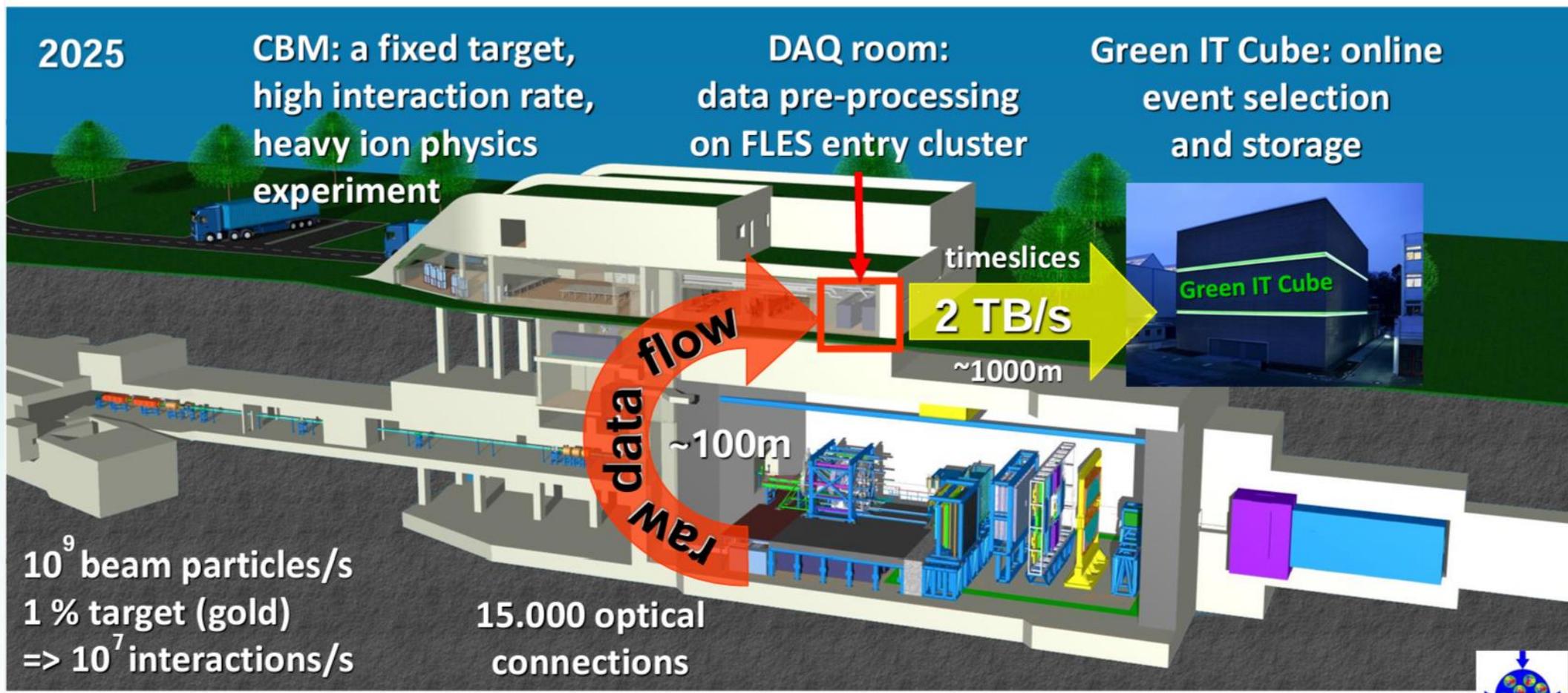
Triggerless DAQ@LHCb



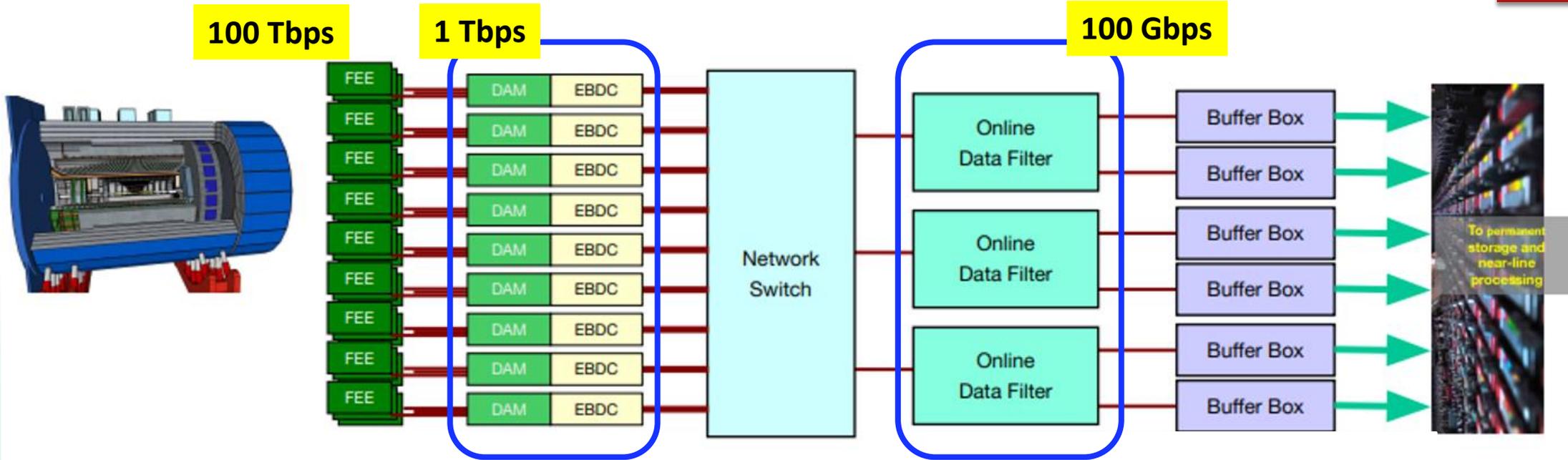
Triggerless DAQ@CBM

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The CBM data flow at SIS100



Streaming DAQ@ePIC



FELIX FLX-182 from ATLAS/Omega group at BNL
Versal Prime FPGA, PCIe Gen4x16,
24 FireFly links@25Gb/s (next version has 48 link capability)



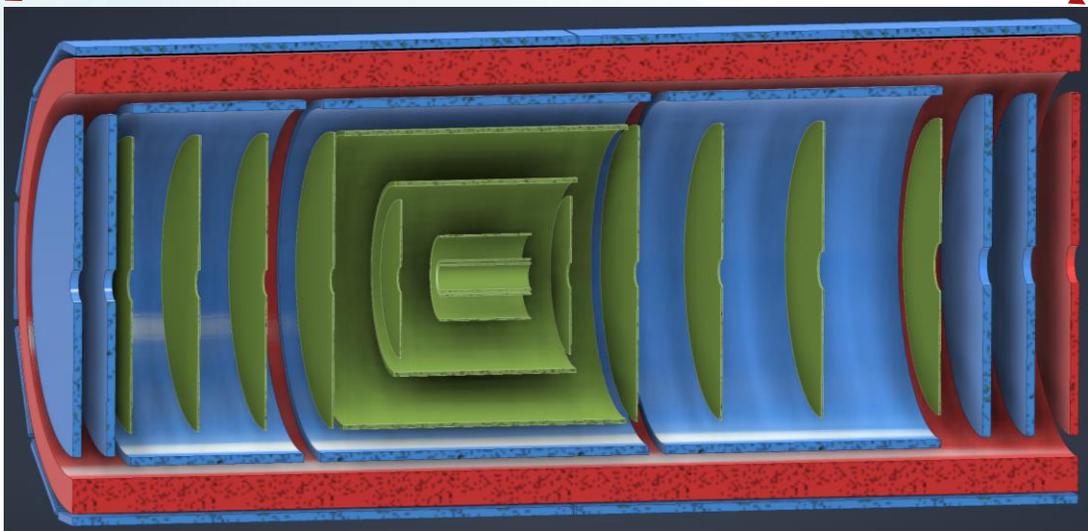
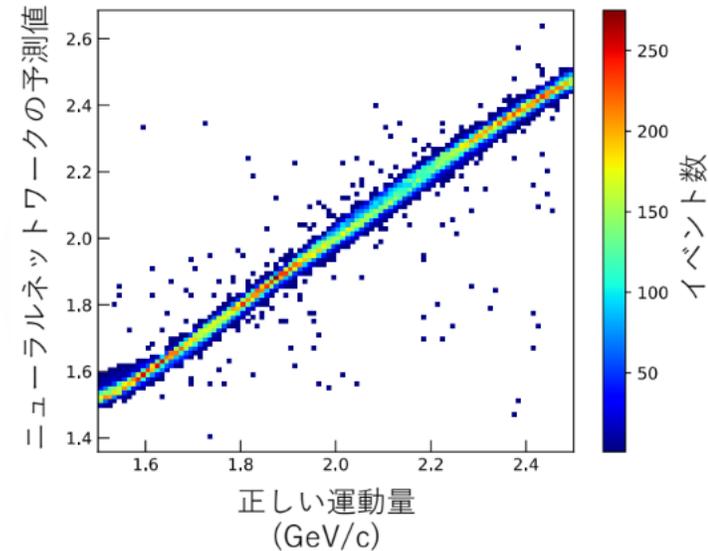
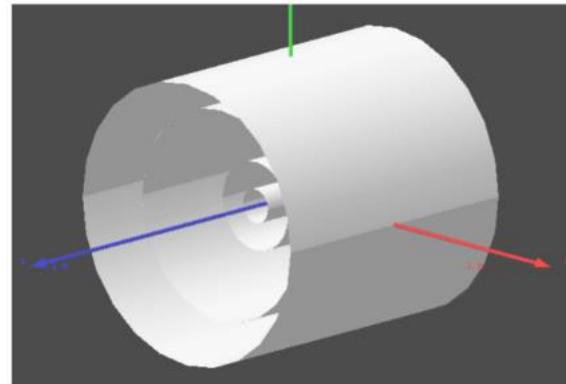
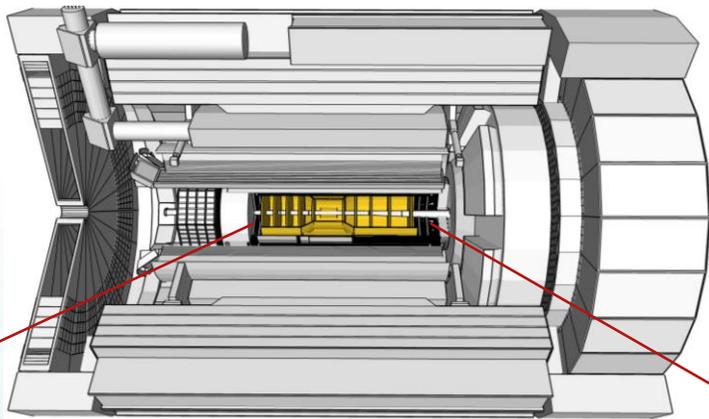
GPU-based online processing



ALICE EPN node
8 GPUs (AMD MI50/MI100)

Current activities – I for ePIC

AI/ML based-online processing on FPGA (hls4ml) for MAPS Si layers



Performance Estimates

• Timing

◦ Summary

Clock	Target	Estimated	Uncertainty
ap_clk	5.00 ns	4.258 ns	0.62 ns

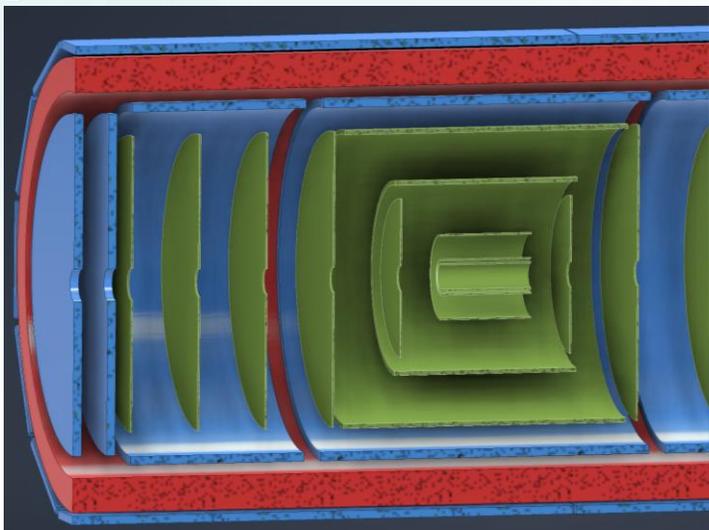
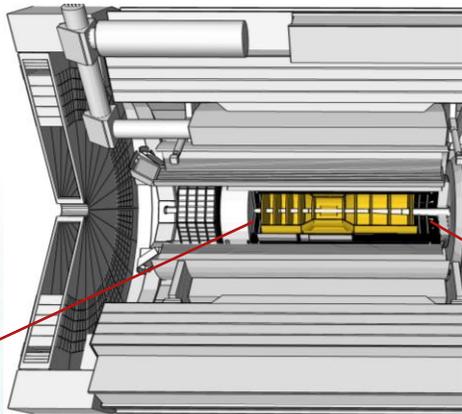
• Latency

◦ Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		Type
min	max	min	max	min	max	
4	4	20.000 ns	20.000 ns	1	1	function

Current activities – I for ePIC

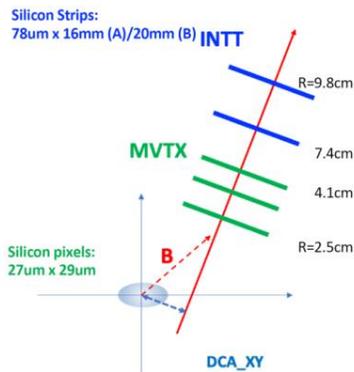
AI/ML based-online processing on FPGA (hls4ml) for MAPS Si layers



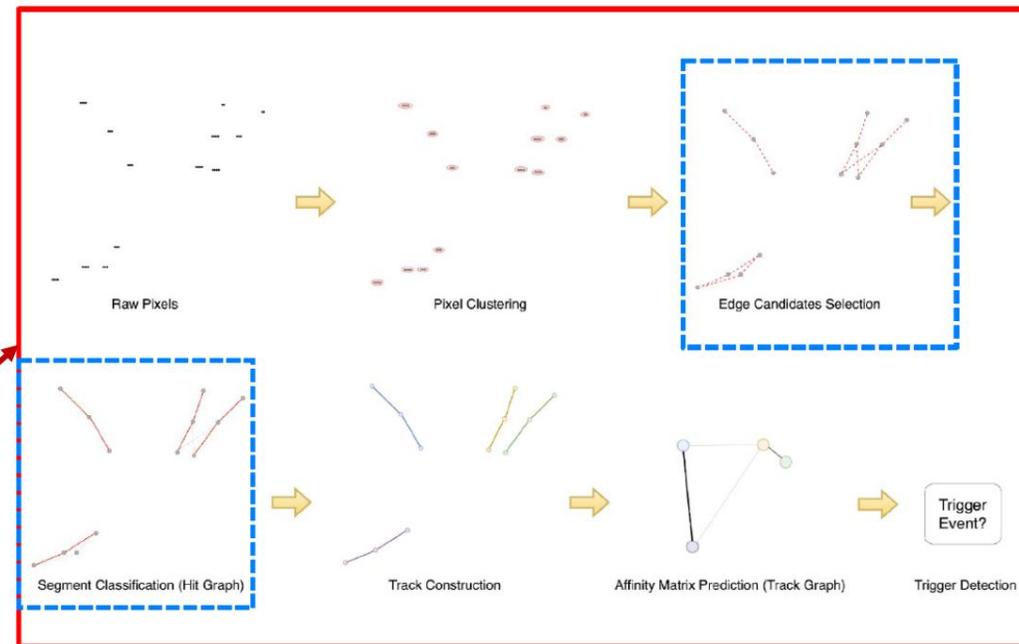
FPGA based data filter for sPHENIX and EIC

[Y. Corrales Morales, RHIC AUM 22, [link](#)]

Produce real-time selection of HF events: hit input → clustering → seeding → trak reco → displaced vertex tagger



FELIX (ATLAS/sPHENIX)



Current activities – II for ePIC

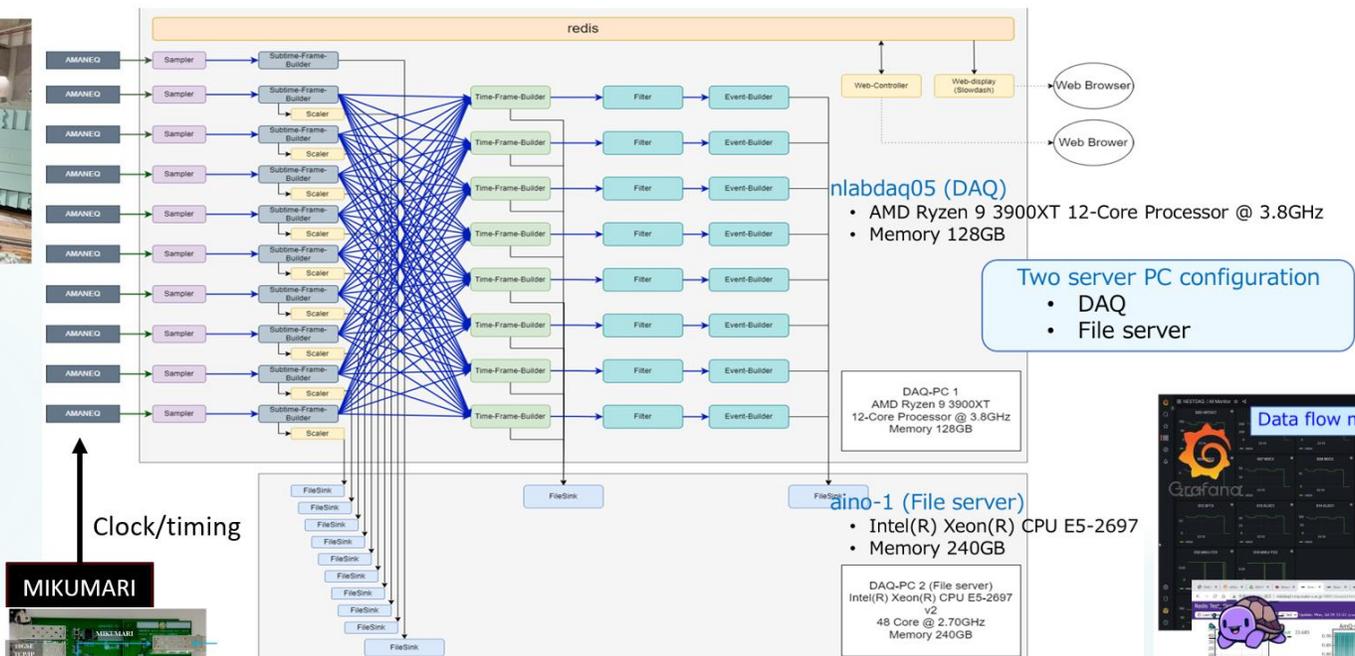
▶ SPADI-Alliance collaboration

SPADI Alliance

Signal processing and data acquisition infrastructure alliance

▶ Standardization of streaming DAQ in many facilities (RIBF, J-PARC, etc)

▶ Framework for streaming DAQ/Computing based on FairMQ and Redis



Beamtest at J-PARC
Physics run at RCNP

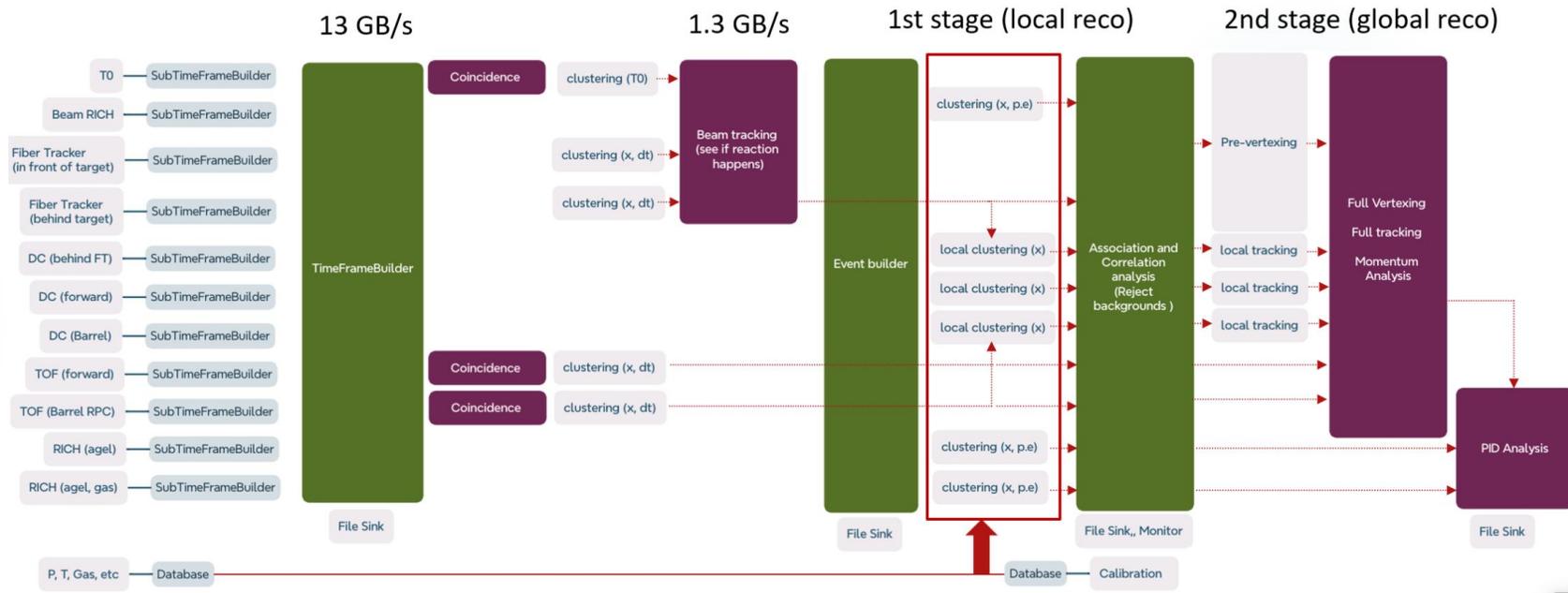
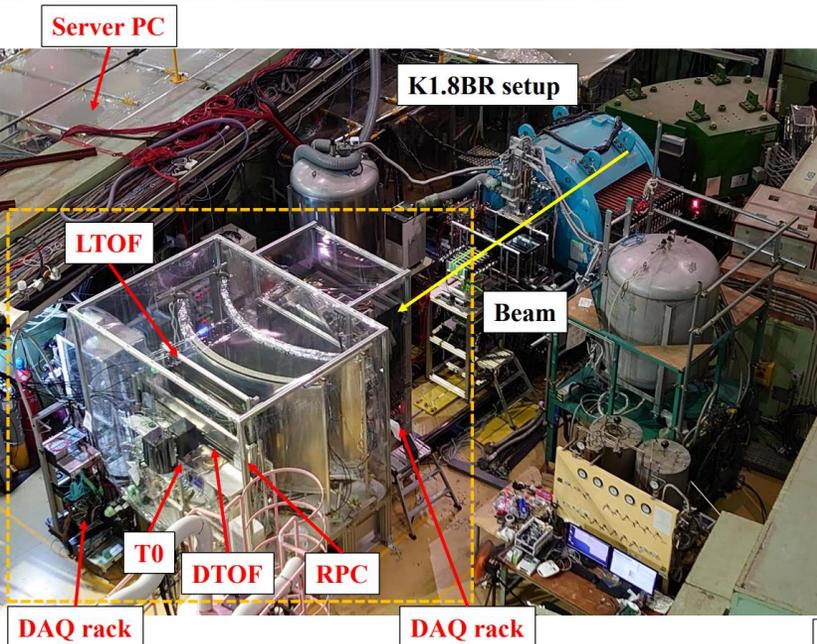
nestDAQ (network based streaming DAQ)

Using nestDAQ at JLab under discussion

Current activities – III for ePIC

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- ▶ Preparation for the beamtest of E50 at J-PARC in April and May
 - ▶ E50 could be one of the testbeds of streaming DAQ for ePIC
 - ▶ Deployment of GPU data processing



今後の予定

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- ▶ nextDAQをJlabのbeam dump experiment (dark photon search)に応用
- ▶ Timeframe data のOnline data filtering
 - ▶ DAM (Versal FPGA)でのfiltering (local reconstruction)
 - ▶ GPUでのfilterin (global reconstruction)
 - ▶ simulationによるbenchmarkingとresource estimate
- ▶ E50でのonline filteringの試験
 - ▶ E50での経験がそのままePICに活かされる (と予想)

まとめ

- ▶ **高エネルギー原子核実験の今後の基盤技術**
 - ▶ MAPS、LGAD、Streaming DAQ
- ▶ **高レートかつ高精度が必要な実験で必要になる技術**
 - ▶ あとは、高集積回路技術（インターポザー、チップレット）とデータ転送
- ▶ **一緒に共同で開発しませんか？**
 - ▶ 将来のJ-PARCでの実験に有益

Backup slide

