

# AC-LGAD TOF

### Satoshi Yano (Hiroshima University) EIC-ASIA meeting on 12/12/2024

### The ePIC detector

### ePIC is the "encapsulated" detector

### EM & Hadron Calorimeter







### Far-forward detectors





### PID detectors







- Two types of AC-LGAD TOF, BTOF and FTOF, are installed for ulletthe low-p PID
  - Complementary to the Cherenkov detectors
- BTOF covers mid-rapidity (-1.2< $\eta$ <1.6) composed of tilted 144 lacksquarestaves (288 half-staves)
  - п/К separation below 1.2 GeV/c is performed
  - Strip-type AC-LGAD sensor is used
  - It is placed at ~64 cm from the beam-pipe
- FTOF covers forward-rapidity (1.9<η<3.9), hadron going • direction
  - п/К separation below 2.5 GeV/c is performed \_\_\_\_
  - Pixel-type AC-LGAD sensor is used

## **AC-LGAD TOF in ePIC**







### **AC-LGAD for BTOF and FTOF**

- **Strip-type** sensor,  $3.2 \times 4 \text{ cm}^2$  3.2 x 2 cm<sup>2</sup> sensor size with 0.005 x 1 cm<sup>2</sup> metals with 0.05 cm pitch, is used in **BTOF** The readout metal geometry is <del>64 x 2</del> 64 x 2 and <del>256</del>124 channels in total each
- 1 ASICs are attached to each sensor with wire bonding
- **Pixel-type** AC-LGAD sensor, 1.6 x 1.6 cm<sup>2</sup> sensor size with 0.05 x 0.05 cm<sup>2</sup> metals, is used in **FTOF** The readout metal geometry is 32 x 32 and 1024 channels in total each
- 1 ASIC (2D 32x32) is attached to the one sensor









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  - \_\_\_\_\_



HPK and BNL sensors show reasonable results in both strip and pixel types with the "BEST" bias voltage

The higher performance of time resolution should be achieved when considering the electronics jitter and TO resolution

## PID performance by AC-LGAD TOF







- EICROC (32x32 = 1024ch) is one of the common ASICs used in ePIC
  - Design suits to pixel-type AC-LGAD readout (for low input capacitance) \_\_\_\_
  - 10-bit TDC and 8-bit ADC is now available (EICROC0)
- We have several options for the strip-type AC-LGAD readout
  - The strip type has a large input capacitance of ~10 pF
    - "Standard" EICROC should be modified if it is used for the strip type
  - FCFD and modified HGCROC are the candidates
    - FCFDv1 with the analog block is available and FCFDv2 with digital block will be available beginning of next year
    - HGCROC has been developed for CMS Calorimeter and is ready
    - ETROC (CMS ASIC) will be used for the coming electronics development
- It is very welcome to join the ASIC development
  - We are discussing how to collaborate with eRD109 (electronics R&D consortium)

### ASIC



Analog block

### HGCROC3

**Digital block** 

TDC

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## **Challenging points other than sensor and ASIC**

- BTOF is composed of long stave structures with a low material budget  $\sim 3\%$  X/X0 lacksquare
  - ~0.5% X/X0 material budget with 135 cm must be developed
  - We have never developed such a long and low material FPC!
  - Due to the restriction, the cooling system design flexibility is limited
- Temperature control of the sensor is one of the most challenging and important  ${\color{black}\bullet}$ points to realize BTOF
  - AC-LGAD is very sensitive to its temperature
- To avoid the acceptance hole and enhance the cooling capability, the double-• side design is the baseline
  - The procedure of assembling and construction plays a key role in enhancing the yield 135cm





135cm





## The AC-LGAD TOF collaboration and schedule

Institute	Contact Person	NOW (TDR->Project)						
Brookhaven National Laboratory	Prithwish Tribedy tribady@bnl.gov	DAQ readout chain readout, sensor-ASIC integration, sensor with FF AC-LGAD; EICROC testing						
Fermi National Accelerator	Artur Apresyan <u>Artur.Apresyan@cern.ch</u>	FCFD ASIC (no ePIC)						
OMEGA	Dominique Marchand dominique.marchand@ijclab.in2p3.fr	EICROC						
Los Alamos National Laboratory	Xuan Li <u>xuanli@lanl.gov</u>							
Rice University	Wei Li <u>wl33@rice.edu</u>	B/FTOF FEE?, Backend electronics (postdoc), simulation and reconstruction						
Oak Ridge National Laboratory	Oskar Hartbirch <u>hartbricho@ornl.gov</u>	sensor-ASIC integration, frontend electronics (waffle probing), module assembly						
Ohio State University	Daniel Brandenburg <u>Brandenburg.89@osu.edu</u>	BTOF/FTOF: module assembly; backend electronics						
Purdue University	Andreas Jung anjung@purdue.edu	Module assembly						
Univ. of California, Santa Cruz	Simone Mazza <u>simazza@ucsc.edu</u>	Sensor, sensor-ASIC integration, module assembly (no in-kind)						
University of Illinois at Chicago	Olga Evdokimov mailto:evdolga@uic.edu							
Hiroshima University	Kenta Shigaki <u>shigaki@hiroshima-u.ac.jp</u>	FTOF EICROC testing, sensor testing (30%), simulation						
RIKEN	Yuji Goto. goto@bnl.gov	BTOF: module assembly						
Shinshu University	Kentaro Kawaide <u>kawade@shinshu-u.ac.jp</u>	Sensor testing, simulations						
University of Tokyo	Taku Gunji gunji@cns.s.u-tokyo.ac.jp	DAQ streaming readout						
South China Normal University	Shuai Yang syang@scnu.edu.cn							
Univ of Sci. and Tech. of China	Yanwen Liu							
Indian Institute of Tech., Mandi	Prabhakar Palni prabhakar.palni@unigoa.ac.in	FTOF Module Assembly/QA, sensor testing						
National Inst. of Sci. Edu. Res.	Ganesh Tambave ganesh.tambave@niser.ac.in	Module Assembly						
National Central University		FF AC-LGAD (sensor QA)						
National Cheng-Kung University	Yi Yang <u>yiyang@ncku.edu.tw</u>	Mechanics and cooling systems						
National Taiwan University	Rong-Shyan Lu <u>rslu@phys.ntu.edu.tw</u>	FF AC-LGAD; module assembly						
Univ. Técnica Federico Santa María		Simulations						
LBNL	Zhenyu Ye <u>yezhenyu2003@gmail.com</u>	BTOF ASIC testing; SH						
Kent State University	Zhangbu Xu zxu22@kent.edu	Simulation, readout test, machine shop (in-kind)						
Nara	Takashi Hachiya <u>hachiya@cc.nara-wu.ac.jp</u>	BTOF module assembly/validation/FPCB						



- The schedule is based on the data-taking start • in 2032
- I am not sure, but it will be behind the schedule lacksquareby 2 years?





## **Organization of TOF-Japan**



- The Japanese community has committed to the AC-LGAD TOF project
  - Especially, we focus on the BTOF part
- Recently, Tohoku University has participated in the project officially
- The institutes are working on,
  - Simulation (background & material budget)
  - Long FPC design
  - Sensor R&D
  - Assembling & Construction
- TOF-Japan meeting (<u>link</u>) is held every Wednesday (10:00JST → 20:00EST)



## **Assembly building & Resource in Japan**

- Construction has begun on a new building to house TOF's ulletdevelopment and assembling room
  - The building is scheduled to be completed by the end of 2025
- There is one 100 m<sup>2</sup> 1,000  $\sim$  10,000 class clean room that we can ulletuse for BTOF
  - Wire bonding machine, probe station, laser system and other equipment will be installed here
- We are discussing whether to build another site at RIKEN lacksquare
  - The site will be used not only by BTOF but also by ZDC activities —
- We requested a large amount of grant for our government to ulletsucceed in the ePIC project
  - BTOF is one of the main projects in the plan (\$10s M) \_\_\_\_
  - The official conclusion will be public this December





Japan to Join Electron-Ion Collider Accelerator **Construction Project; Potential Boost for Quantum Computer Technology** 



Japan will participate in a U.S. project to build a large electron-ion collider (EIC), a particle accelerator capable of observing the world at the level of one trillionth of a millimeter, it has been learned.

The EIC is expected to shed new light on the physical laws governing the subatomic world and contribute to the practical application of advanced technologies such as quantum computers.

The Education, Culture, Sports, Science and Technology Ministry plans to announce soon its intention to participate in the plan, with the goal of starting operations in 2032.

The state-of-the-art EIC accelerator, a circular experimental facility about 3.8 kilometers in rcumference, will be built by Brookhaven National Laboratory (BNL) in New York, part of the U.S. Department of Energy.

BNL plans to replace the existing accelerator in the basement of the building. Construction is scheduled to begin in 2026, with operations beginning in 2032.









- Takashi Hachiya (NWU) is working on the FPC design •
  - FPC design is still difficult despite relaxed conditions
  - The first one is designed with ETROC2
- We visited HAYASHI-REPIC CO. Ltd. to discuss how to cooperate with the lacksquareAC-LGAD TOF project
  - The company made the long & low material FPC of sPHENIX
  - The mass production of the ATLAS Strip tracker for the upgrade is ongoing
- We are planning to have a meeting with HPK engineers next week •
  - The strategy for the coming sensor production will be discussed
- We are preparing the test beam at Tohoku University lacksquare
  - Masashi Kaneta (Tohoku University) plays a key role in the test

### **Other items**

### BEX

- Cable design (prototype)
- Dimension (L x W): 120 x 5 cm<sup>2</sup>
- 4 layers (signal , 2xGND, PWR):  $X = 0.8\% X_0$ • Cu : 12um thick per layer + 30 um Cu plating on surface
- Lines : 124 lines (Line and space : 130 & 130 um)
- $Z_{diff}$ : 100 $\Omega$  by strip line structure • Signal layer is sandwiched by GND layers
- Liquid Crystal Polymer (LCP) as substrate
- Less signal loss due to low di-electric constant &  $tan(\delta)$
- Thick LCP available for Z<sub>diff</sub>: 100um









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- AC-LGAD TOF is an important PID doctor for low-p region at mid and forward rapidity
- BTOF uses the strip type, and FTOF uses the pixel-type sensor
  The covering area of BTOF and FTOF is 12 m<sup>2</sup> and 1.1 m<sup>2</sup>, respectively
- The spatial resolution is already above the requirement, but the higher timing resolution is necessary to get 35 ps timing resolution with the whole system
- Tohoku University has joined the project and they play in very important role in the coming test beam in Japan
- Our government decision for the grant is about to be public soon (this month)



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