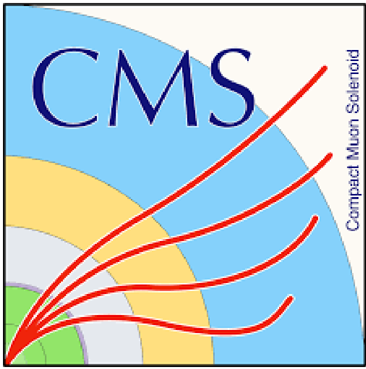


R&D of ToF - status in Korea

CHANG-SEONG MOON

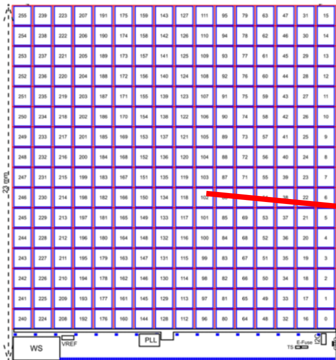
CENTRE FOR HIGH ENERGY PHYSICS (CHEP), KYUNGPOOK NATIONAL UNIVERSITY (KNU)

CMS - MTD Endcap Timing Layer (ETL)

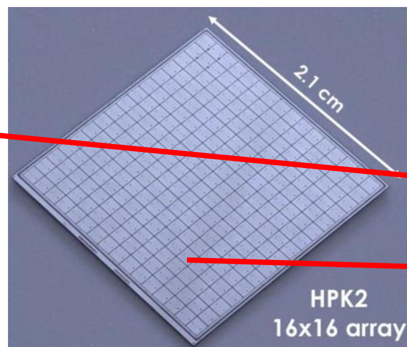
- Two double- sided disks for each side
  - Maximize geometrical acceptance (85% per disk)
  - Coverage : 1.6 < |η| < 3.0
  - Average of 1.8 hits per track
  - **Time resolution per track < 35 ps**
    - based on single hit resolution < 50 ps
- Low-Gain Avalanche Diode (LGAD) sensor bump bonded readout ASIC (ETROC)

7330 sensors
for each disk (905 kCHF)
-> 123 CHF per sensor

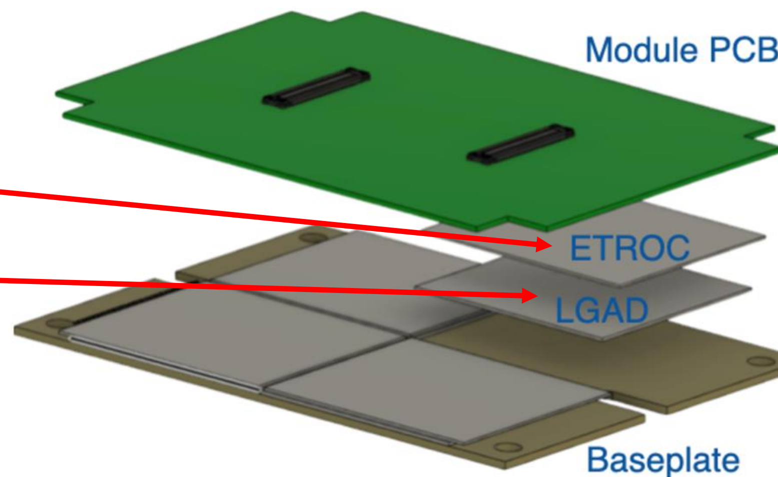
8000 modules (4 sensors each)

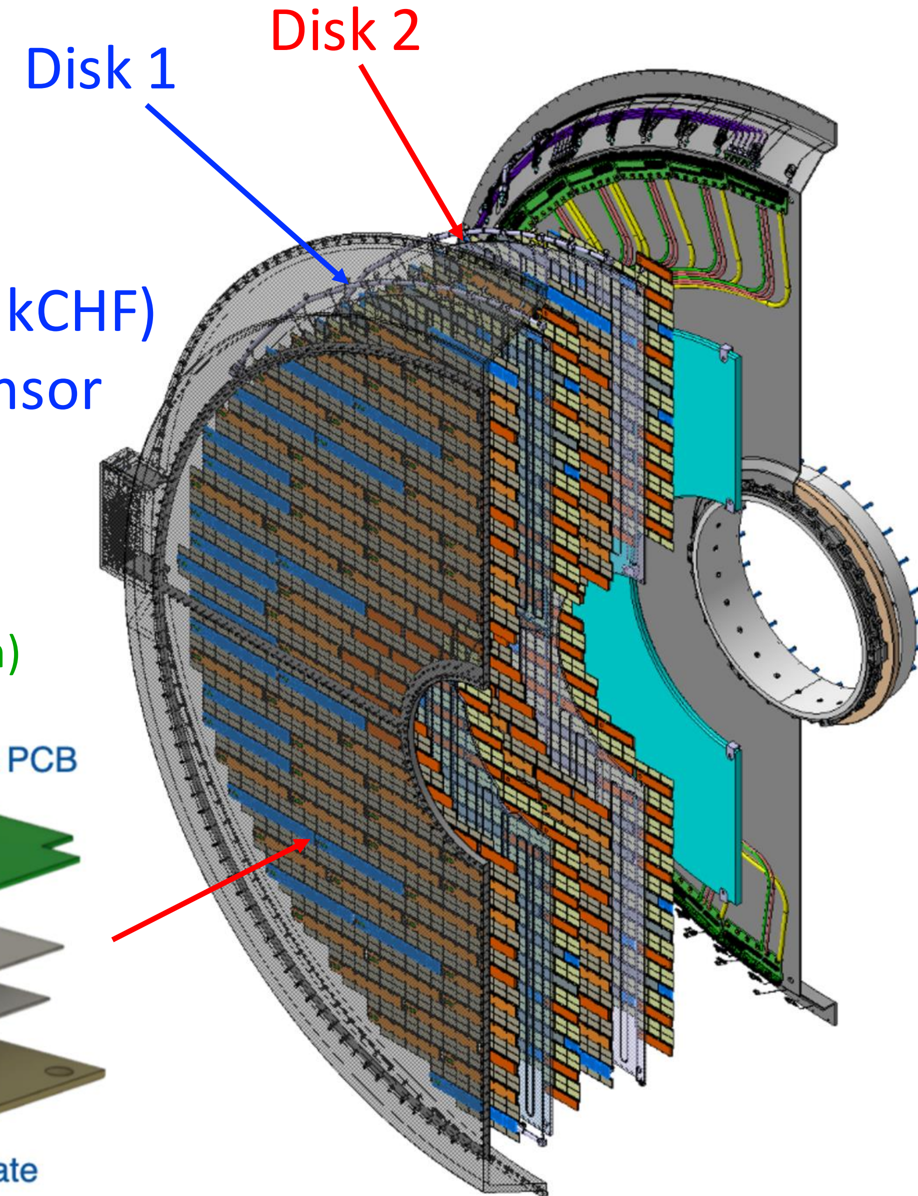


ETROC
(ASIC Chip)



LGAD sensor



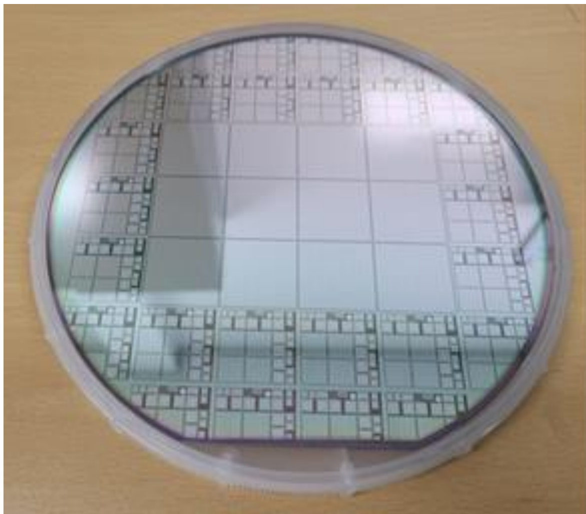


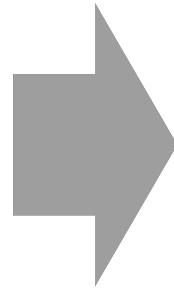
31.5 cm < radius < 120 cm

UFSD-K1, UFSD-K1 wafers from FBK in Italy

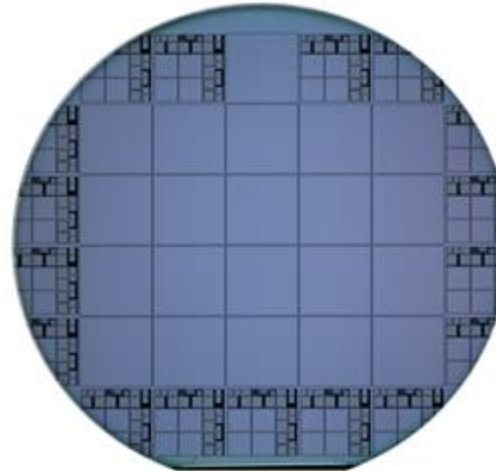
- The UFSD-K1 and UFSD-K2 are the latest version of UFSD (Ultra-Fast Silicon Detectors) ordered from Korea.
- Fifteen number of UFSD-K1 wafers manufactured by two different wafer suppliers have been delivered to KNU.
- Wafer-level test of the UFSD-K1, K2 is done to measure performance.

UFSD4





UFSD-K1



Increased the number of 16X16 arrays from 12 to 21.

Finalized gain layer design to shallow type.

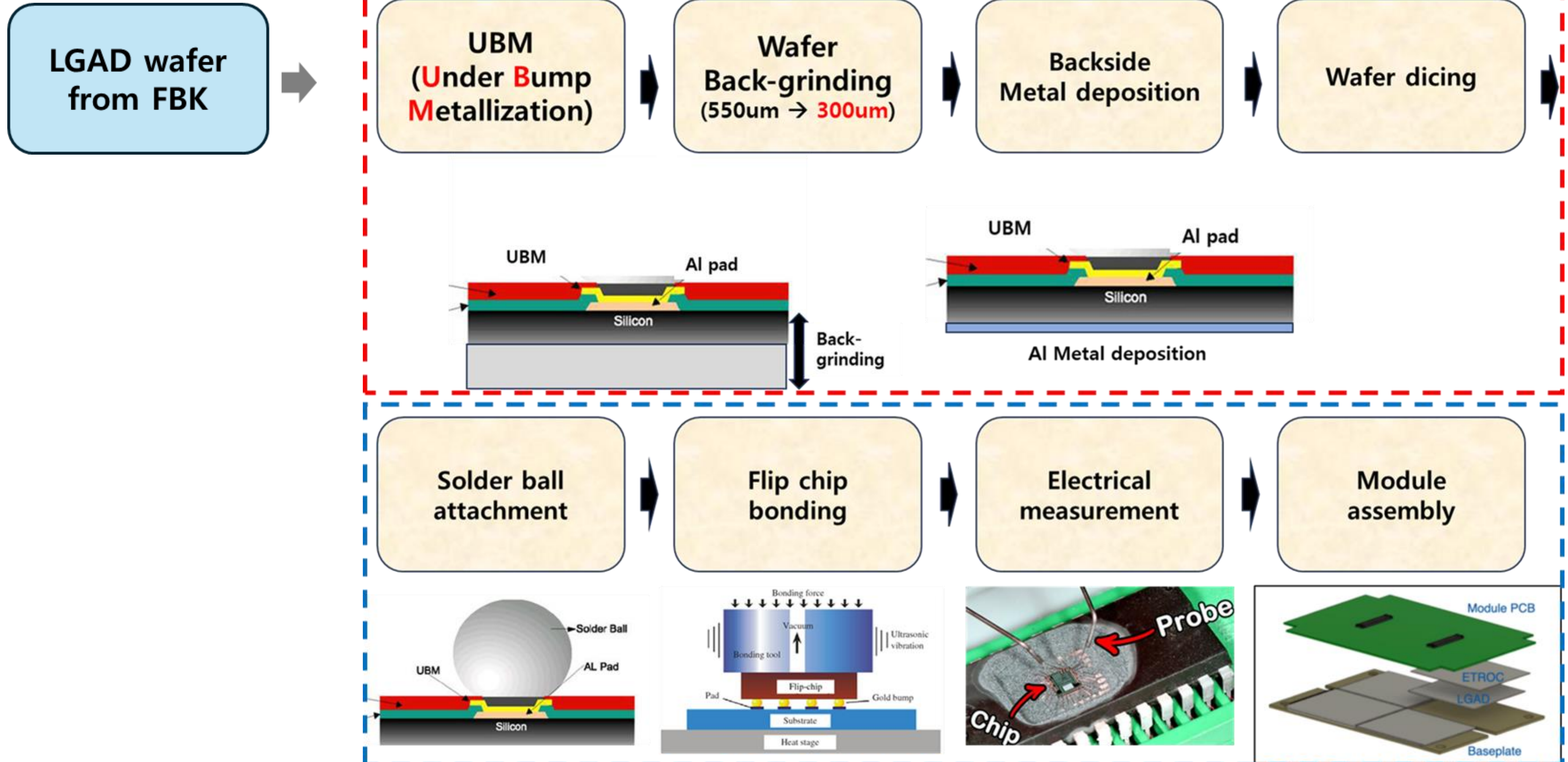
UFSD-K1

WAFER #	W LABEL	SUB. SUPPL.	CARBON	PGAIN DOSE
1	AA9	STD SUPPLIER	0.8 - Litho - CHBL	1.00
2	GB1	NEW SUPPLIER	0.8 - Litho	1.00
3	GB2	NEW SUPPLIER	0.8 - Litho	1.00
4	GB3	NEW SUPPLIER	0.8 - Litho	1.00
5	AA10	STD SUPPLIER	0.8 - Litho	0.98
6	GB4	NEW SUPPLIER	0.8 - Litho	0.98
7	GB5	NEW SUPPLIER	0.8 - Litho	0.98
8	GB6	NEW SUPPLIER	0.8 - Litho	0.98
9	AA1	STD SUPPLIER	0.8 Spray	0.98
10	GA17	NEW SUPPLIER	0.8 Spray	0.98
11	GA18	NEW SUPPLIER	0.8 Spray	0.98
12	GA19	NEW SUPPLIER	0.8 Spray	0.98
13	AA2	STD SUPPLIER	0.8 Spray	1.00
14	GA20	NEW SUPPLIER	0.8 Spray	1.00
15	GA21	NEW SUPPLIER	0.8 Spray	1.00
16	GA22	NEW SUPPLIER	0.8 Spray	1.00
17	GB7	NEW SUPPLIER		4 HBA
18	GB8	NEW SUPPLIER		5 HBA

UFSD4 # 14

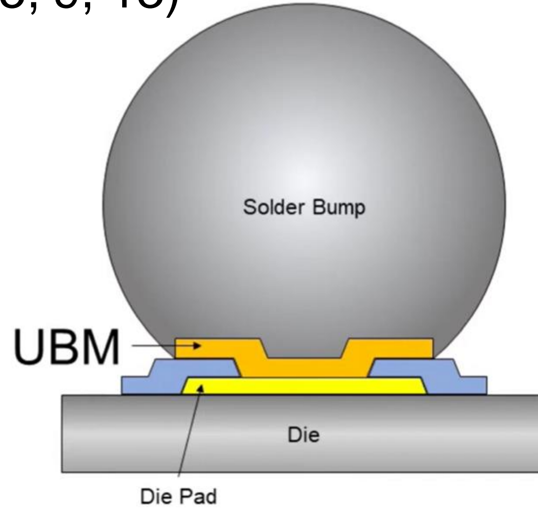
Wafer #	DI	Gain Layer Dose	Carbon	Diffusion
14	Deep	0.77	0.6	CL-BL

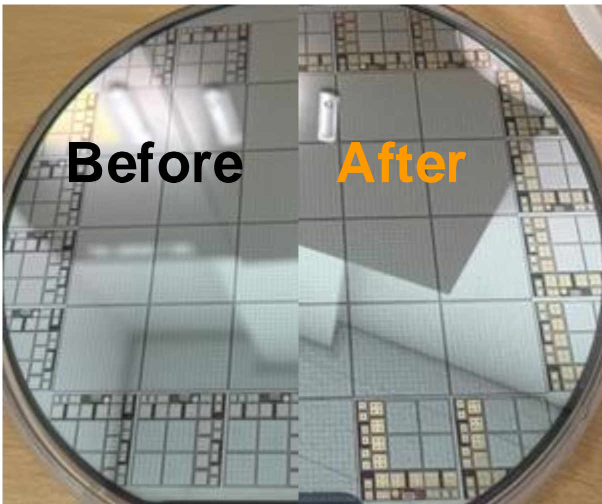
LGAD wafer post-processing procedure in Korea



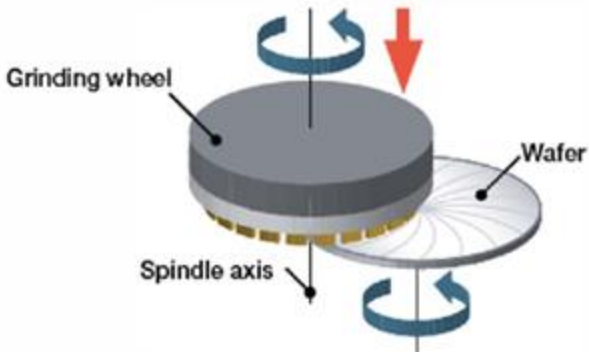
Wafer post-processing status in Korea

- Vendors from korea completed post-processing and delivered to KNU.
    - Total 5 UFSD-K1 wafers
        - UFSD-K1 standard supplier wafers(# 1, 5, 9, 13)
        - One new supplier wafer (# 6)
    - One UFSD4 No. 14 wafer
- UBM process proceeds with electroless plating
    - Thin film metal layer (Ni/Au) stack
- Backgrinding thickness = 300 μm
- Al used for backside metalization
- Dicing done with 16x16 sensor size (21mm x 21mm)

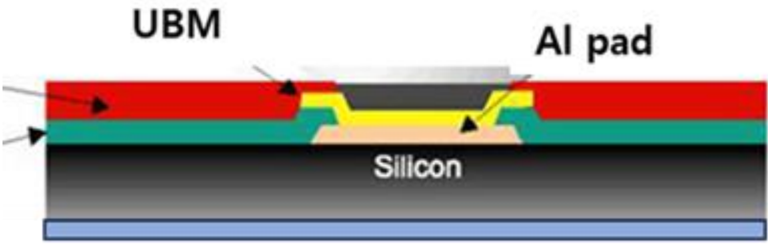




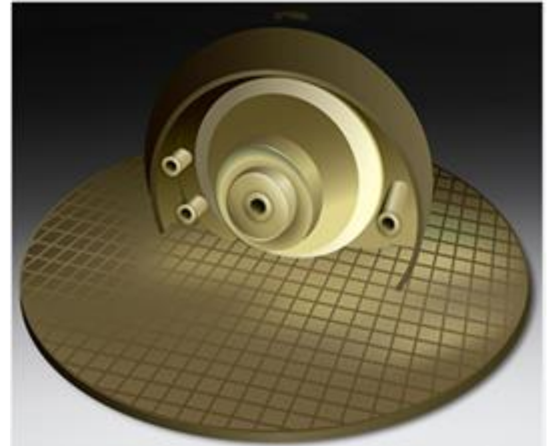
1) UBM before & after



2) Backgrinding



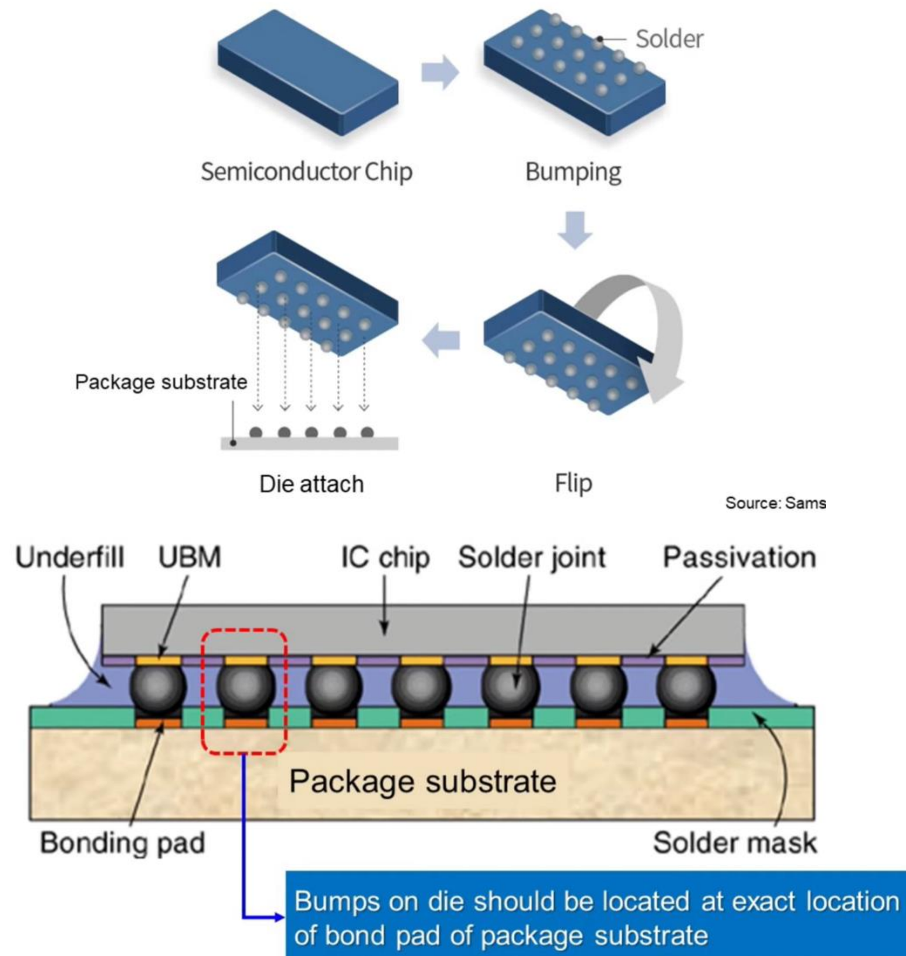
3) Al backside metalization



4) Dicing

bump-bonding / Flip-chip bonding process

- **Bump/Flip-Chip Bonding is a process that creates a bump on the chip to make an electrical/mechanical connection with the chip/substrate.**



Bump bonding test with 16x16 LGAD (UFSD-K1) and ETROC2

Preparation of 16x16 LGAD array sensor (UFSD-K1)

- All silicon post-processing is conducted in Korea

LGAD wafer fabricated from foundry company

1) UBM process using electroless plating

1) Preparation for UBM on LGAD Al pad

2) Zincation for good electroless plating

3) Au/Ni layer formation by electroless plating

Solder bumping site

[Photo image and a part design of 16x16 array LGAD sensor]

2) Wafer back-grinding for wafer thinning

3) Al metallization on LGAD backside

4) LGAD wafer dicing

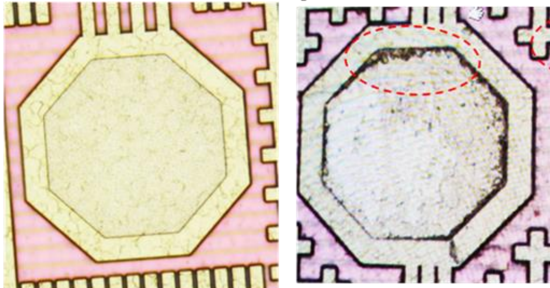
[Diced wafer]

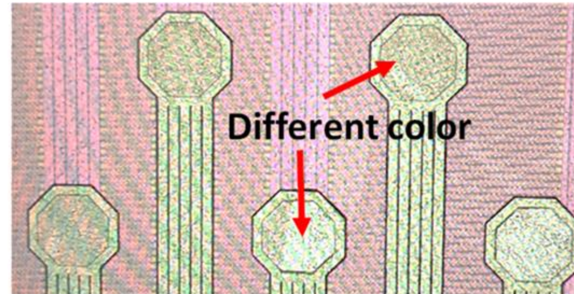
Preparation of ETROC2 chip for bump bonding

- Step 1 : The ETROC2 chips (N60R80) received from CERN
  The surface of the chips was not so good condition.
- Step 2 : Rework (cleaning) of the ETROC2 chips for UBM and bump bonding

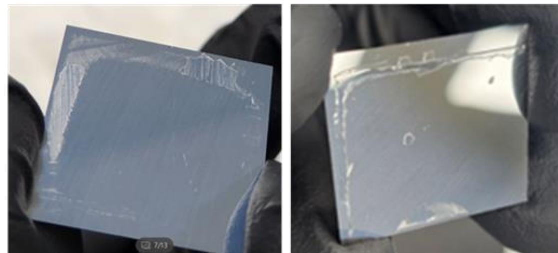
As received ETROC2

Non-uniform Al pad condition

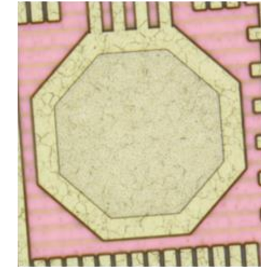




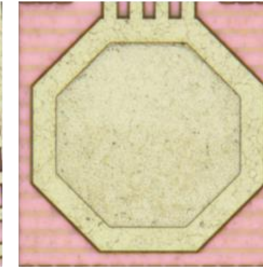
ETROC2 backside surface



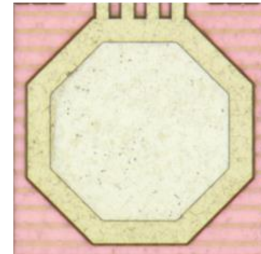
Case. 1



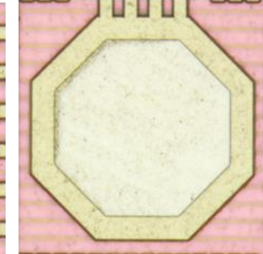
Case. 2



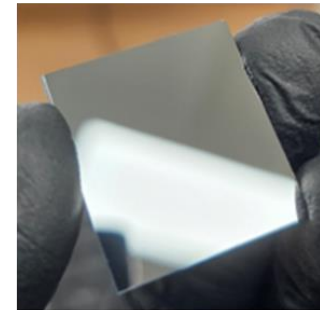
Case. 3



Case. 4



After plasma cleaning and solvent cleaning, the surface condition was still not uniform.



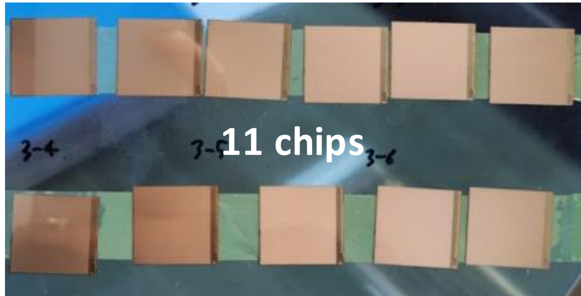
After back-grinding (~10μm)

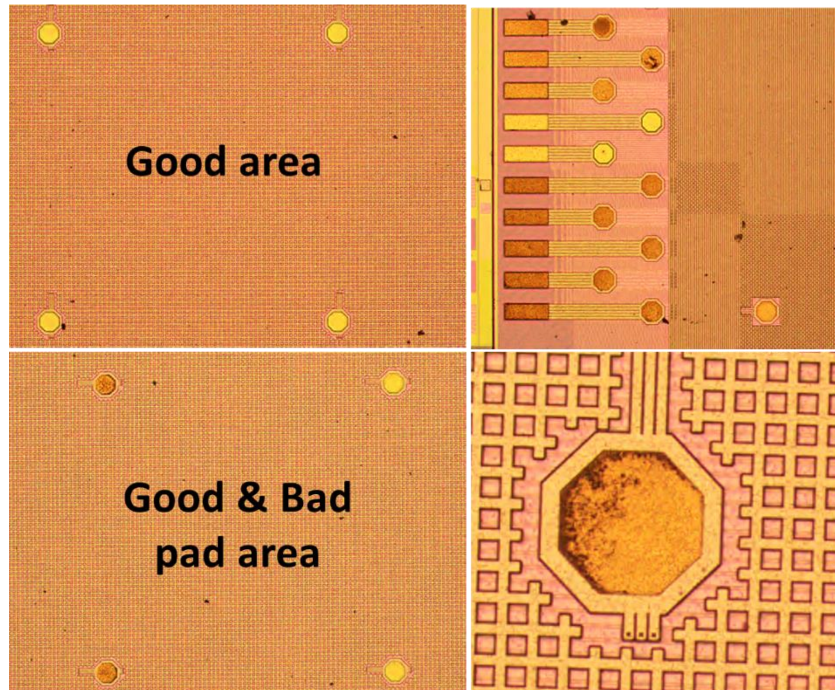
Preparation of ETROC2 chip for bump bonding

- Step 3 : The UBM process is conducted by two Korean vendors.

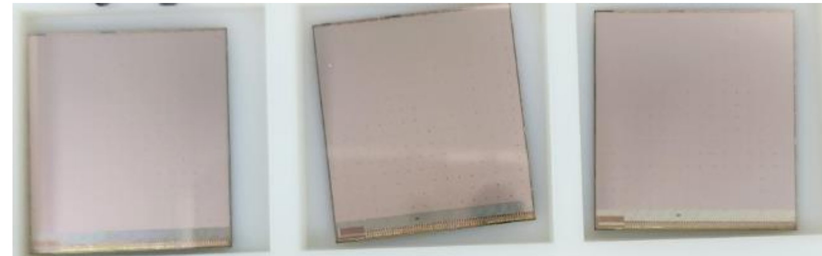
Vendor 1.
MK Chem & Tech
(Main vendor)

Same UBM process conditions for LGAD: **No tuning**

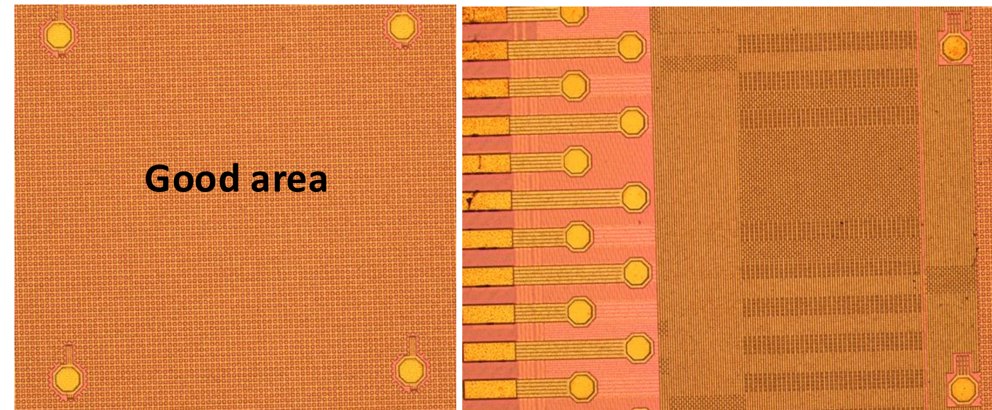




3 chips



Vendor 2.
Wiz flatform
(New vendor)

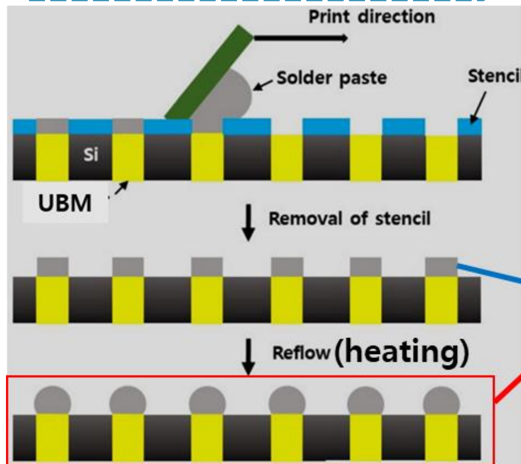


By tuning the UBM process conditions to match ETROC2, most pads successfully formed Au/Ni layers.

Solder bumping on LGAD (USFD-K1) & bump bonding

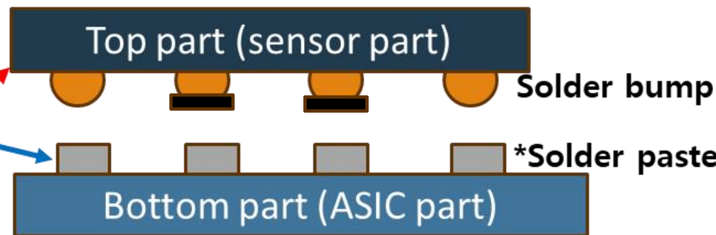
- Solder bumping & Bump-bonding process (at Hansol Semiconductor)

1) Solder bump formation on sensor chip

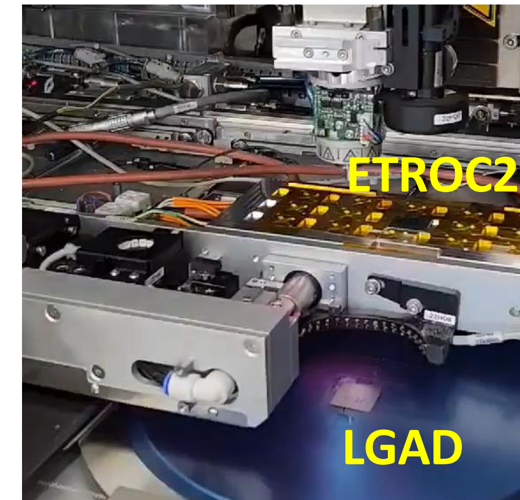


2) Solder paste printing on ETROC2 chip

*Solder paste, with its slight stickiness, temporarily holds the solder bumps in place until soldering is completed.

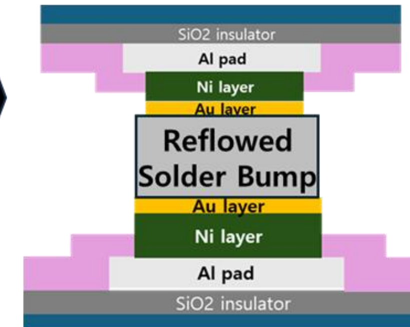


3) Bump-bonding using flip-chip bonder (~10 sec/1sample)



4) Solder reflow process for bump solidification

5) End of bump bonding process



Bump bonded samples with LGAD & ETROC2

- We were able to successfully obtain 10 samples.

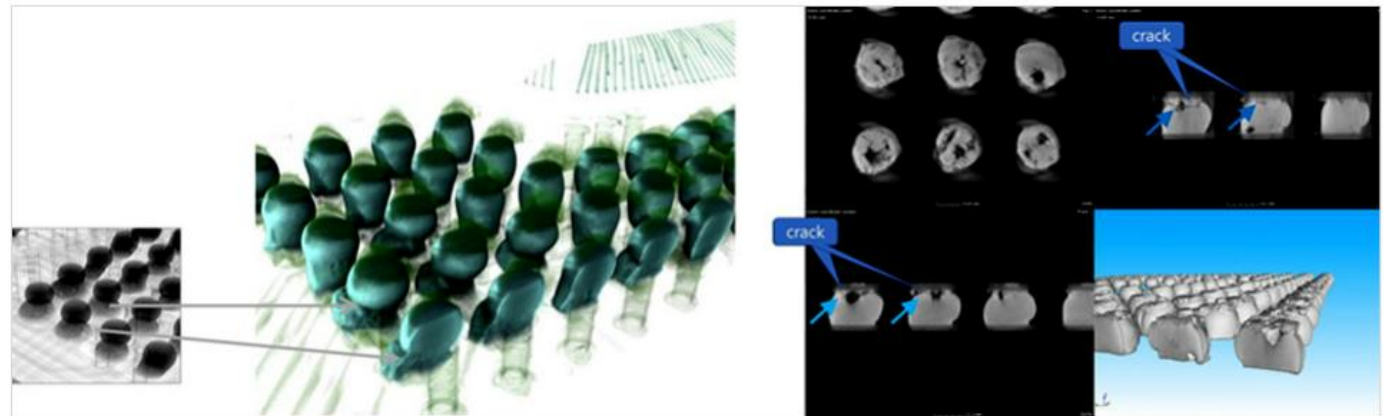
: Four samples were mis-aligned and broken during the bumping or bump bonding process

We learned a lot of know-how how to handle the thin sensors and chips from the process.

- 10 samples are ready to test
  - Some will undergo non-destructive analysis (3D CT)
  - Plan to do the beta ray test based on the system test setup at KNU
  - Mechanical test (Shear strength test)
  - Few of them can be shared to other groups (Boston etc.) for testing.

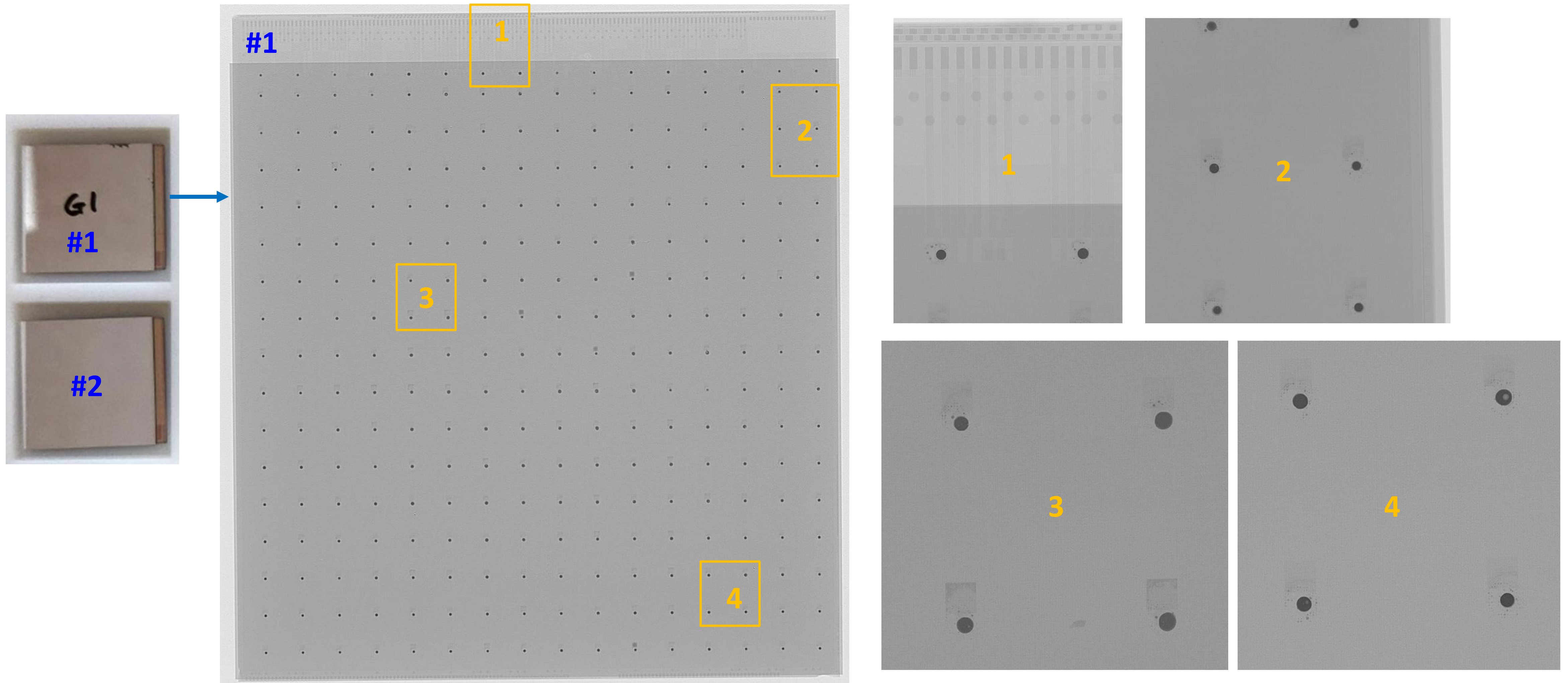
The G1, G2 samples were fabricated using ETROC2 processed by Vendor 2 (Wiz flatform) for UBM.

[Example of solder ball with 3D CT or X-ray analysis]



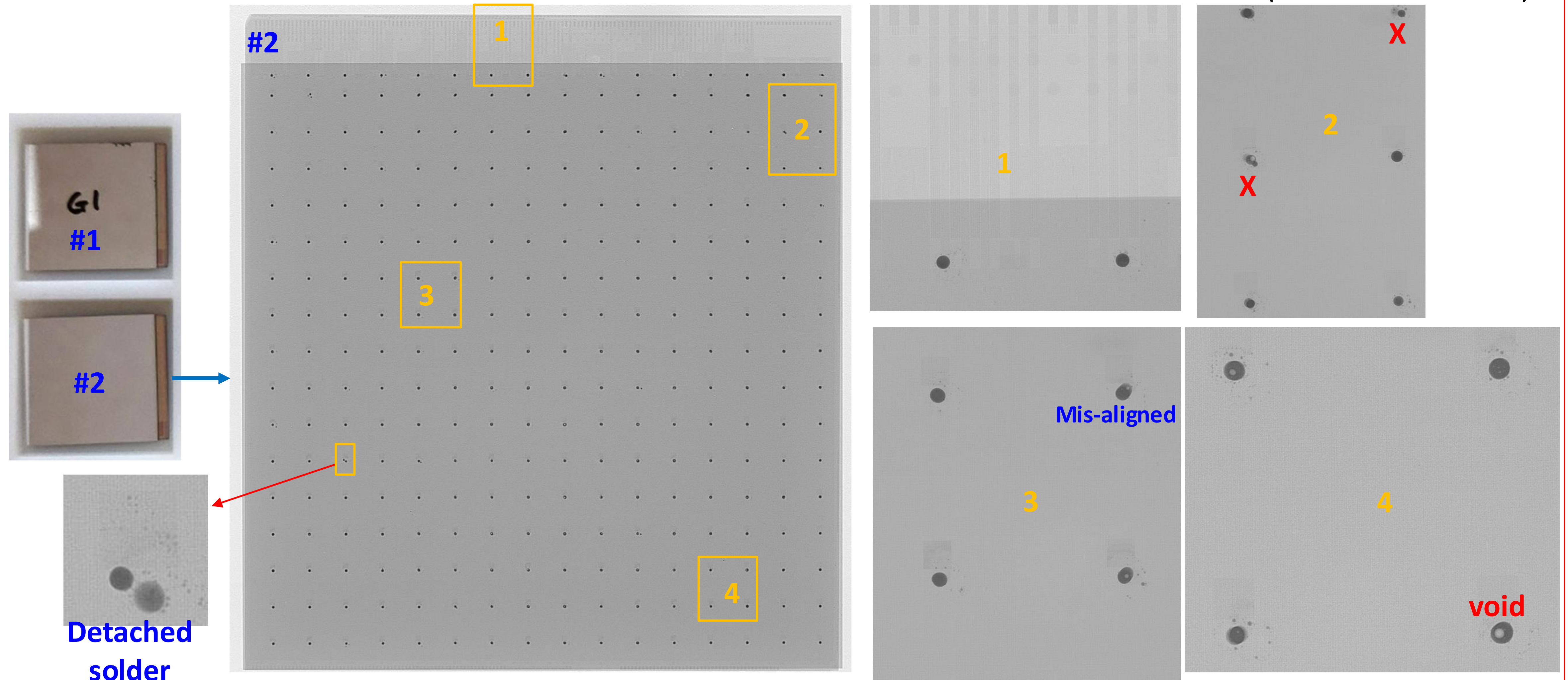
2D X-ray test for Bump bonded sample #1

- Non-destructive 2D X-ray analysis of bump bonded samples (#1)
  - Most of the bump bonding alignments appear to be well done. **(UBM done in Wiz platform)**



2D X-ray test for Bump bonded sample #2

- Non-destructive 2D X-ray analysis of bump bonded samples (#2) : Not good results
  - Many bumps were not formed in the correct positions: the reason due to the poor ETROC2 UBM (MK Chem & Tech)



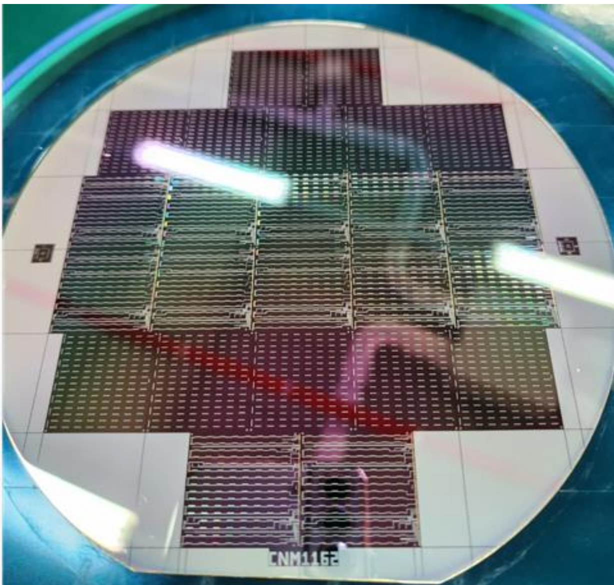
Fabrication of dummy wafer for bump bonding process yield test

Fabrication of dummy wafer for bump bonding test

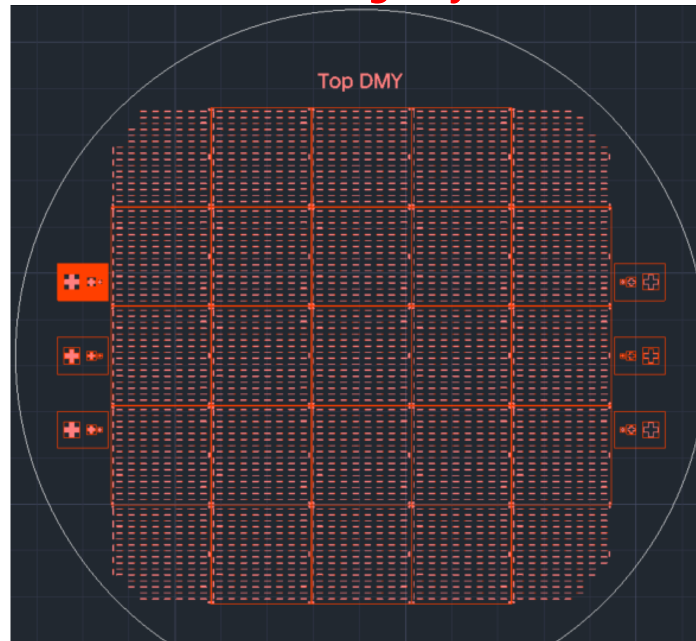
I designed the dummy wafers by myself and fabricated them at the ETRI fab in Korea.

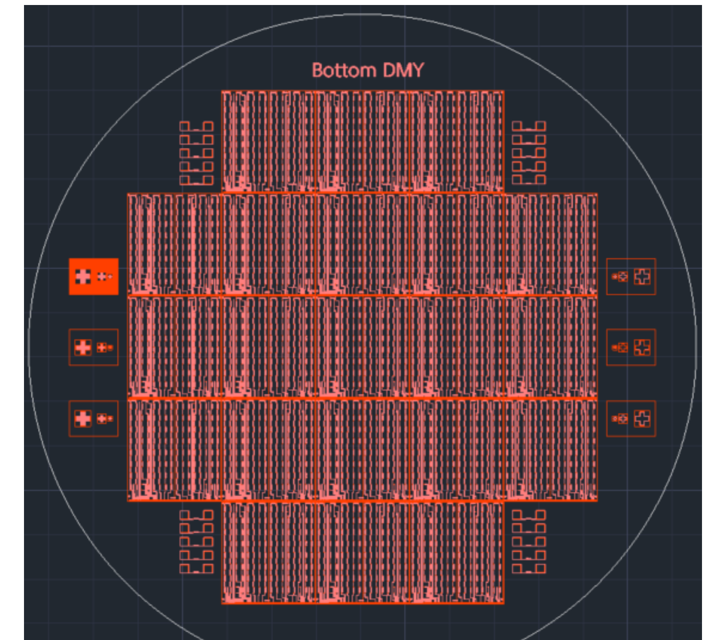
- To verify the yield of the bump bonding process on a large scale.
- The dummy wafers have different sizes for the top and bottom parts compared to the Kansas University wafers.
  - To facilitate the dicing process.
  - Therefore, we made separate photomasks for the top and bottom parts.
- Each wafer consists of 21 main chips and test patterns on the wafer.

6 inch wafer image of the Univ. of Kansas



6 inch wafer design by KCMS team for dummy wafer fabrication in Korea

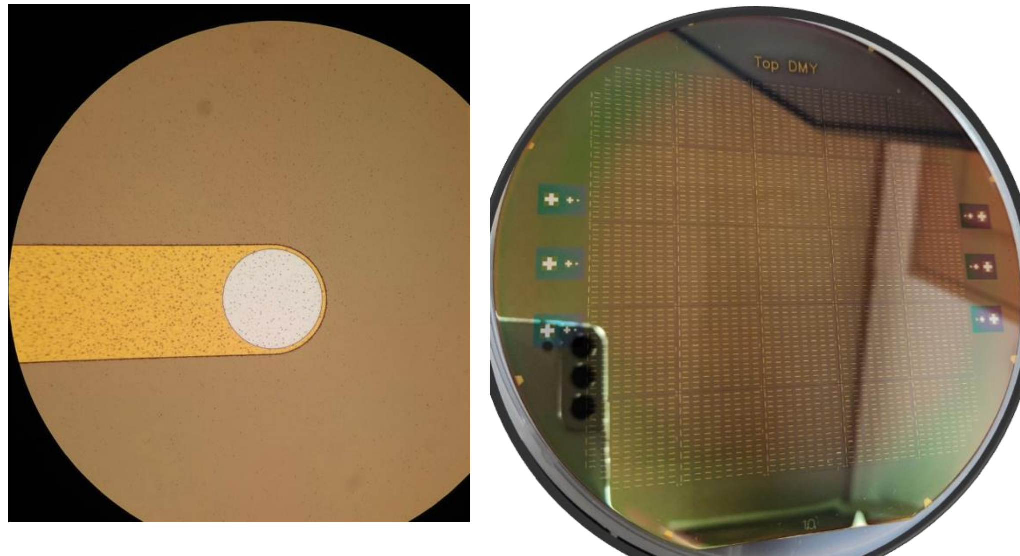


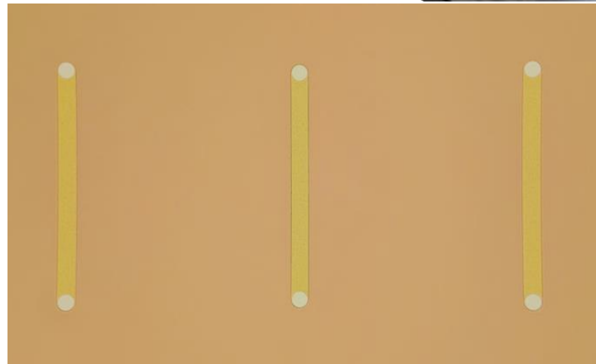


Quality test for the fabrication of dummy wafers

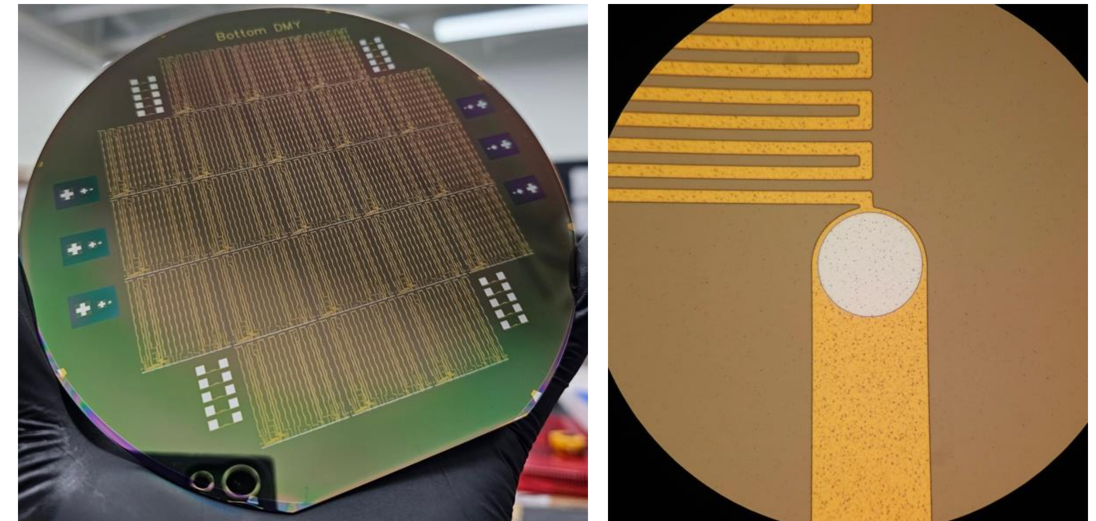
- We produced five wafers each for the top and bottom parts.
  - ❑ All wafers were fabricated at the ETRI fab center in Korea

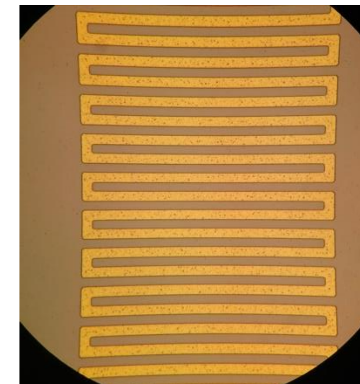
5 Top dummy wafers for LGAD pattern

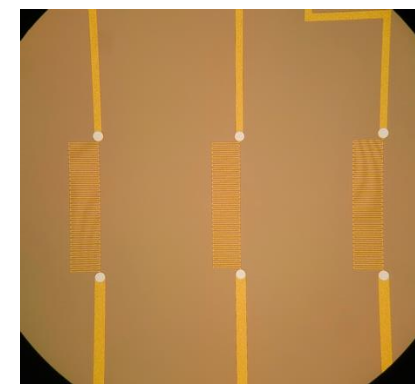




5 Bottom dummy wafers for ETROC2 pattern

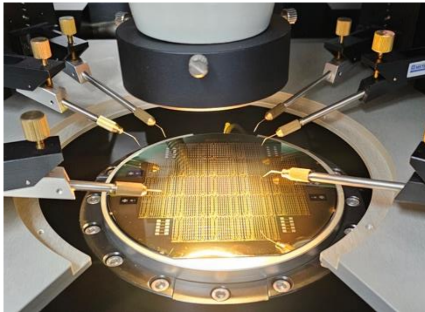




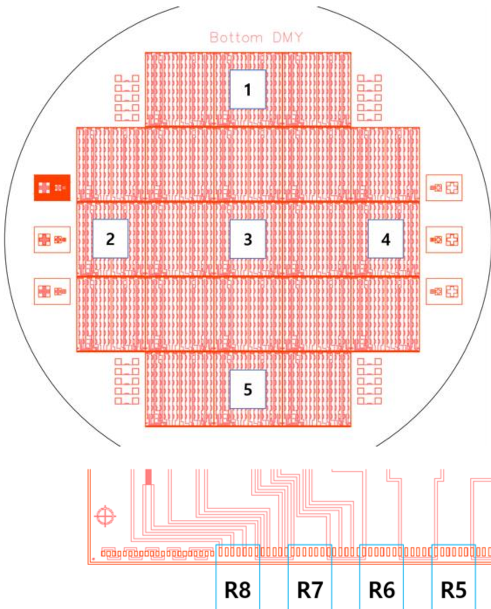


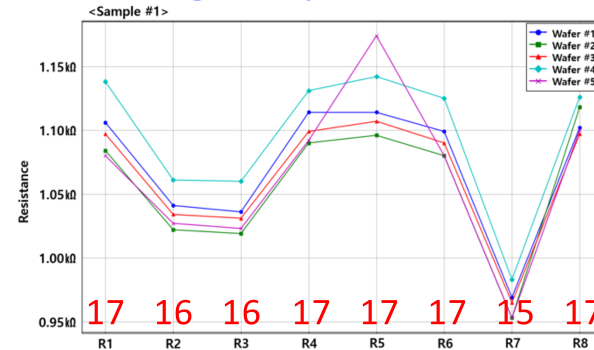
Resistance measurement with bottom dummy

- Selected 5 locations on 5 bottom dummy wafers and, measured the resistance of 8 resistance pattern groups.

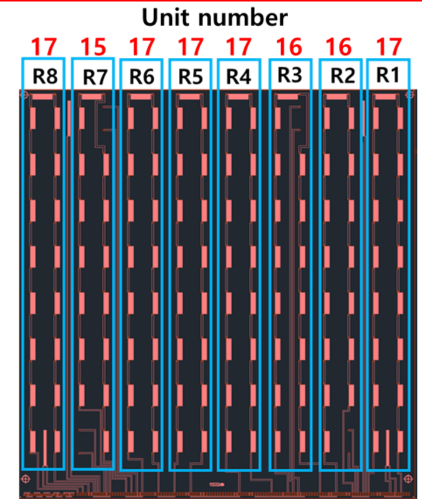


Confirmed uniform resistance values on 5 wafers

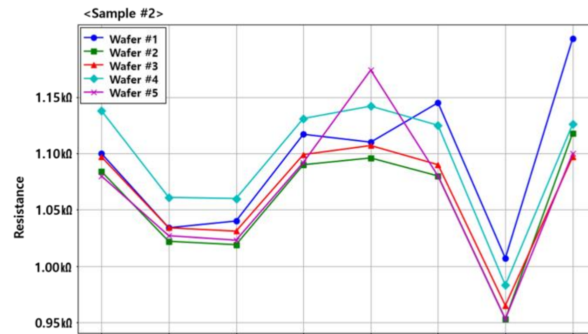




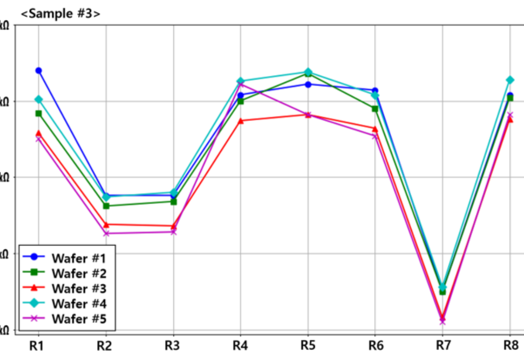
17 16 16 17 17 17 15 17 units

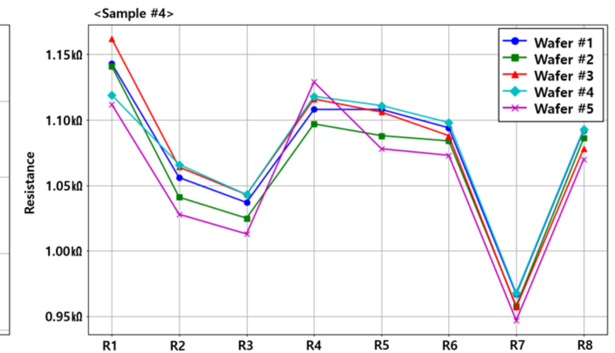


Bottom dummy design

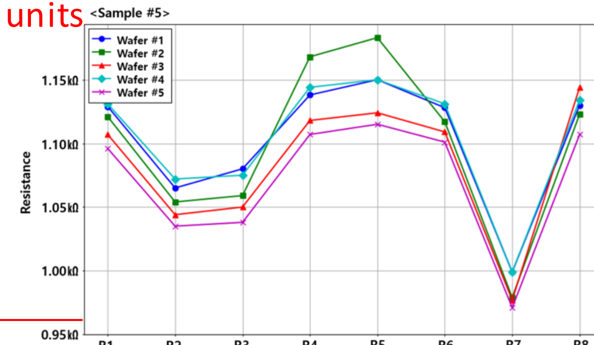


17 16 16 17 17 17 15 17 units





17 16 16 17 17 17 15 17 units



Plan for yield test of dummy wafers

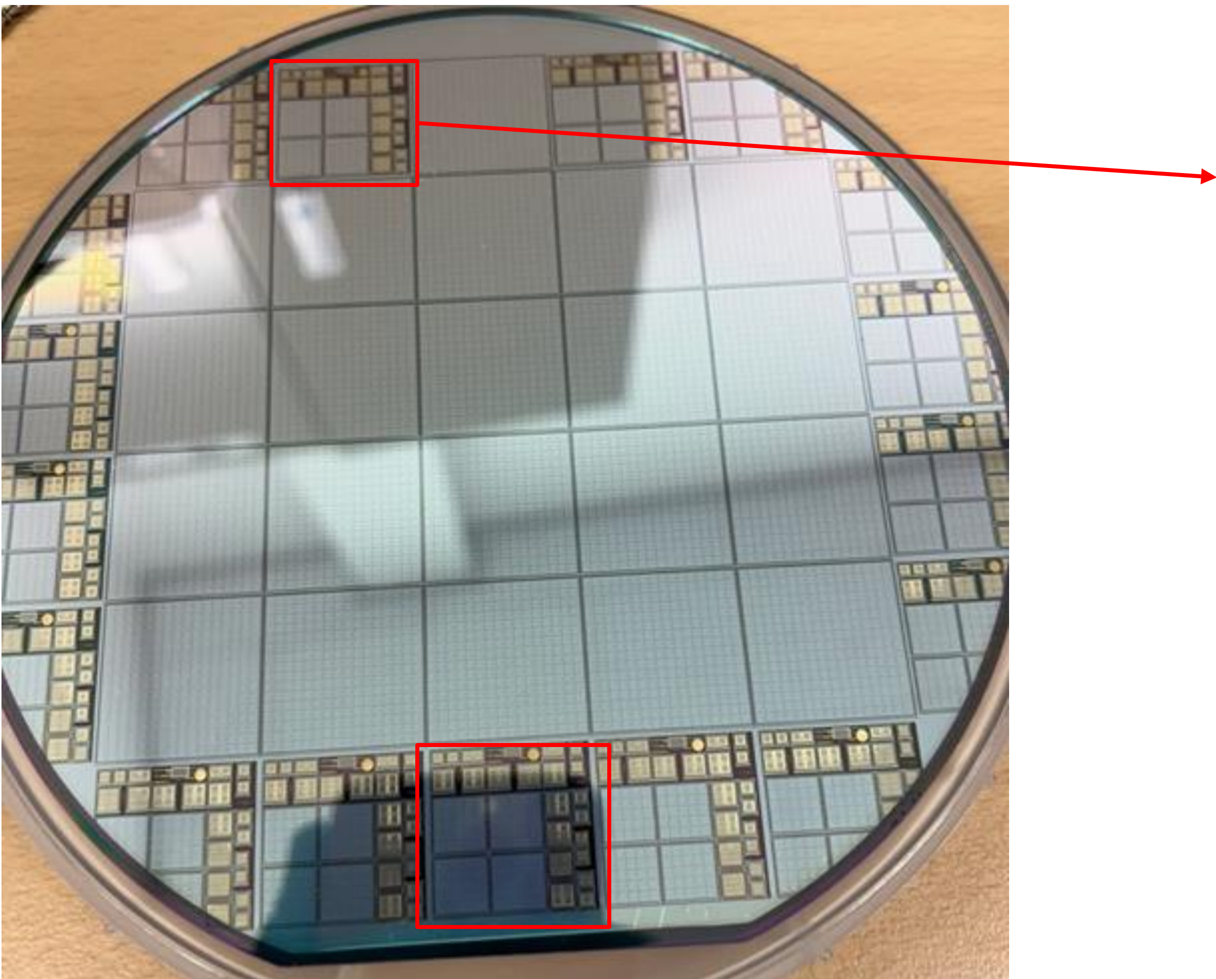
Due to the Christmas and year-end holidays, we plan to complete it by mid-January 2025.

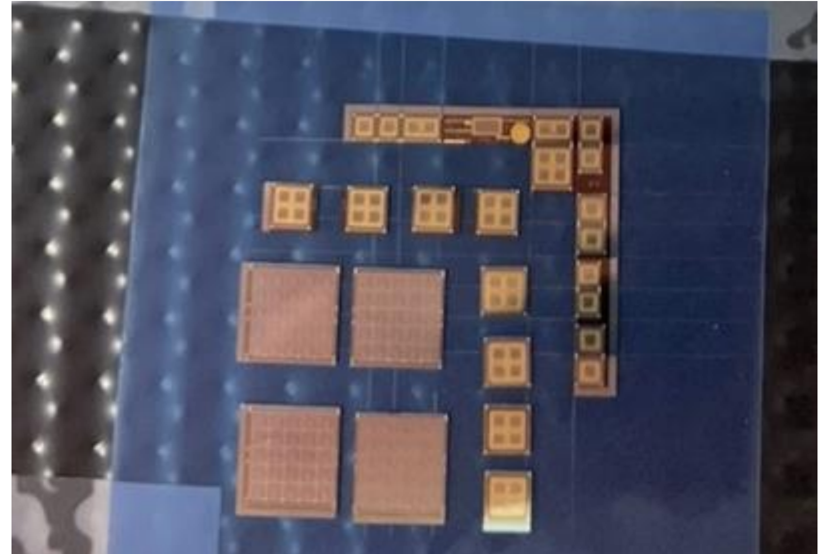
[Timetable for bump bonding tests with over the 100 samples]

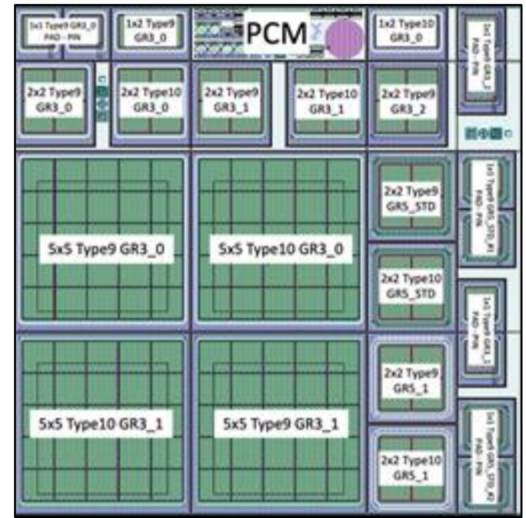
Yield test with Dummy wafers	Nov.					Dec.																															25. Jan.												
Process Item	26	27	28	29	30	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	1	2	3	4	5	6	7	8	9	10	11	12	13
UBM	■	■	■	■	■																																												
Back-grinding 675um → 300um								■	■	■																																							
Dicing											■	■																																					
Solder bumping															■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■													
Bump bonding																			■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■			
Resistance measurement																																						■	■	■	■	■	■	■	■	■			

Wafer post-processing status in Korea

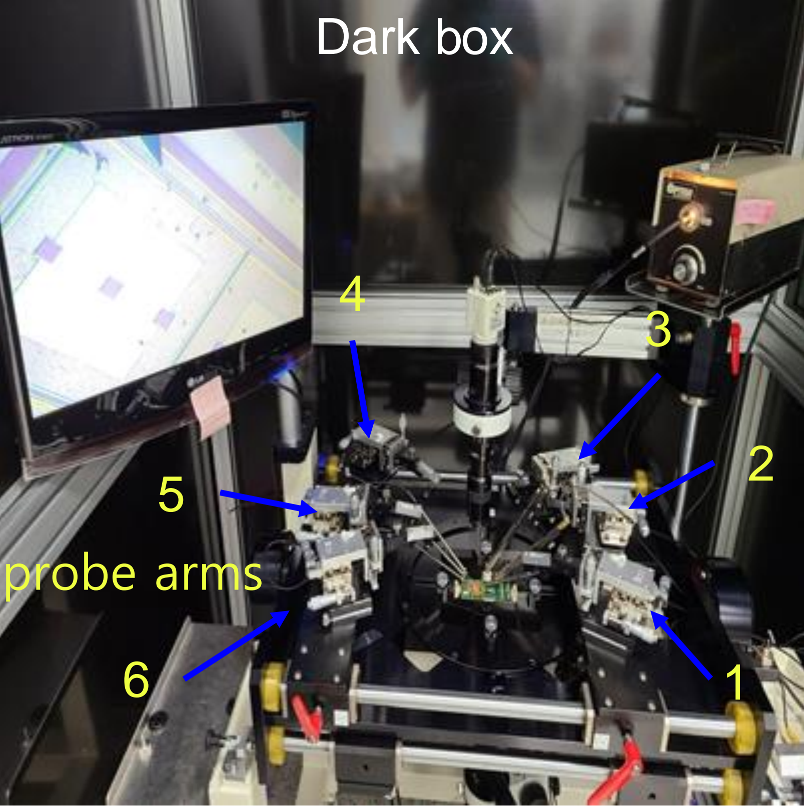
- Two test structures in each wafer were diced in detail.



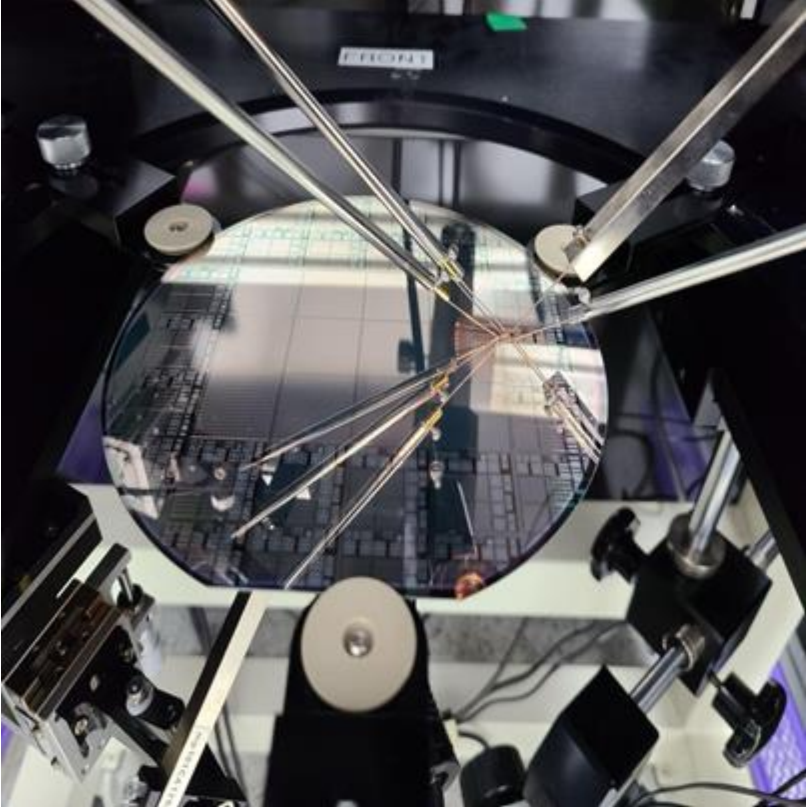




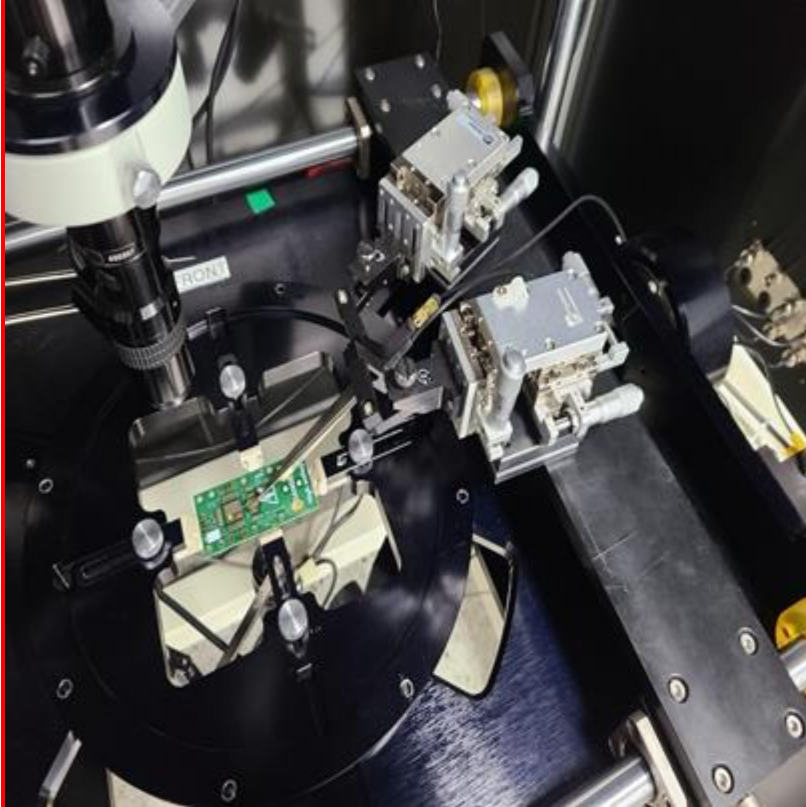
Probe Station setup at KNU



- Overview



- wafer chuck



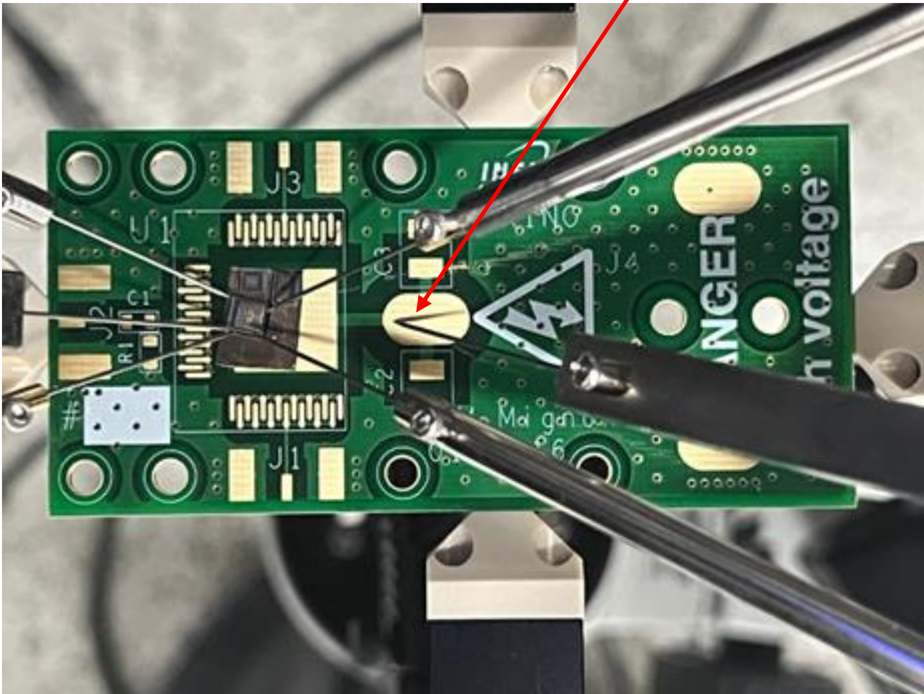
- sensor chuck

- There are 6 probe arms that use magnets to connect with the station
  → Can Compare I-V, C-V measurement results before and after UBM up to **2x2 size sensors**

- Two types of chuck available for wafer-level and sensor-level tests

Sensor level test at KNU

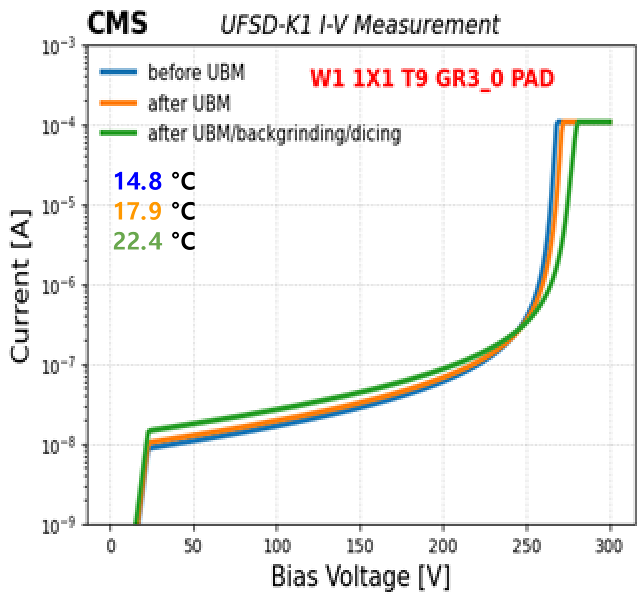
Bias voltage apply

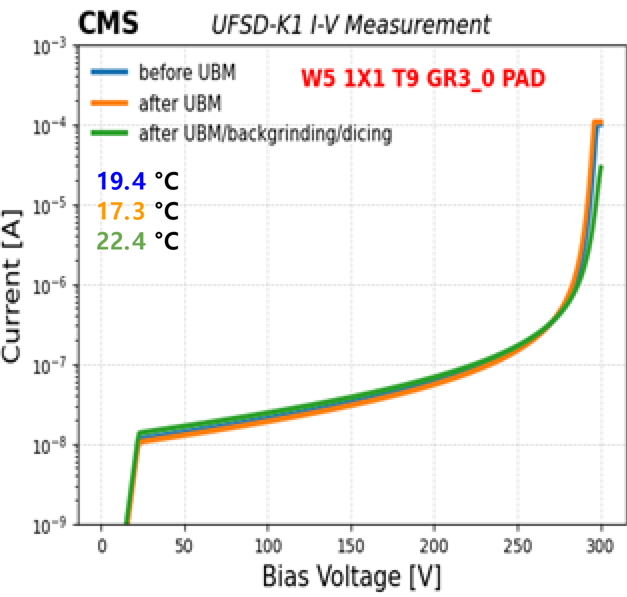


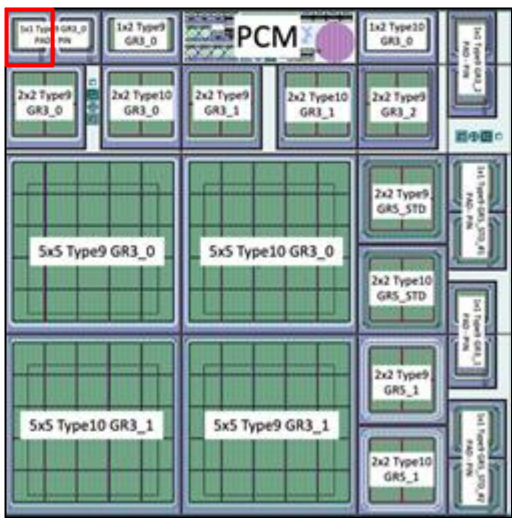
1x1, 1x2, 2x2 | 5x5 | 16x16

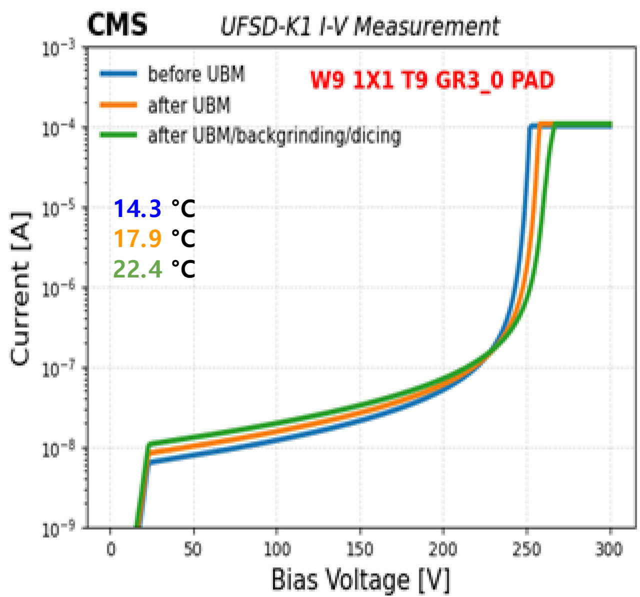
- Sensors can be attached to PCB board with electrically conductive double sided tape.

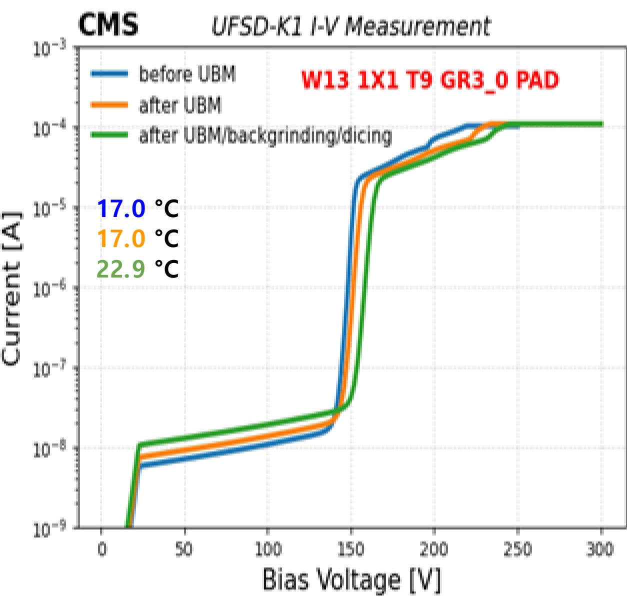
I-V results comparison before and after UBM : 1x1 size (PAD)





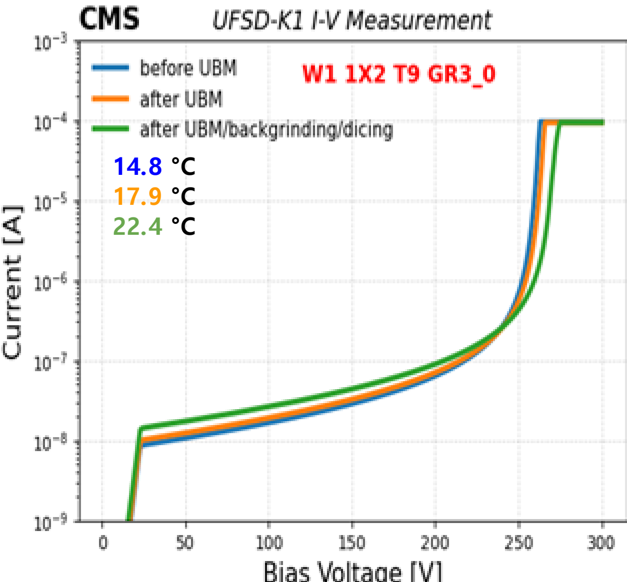


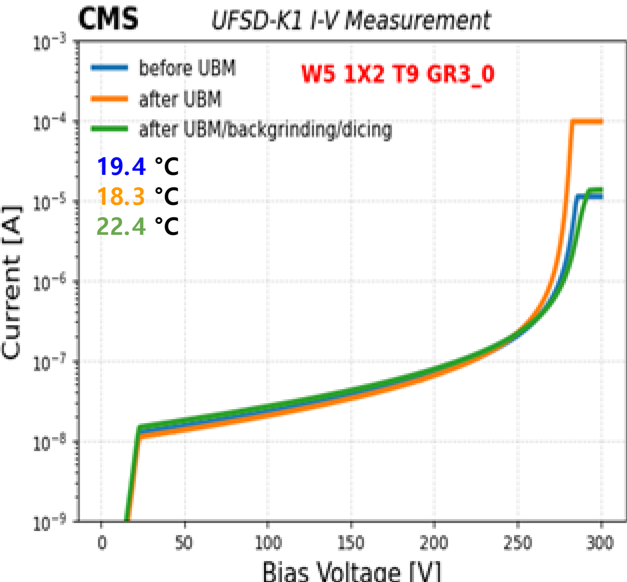


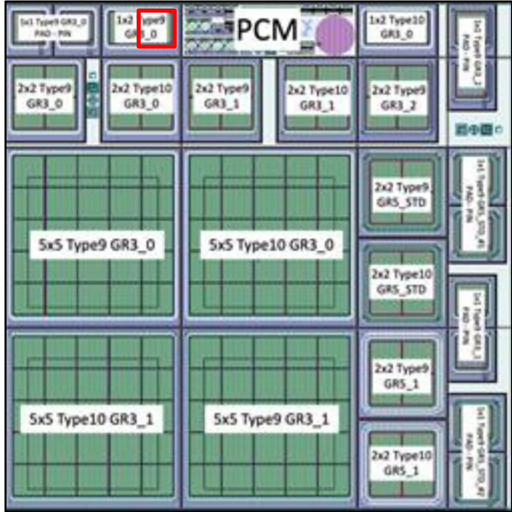


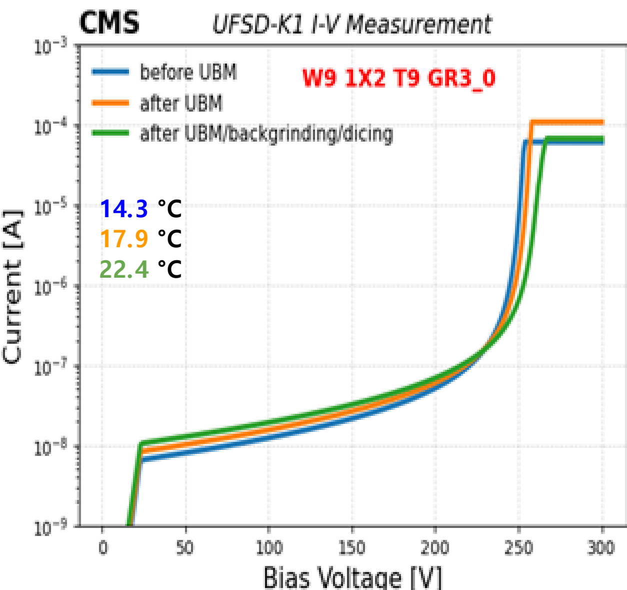
- Current limit = 100 μA
- Bias Voltage applied up to 300 V
- Current increased after post-processing

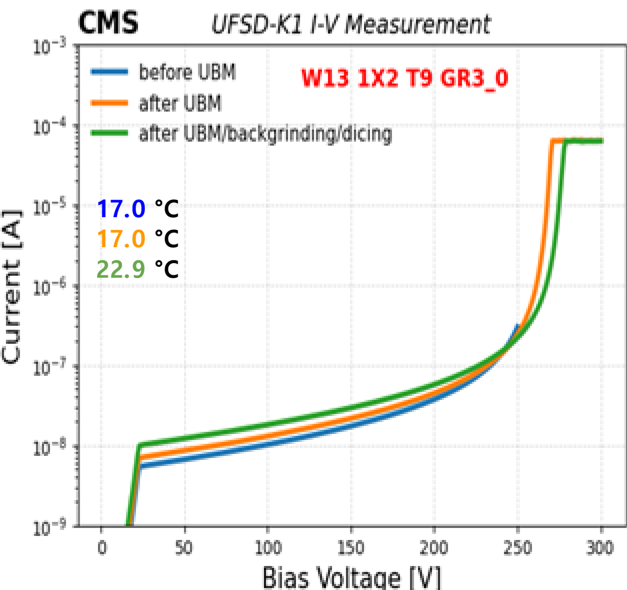
I-V results comparison before and after UBM : 1x2 size





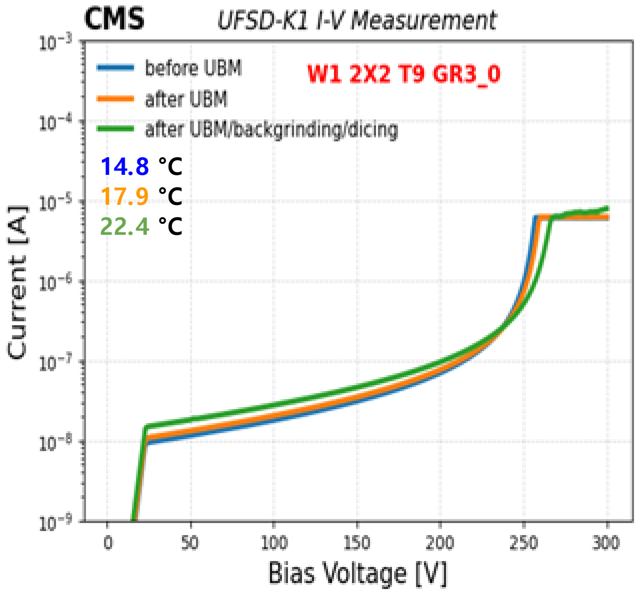


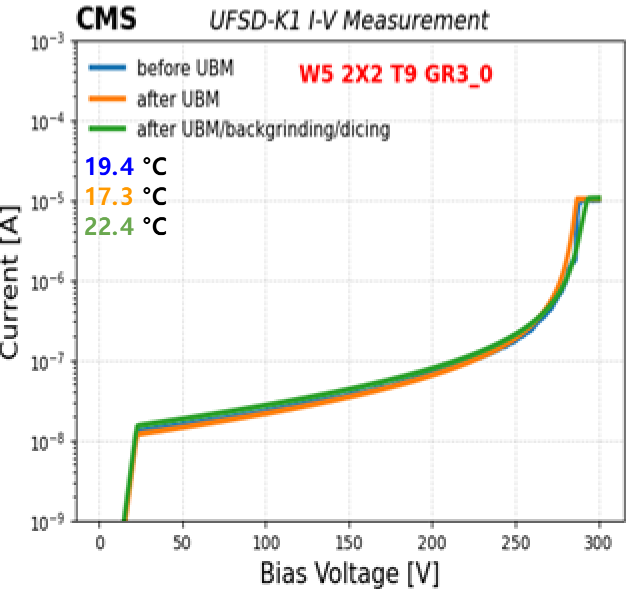


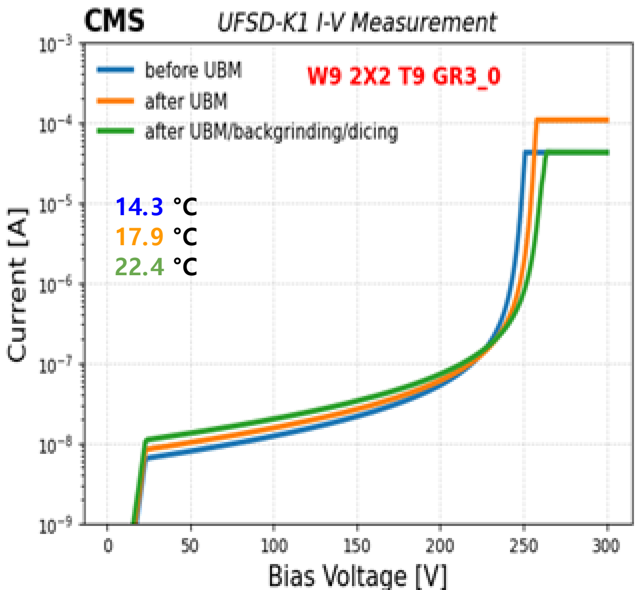


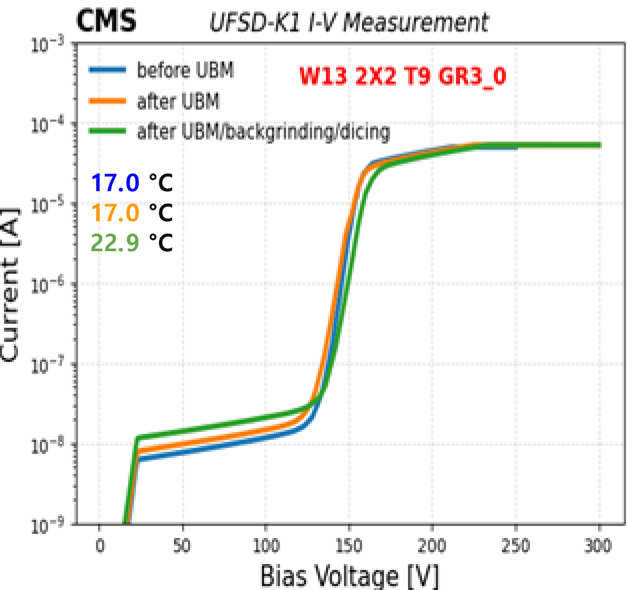
- Grounded other pad during measurement
- Current increased after post-processing

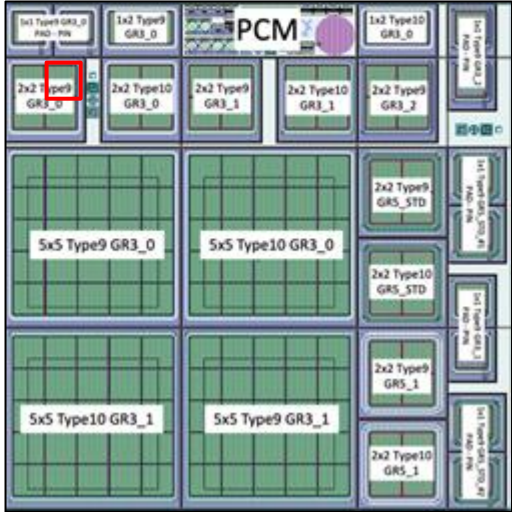
I-V results comparison before and after UBM : 2x2 size





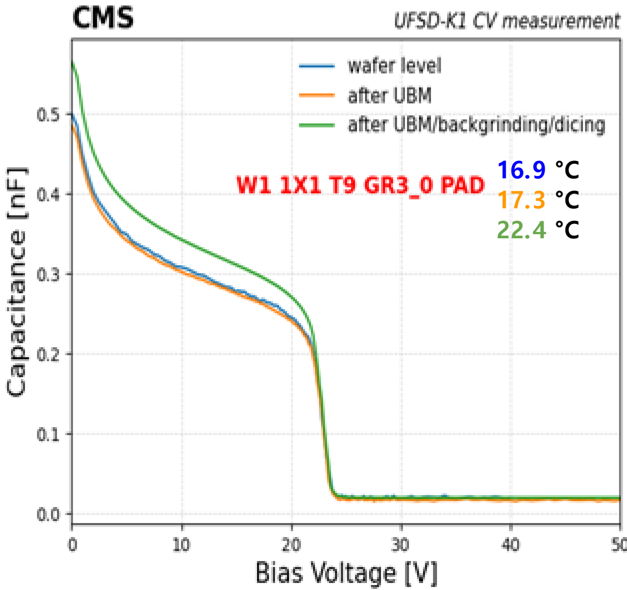


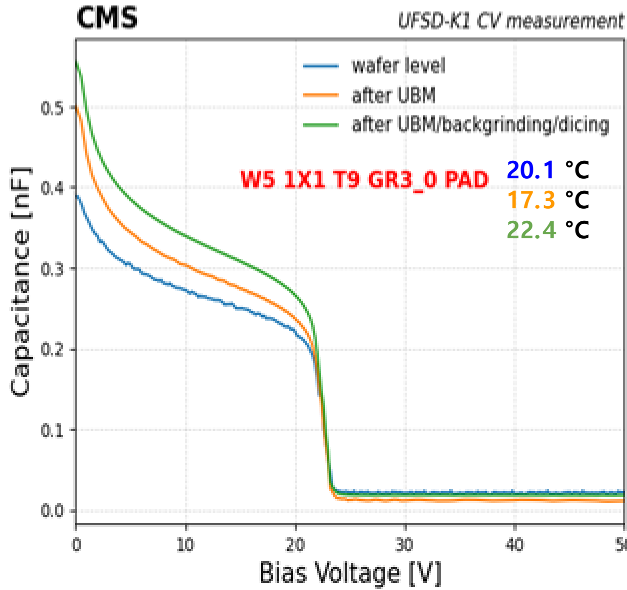


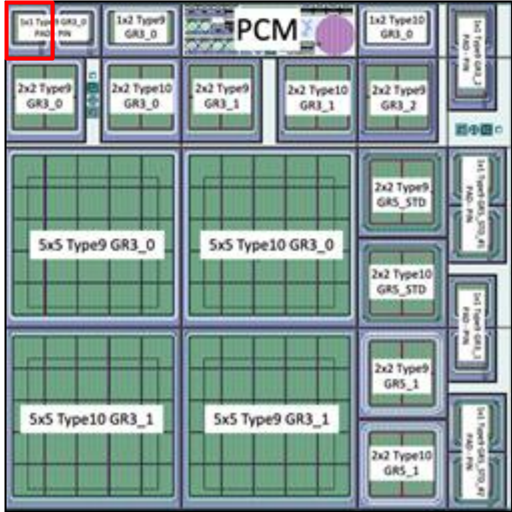


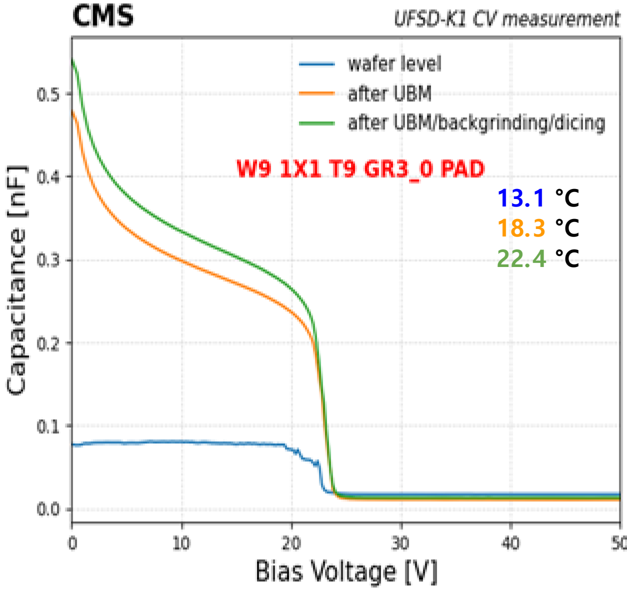
- Grounded other pads during measurement.
- Current increased after post-processing

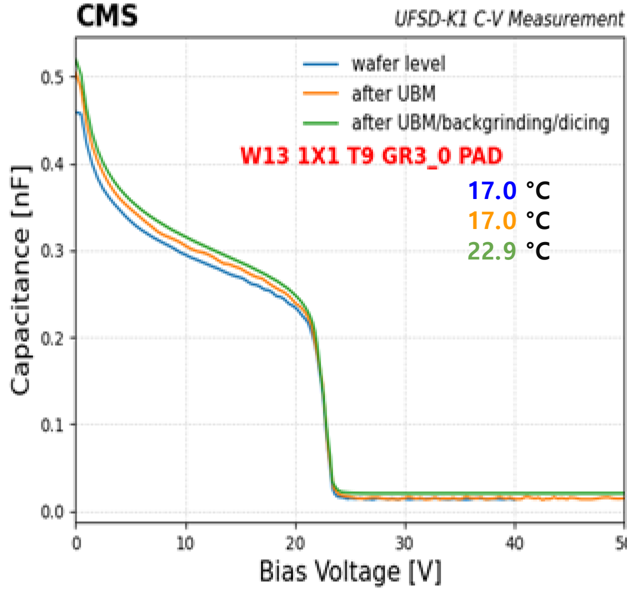
C-V results comparison before and after UBM : 1x1 size (PAD)





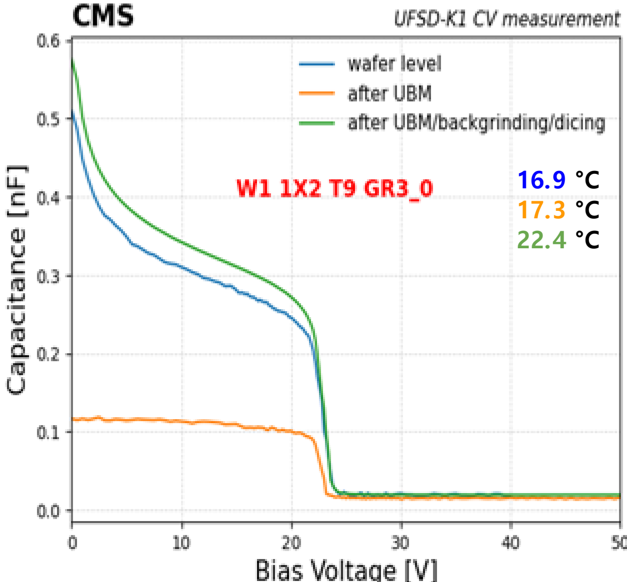


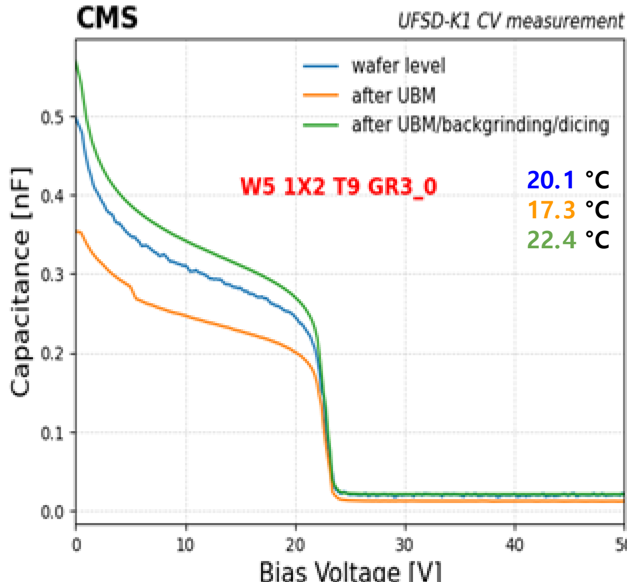


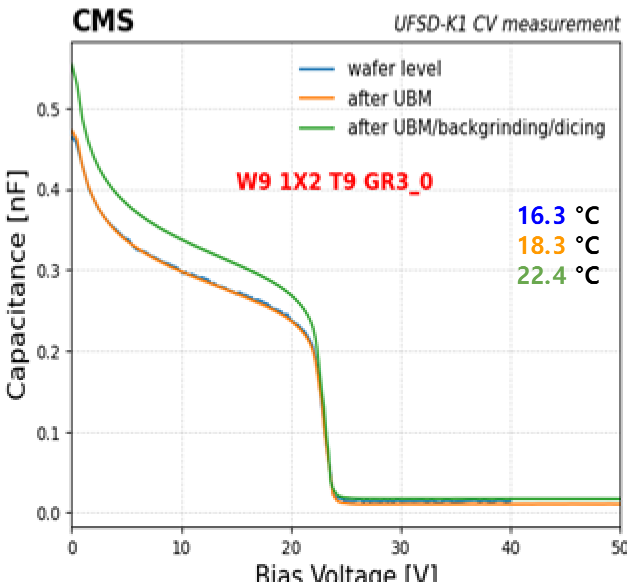


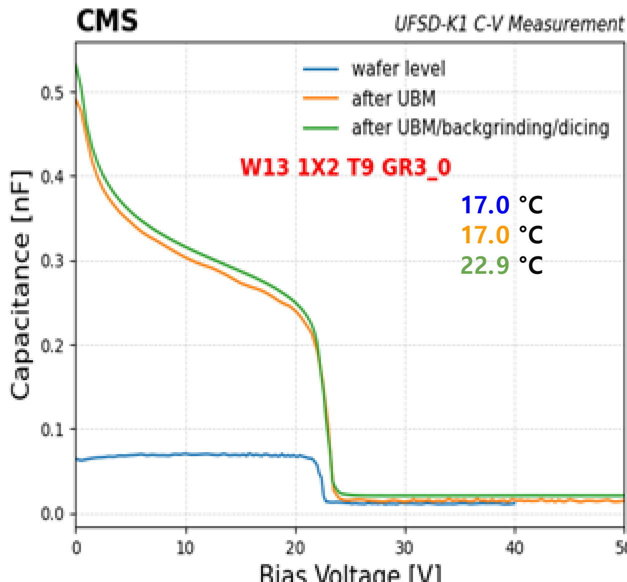
- Bias voltage applied up to 60 V
  - V_{fd} ~ 24V
- V_{fd} is consistent before and after the UBM.
- Difference capacitance below V_{fd}

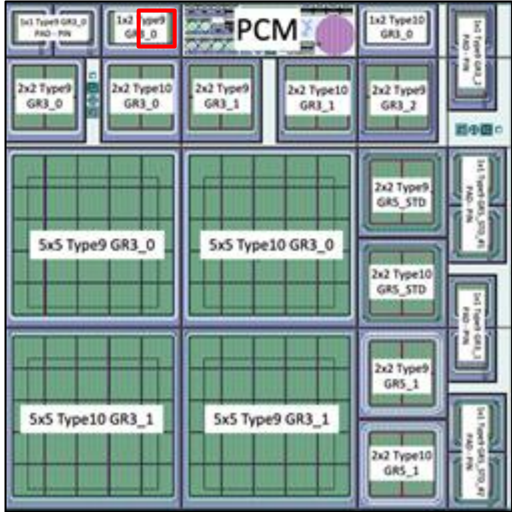
C-V results comparison before and after UBM : 1x2 size





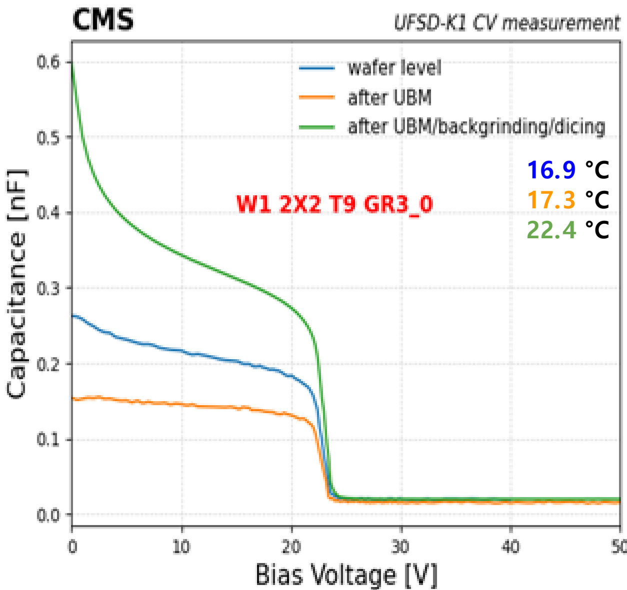


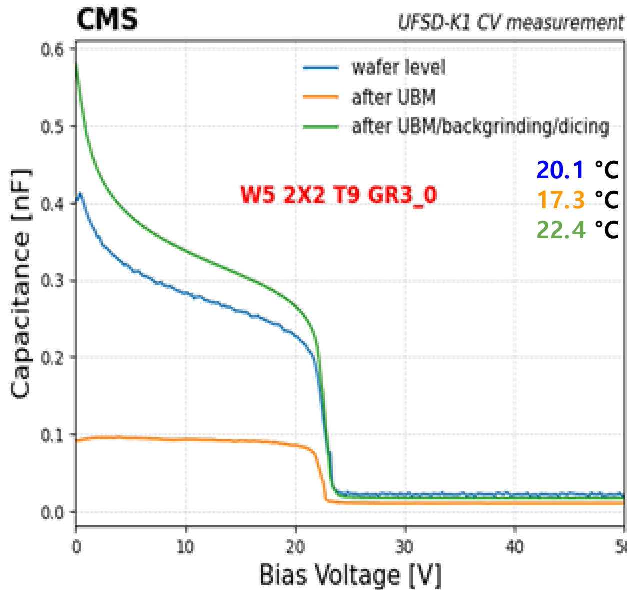


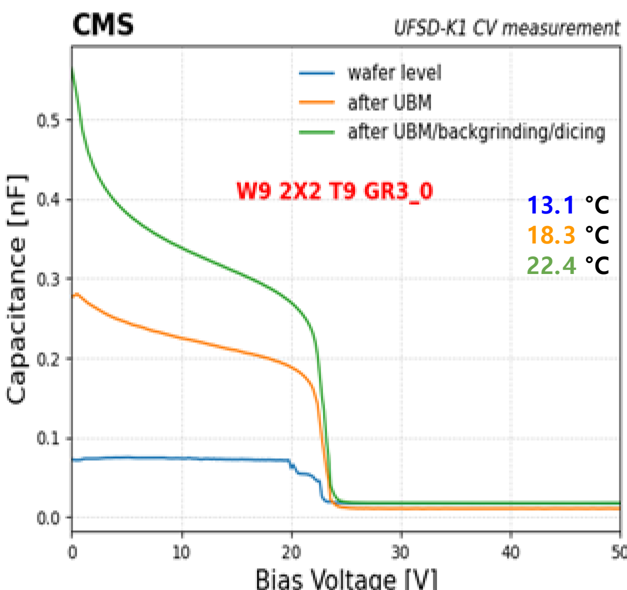


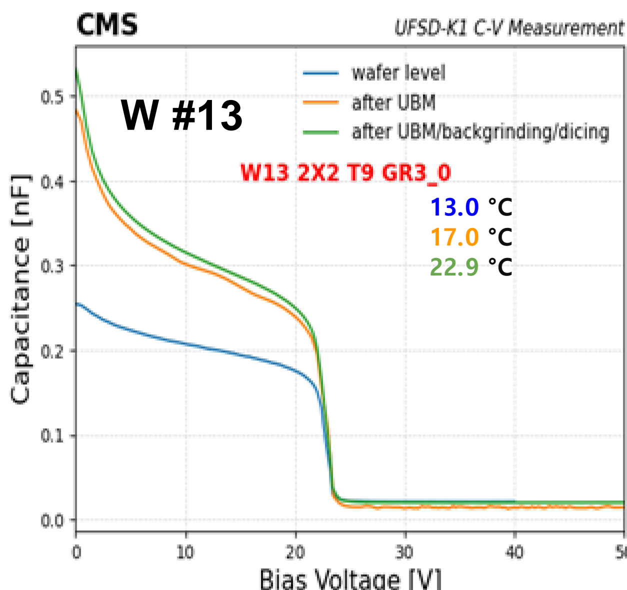
- Bias voltage applied up to 60 V
  - V_{fd} ~ 24V
- V_{fd} is consistent before and after the UBM.

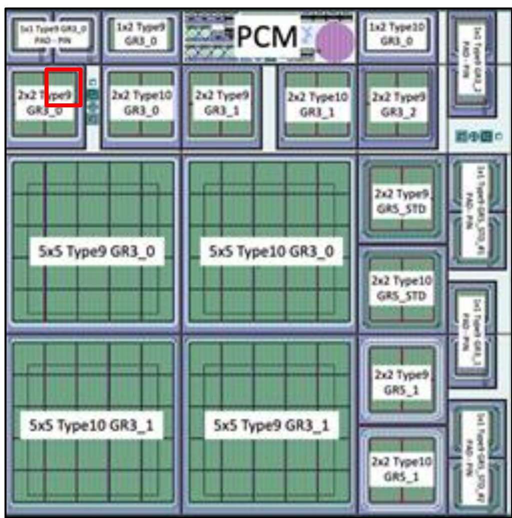
C-V results comparison before and after UBM : 2x2 size







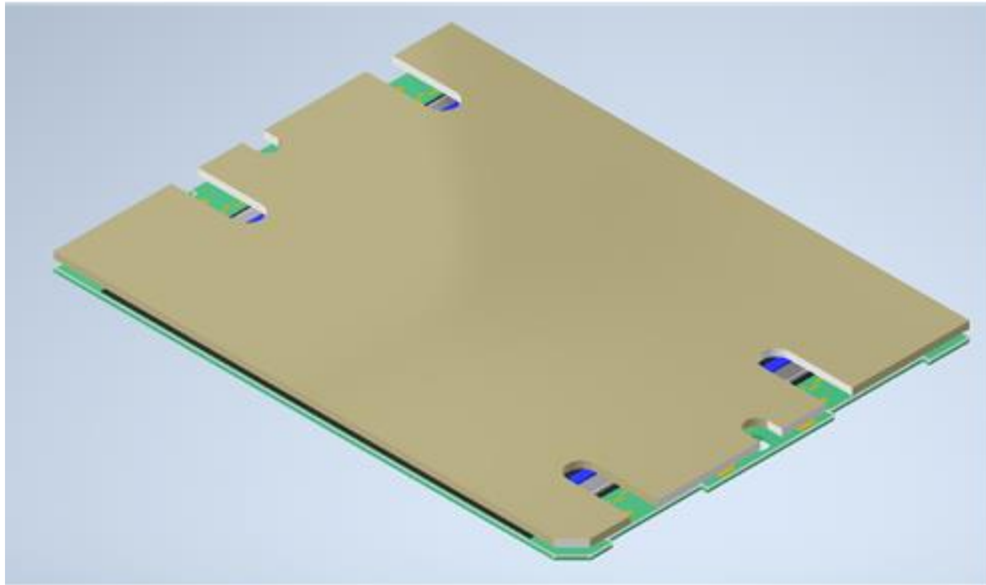




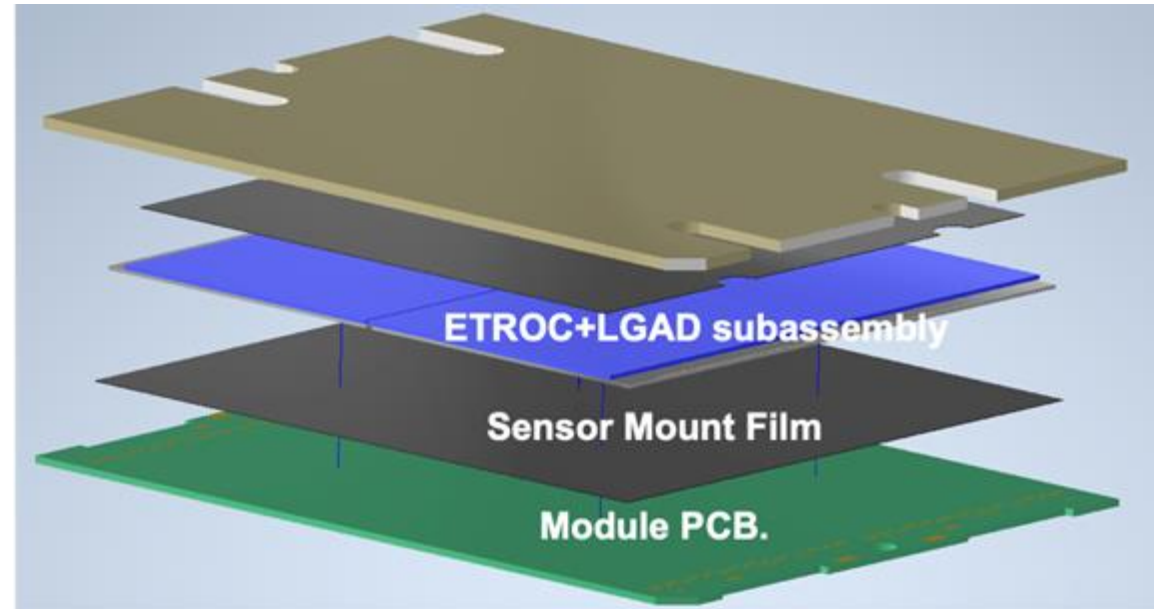
- Bias voltage applied up to 60 V
  - V_{fd} ~ 24V
- V_{fd} is consistent before and after the UBM.

ETL Module design overview

- Module design overview



PCB + subassembly

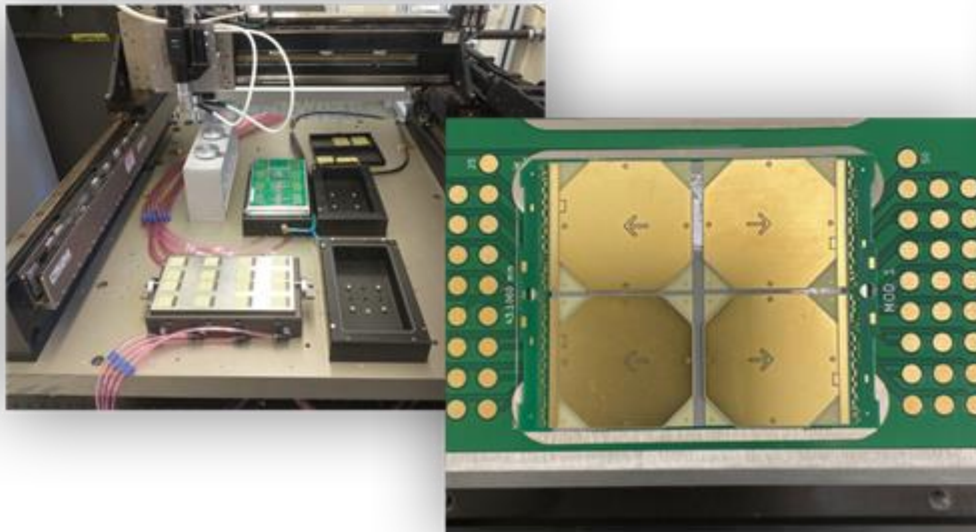


Basic scheme of a module

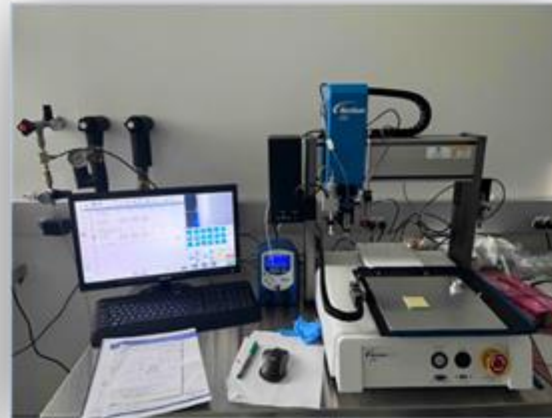
- Module PCB
  - Printed circuit board that serves as the power and readout interface for the module
- 4x ETROC+LGAD subassembly
  - 2x2 arrangement of bump-bonded assemblies
  - Each of a 16x16 pixel LGAD sensor and an “ETROC” readout chip

Assembling the ETL Modules

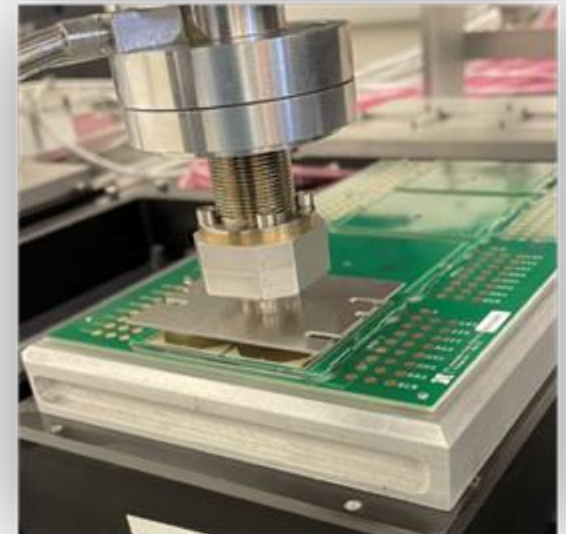
- The ETL detector will need ~8 thousand modules
- Each module will be made of 4 LGAD sensors and ETROCs
- An automated robotic gantry will be used for precision placement at the 10 micron level
- All modules will then be assembled into disks at CERN



Pick & place sensor + PCB



Wirebond and encapsulating

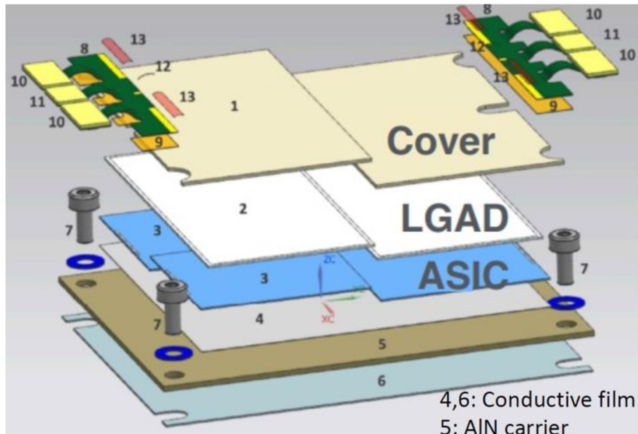


Apply film to baseplate, pick and place, and cure film

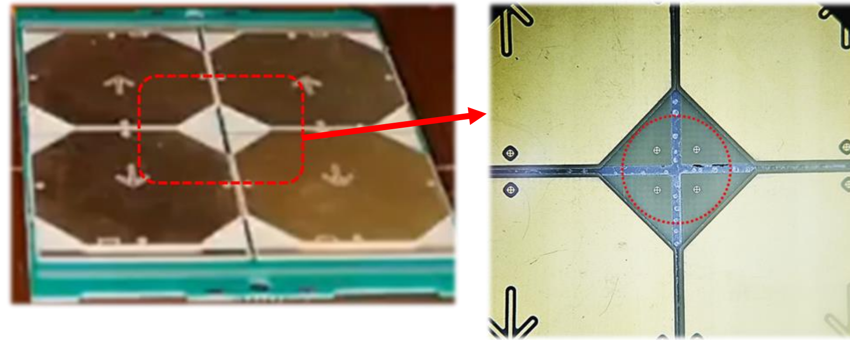
Module assembly test with dummy sample

- Module assembly pre-test for final product

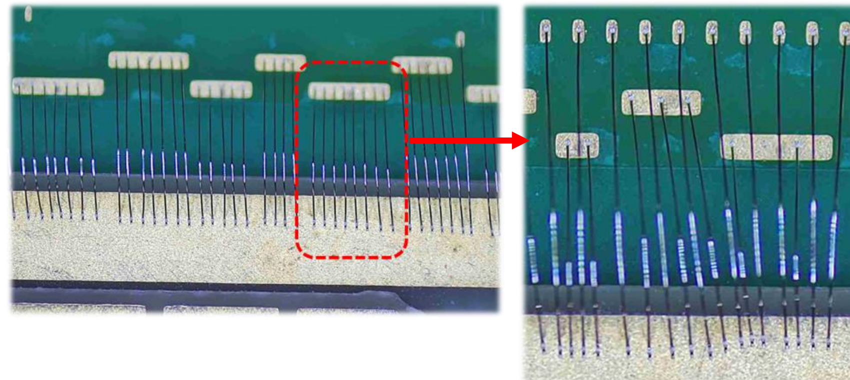
[Module assembly concept of LGAD sensor]



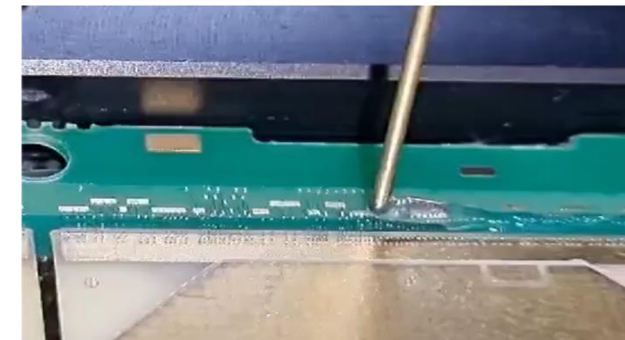
#1. Die attach of Bump bonded sample



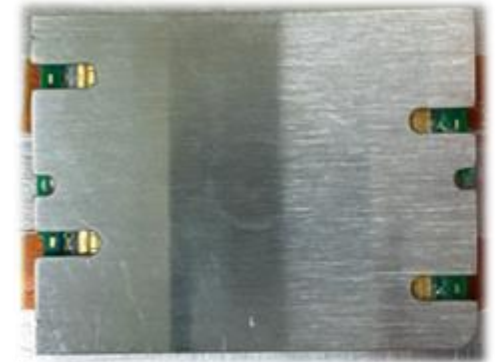
#2. Wire bonding to PCB board



#3. Wire passivation with glue

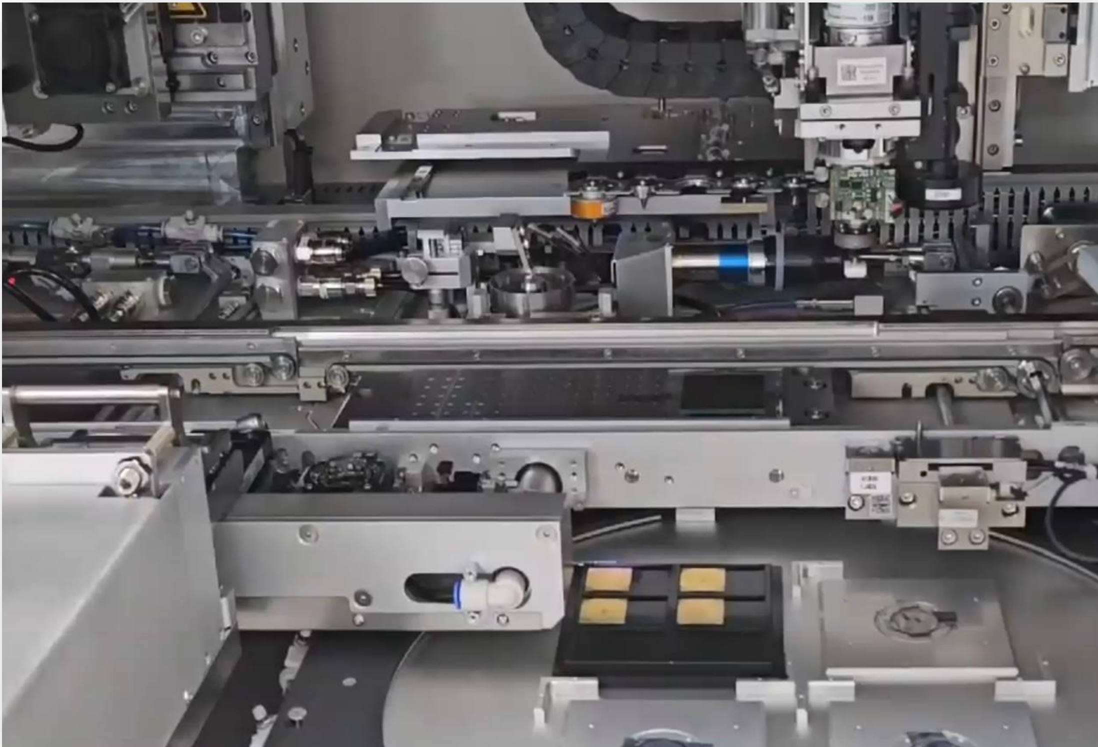


#4. Base plate covering



ETL Module Bonding comparison

TOTAL WORKING TIME = 16sec / 1Chip

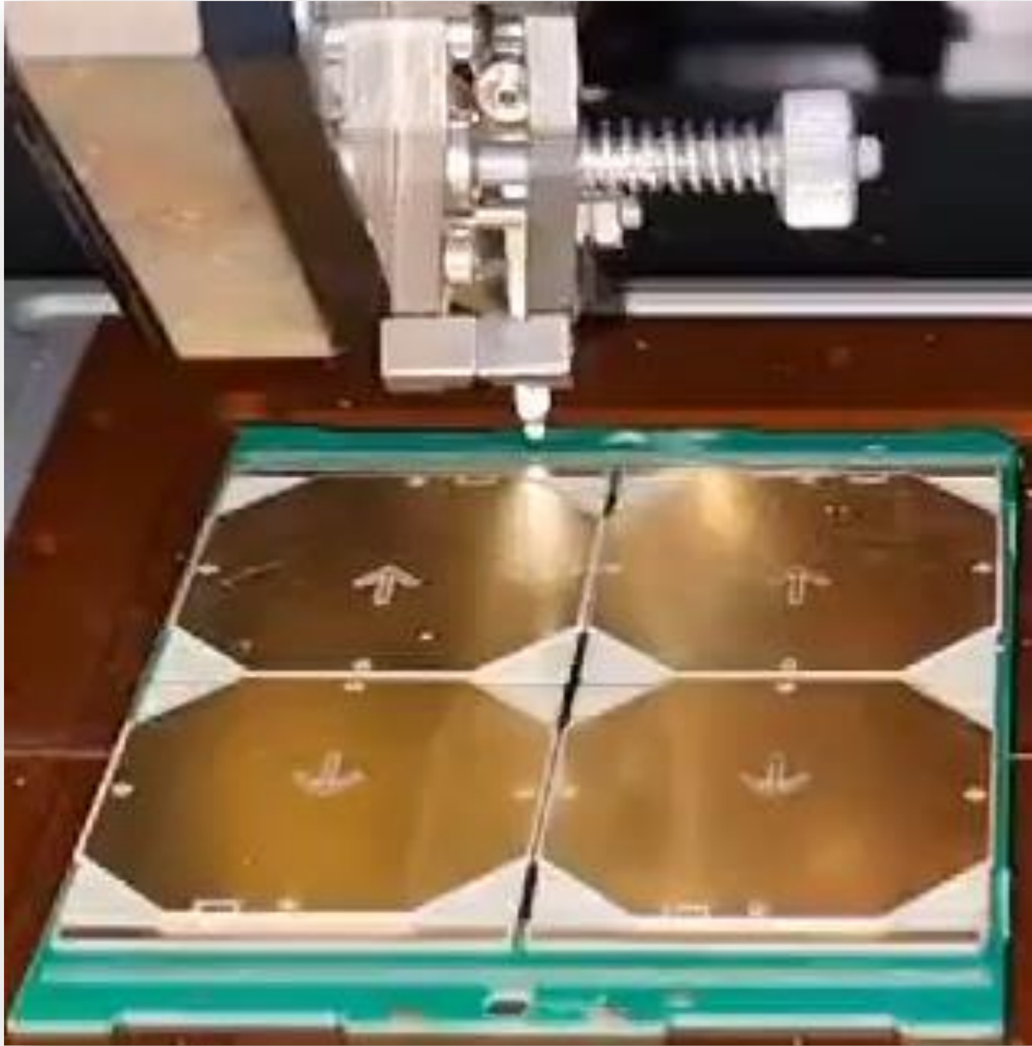


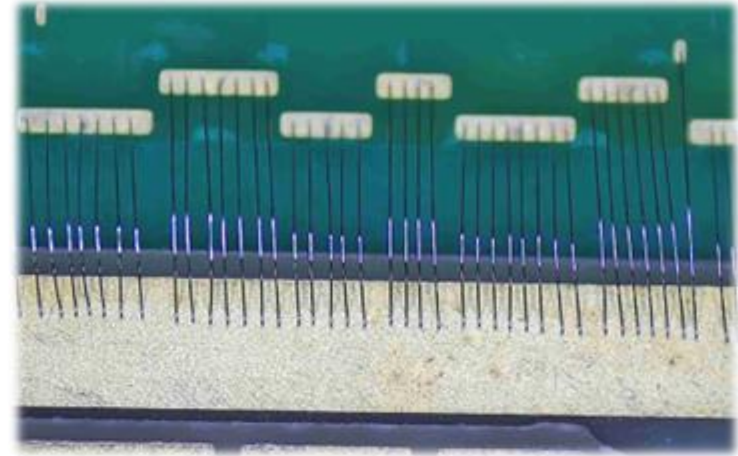
Korean vendor – die bonder machine

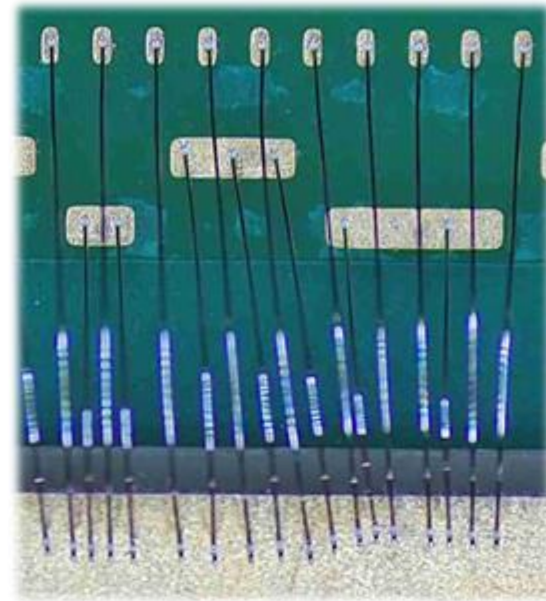
TOTAL WORKING TIME = 1min / 1Chip

Fermilab – Gantry system

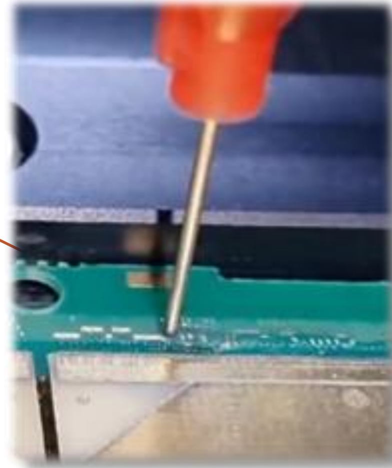
ETL Module Wire Bonding

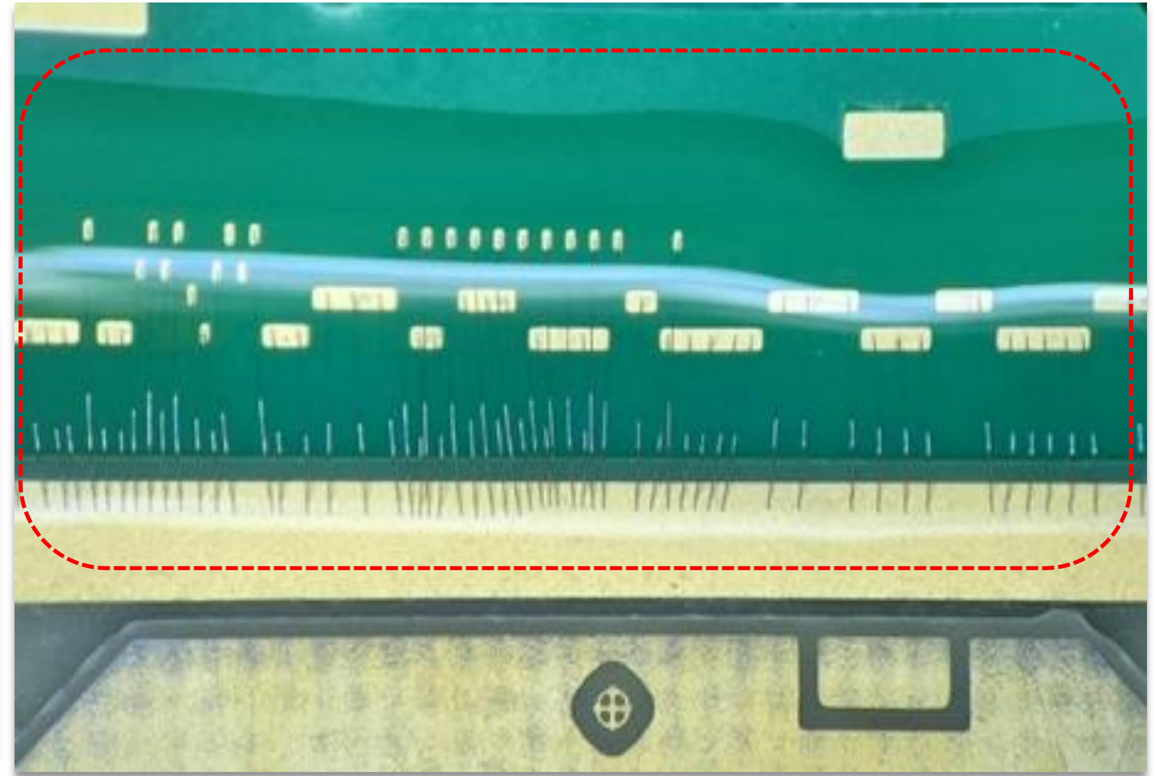






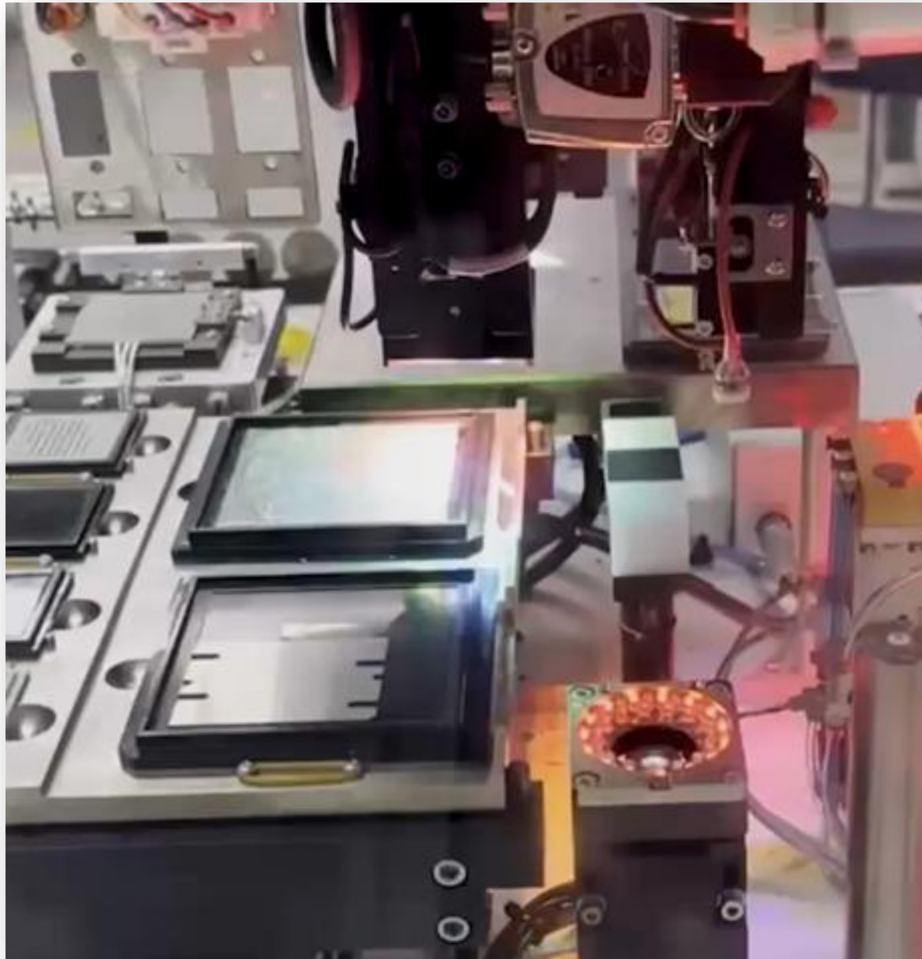
ETL Module Encapsulation



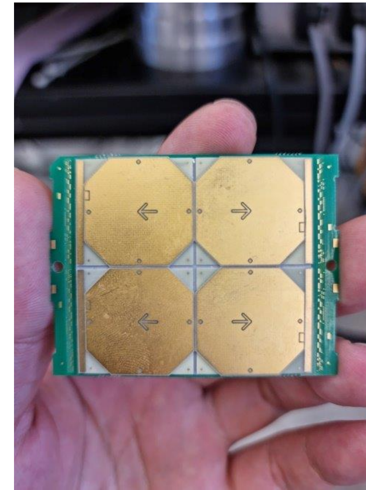


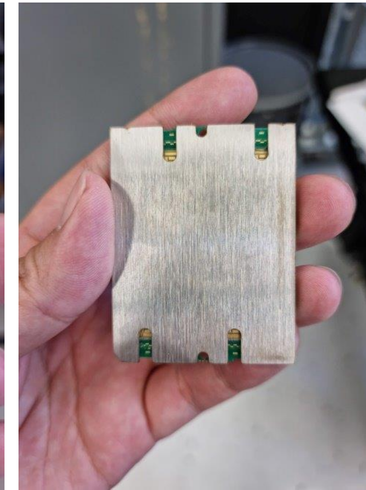
MEMSPACK

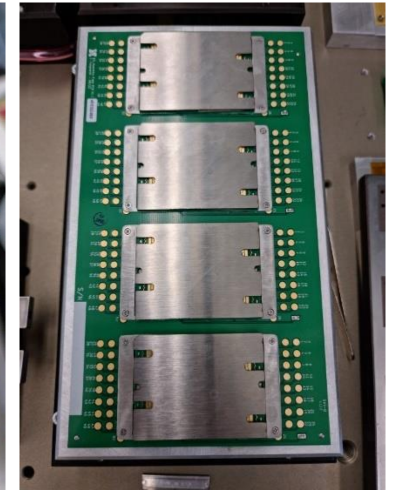
ETL Module Base Plate Bonding



반도체 PACKAGING 장비







- <u>CERN Gantry system issue</u>
- Inaccurate position of baseplate
- Unable to place automatically for current component condition
- Bumpy surface of baseplate makes lift
- Vacuum leakage issue

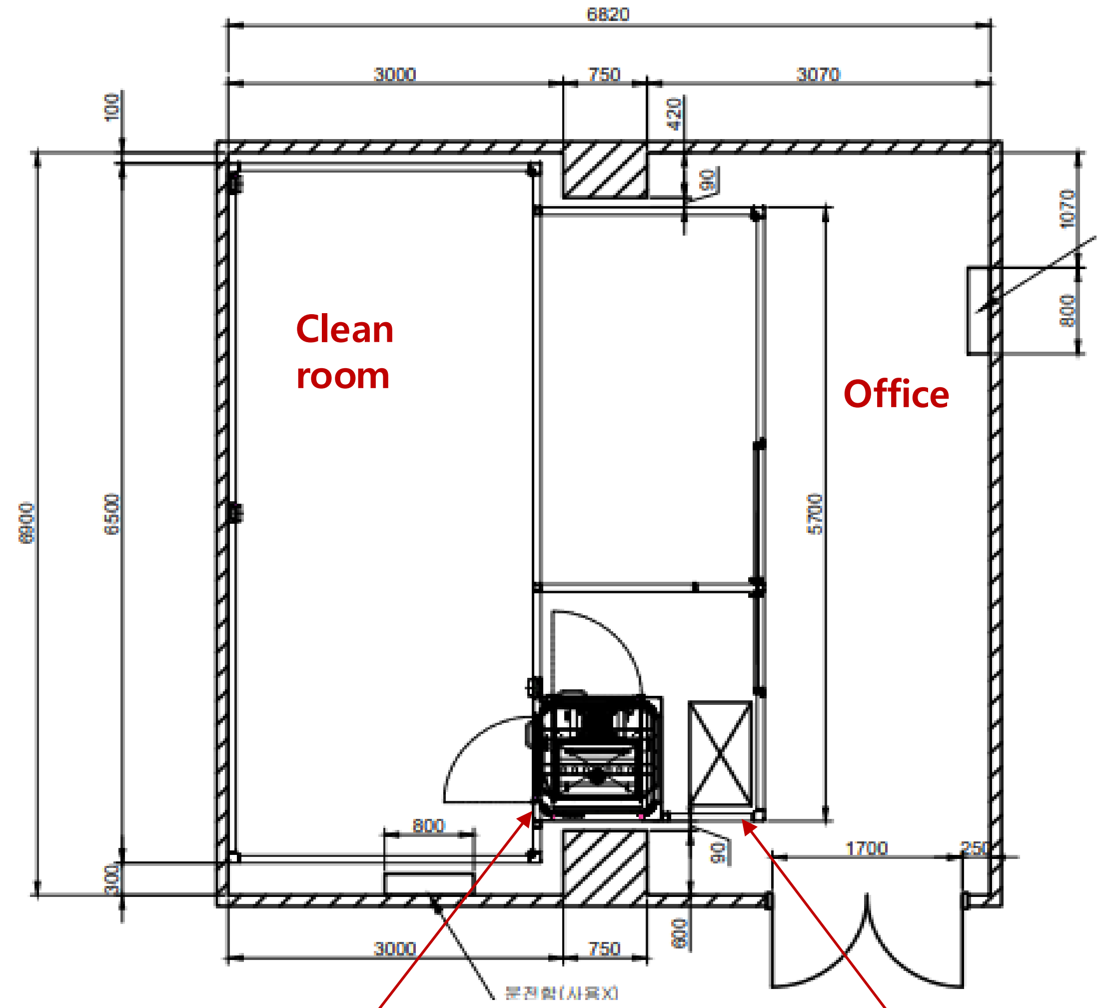
KNU QC/QA facility setup in Korea

1) Clean room setup

- ISO6 (Class 1000)
- Size: 6500(W) x 4800(D) x 2600(H)
- To be completed in Dec, 2024

Expectation

Design of clean room at KNU



Air shower

Temperature & humidity chamber

KNU QC/QA facility setup in Korea

2) Optical inspection & wire bonding setup

- Digital microscope (X1600)
- Optical microscope (X500)
- Olympus wire bonding machine

Wire bonding machine

Digital microscope

Optical microscope

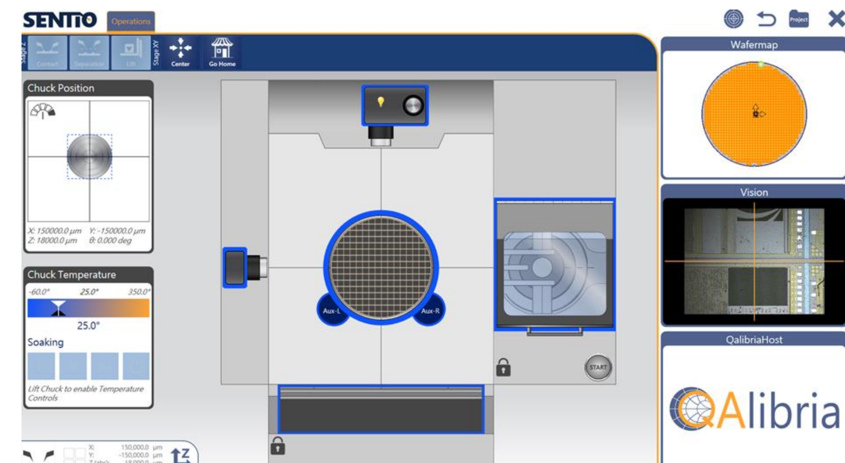
KNU QC/QA facility setup in Korea

3) Probe station system setup (considering to order)

- **MPI TS2000-IFE, 200mm Automated probe station**

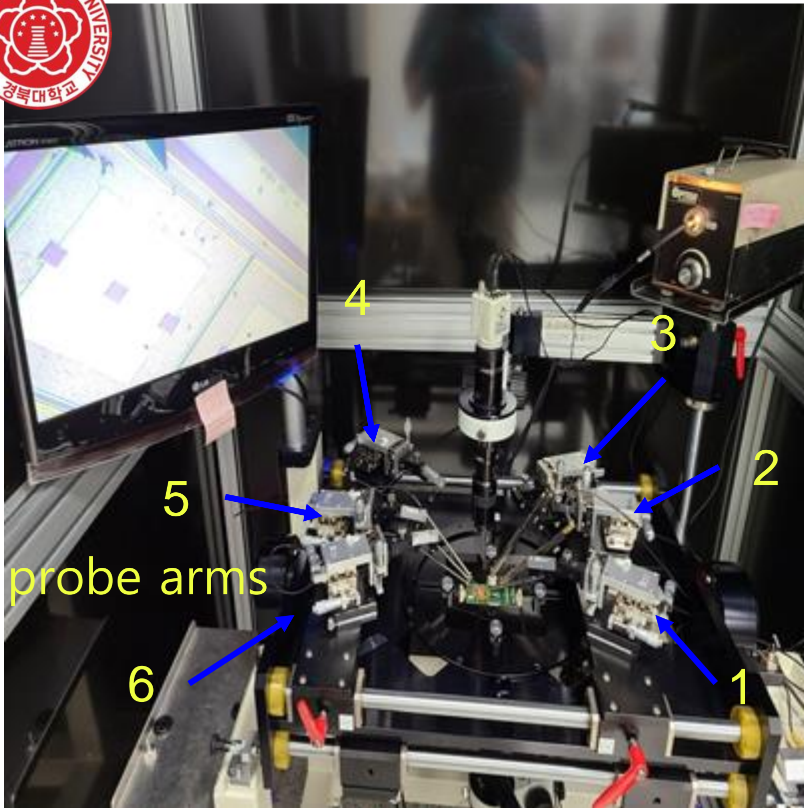
Key features

- **Automated Single Wafer Loader**
  Enables **convenient wafer loading** with easy pre-alignment for automated routines, improving efficiency.
- **Hot/Cold Wafer Swaps**
  Unique capability to load/unload wafers at any chuck temperature, significantly **reducing downtime**.
- **Integrated Hardware Control Panel**
  Provides faster, safer, and more convenient system control and test operation.
- **Temperature control (-60 to 300 °C)**
- **Probe card mounting**

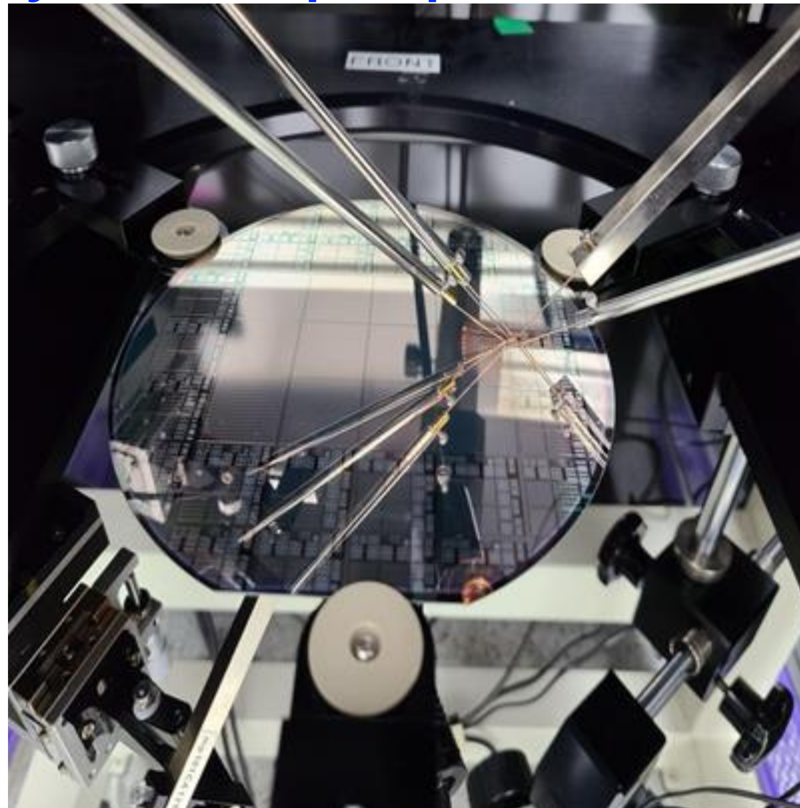


KNU QC/QA facility setup in Korea

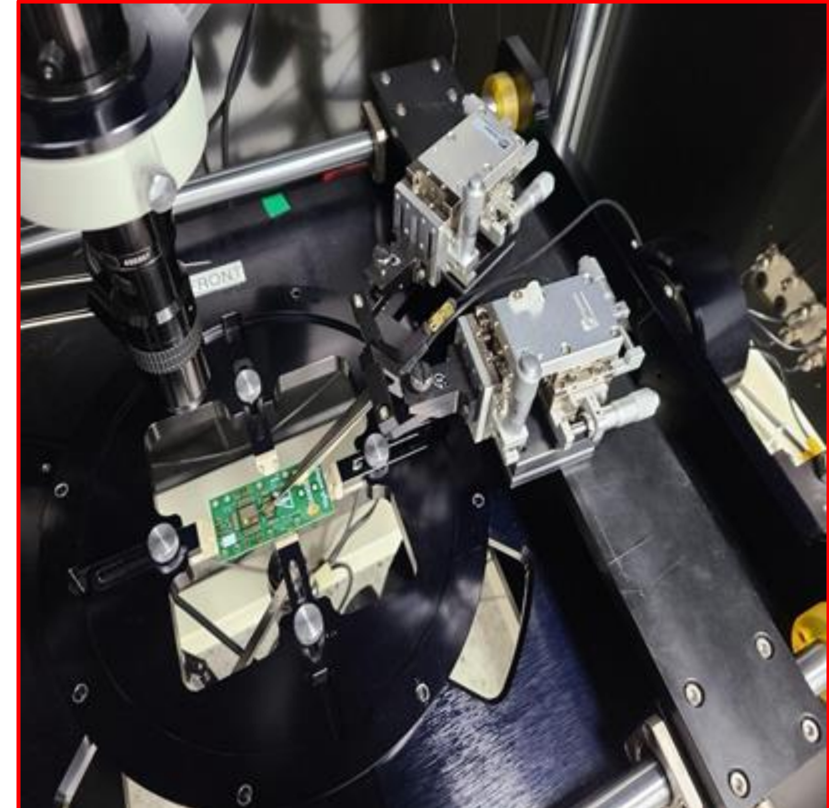
4) Manual Probe station system setup (6 probe arms)



• Overview



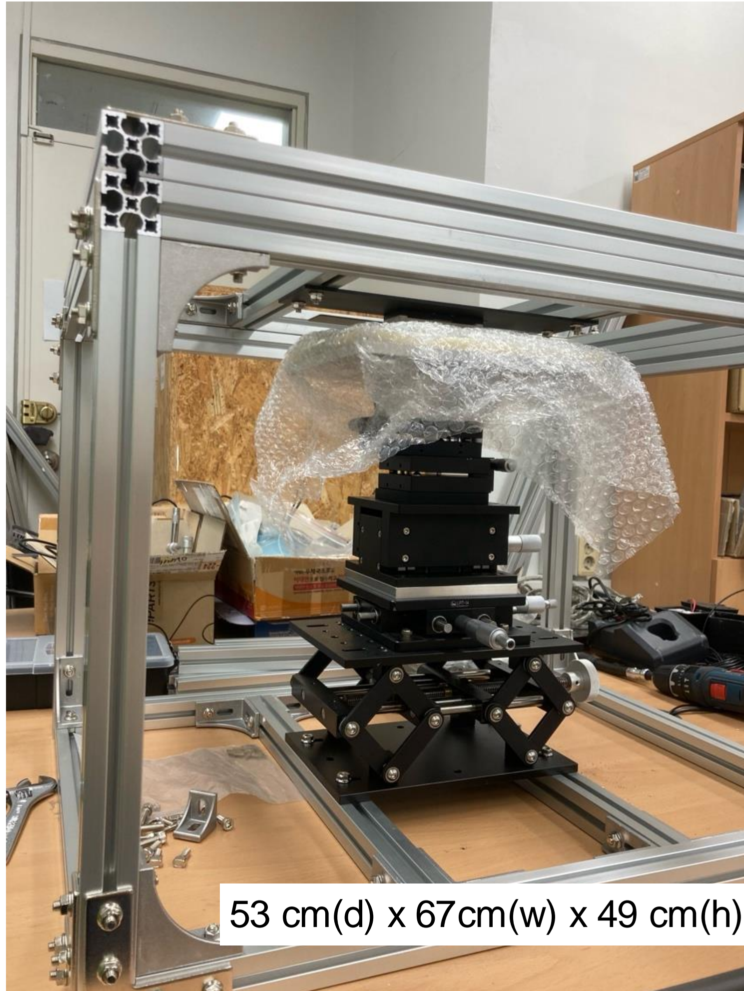
• wafer chuck

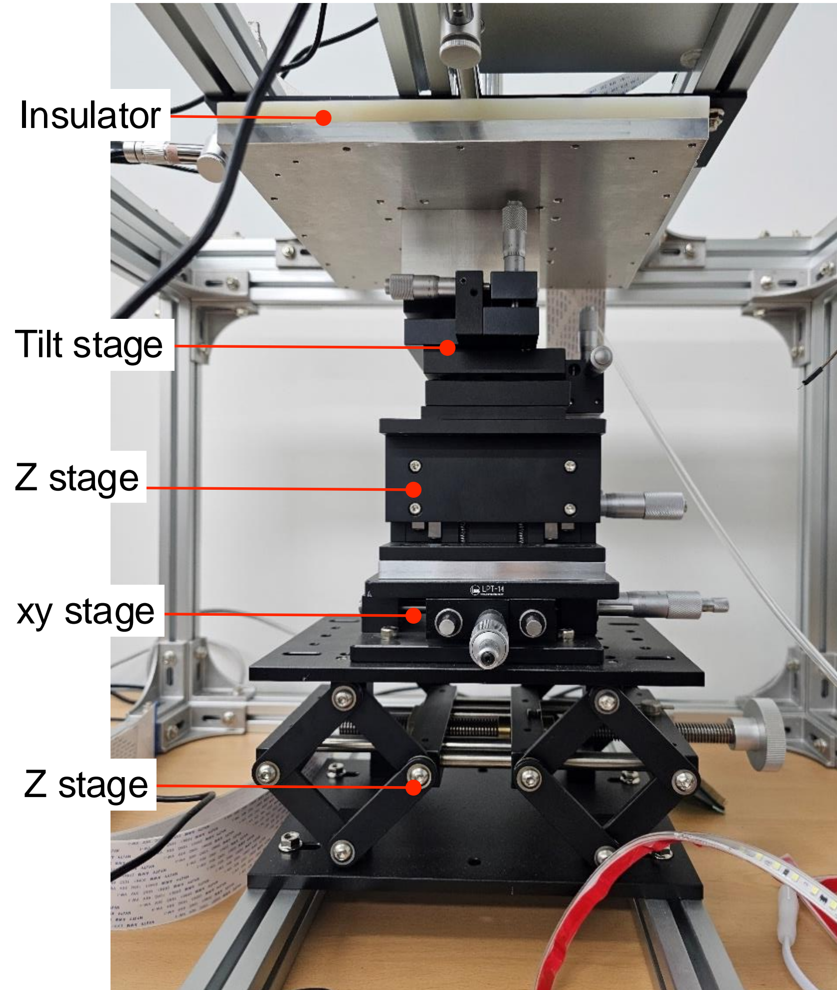


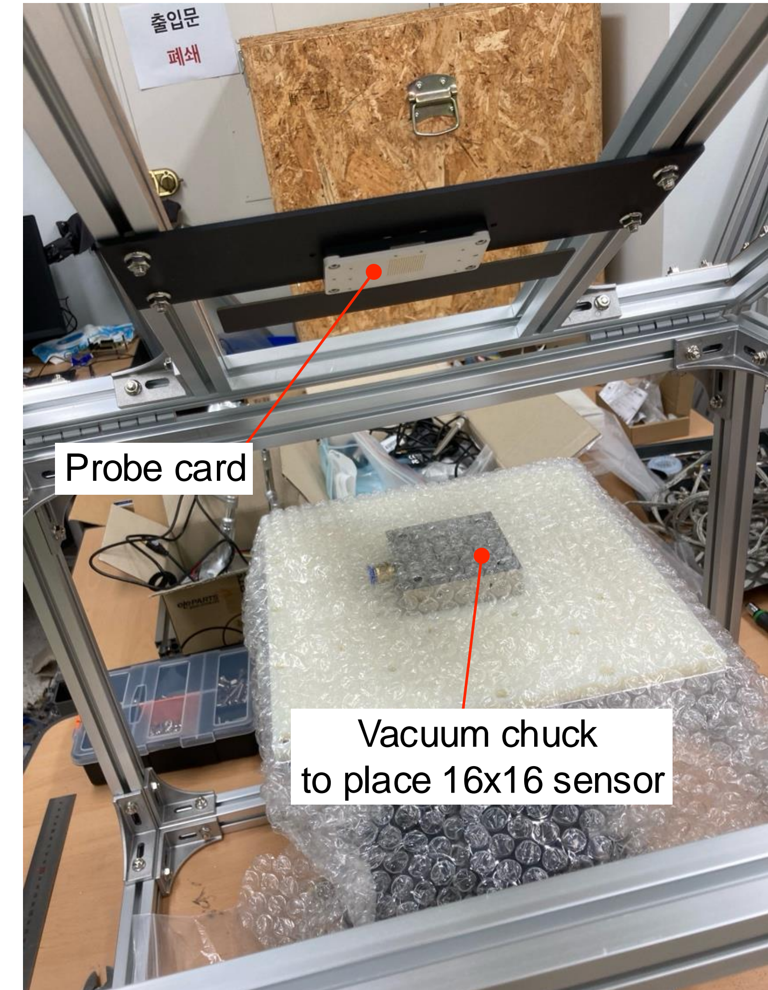
• sensor chuck

- There are 6 probe arms that use magnets to connect with the station
- Two types of chuck available for wafer-level and sensor-level tests

Probe card system test setup





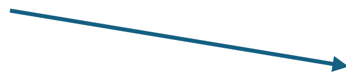


- Meanwhile many improvements have been made on probe card system
  - Added few stages and fixed the probe card, usb microscopes, and vacuum chuck on the jig
- Checked the feasibility of the current probe card design with this probe card jig

Probe card design

Front

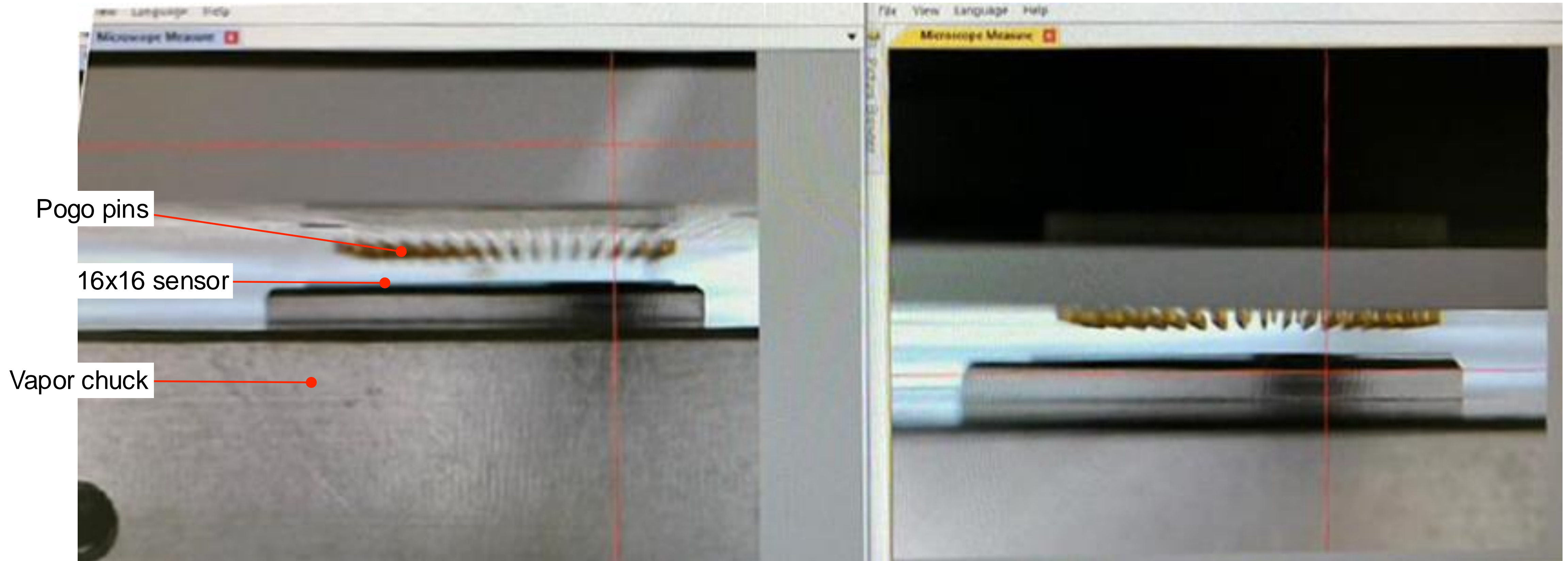
Back



Readout cable connectors

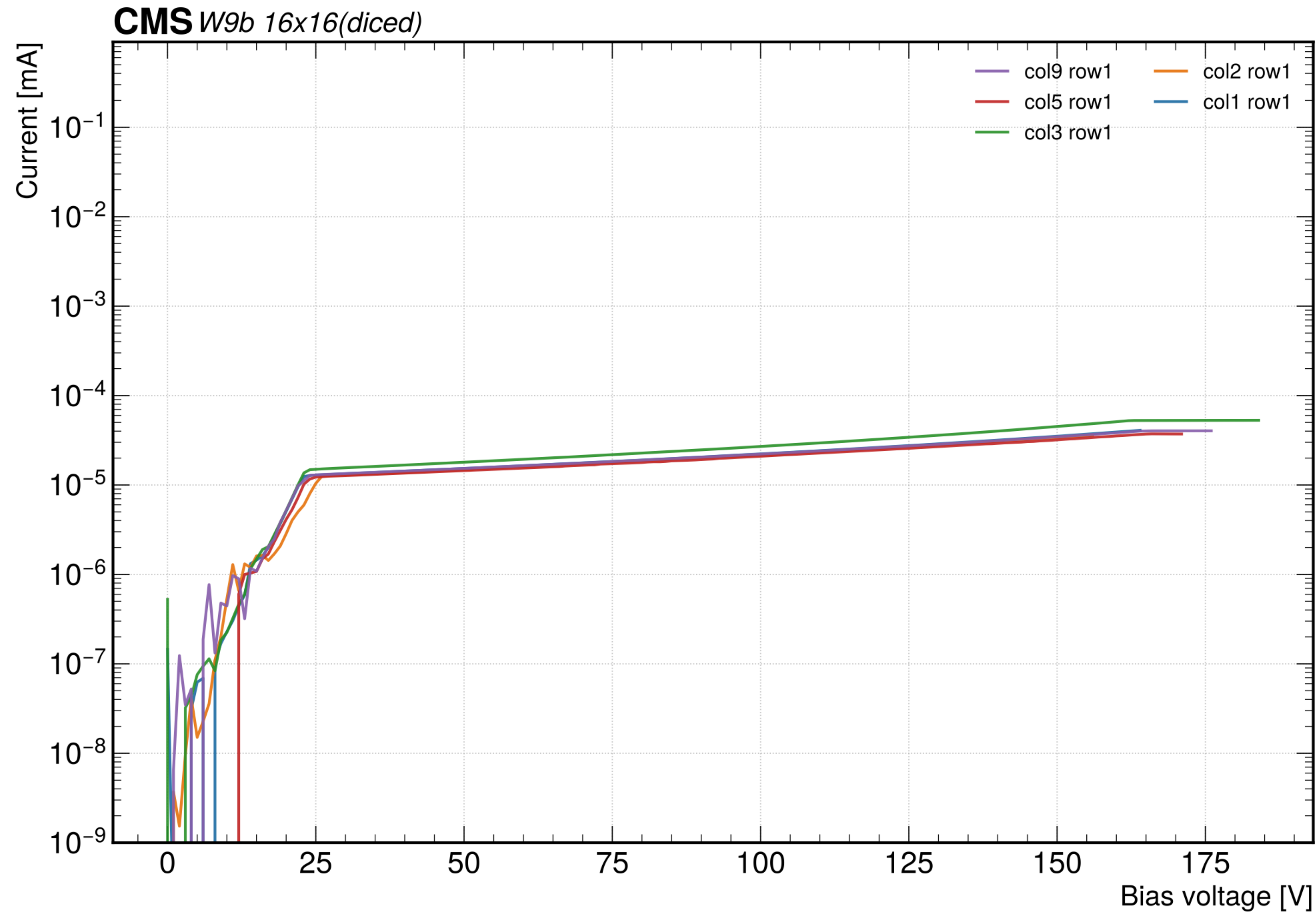
Pogo pins contact

Contact between sensor and pogo pins seen by two side usb cameras



- Using two USB cameras, we adjust the tilt and the distance between the sensor and the probe card using the tilt and z stages.
- Checking good contact
  - ➢ Using a multimeter to confirm the connectivity between the two outermost BBs though the probe card.
  - ➢ If they are connected we assume the contact is good.

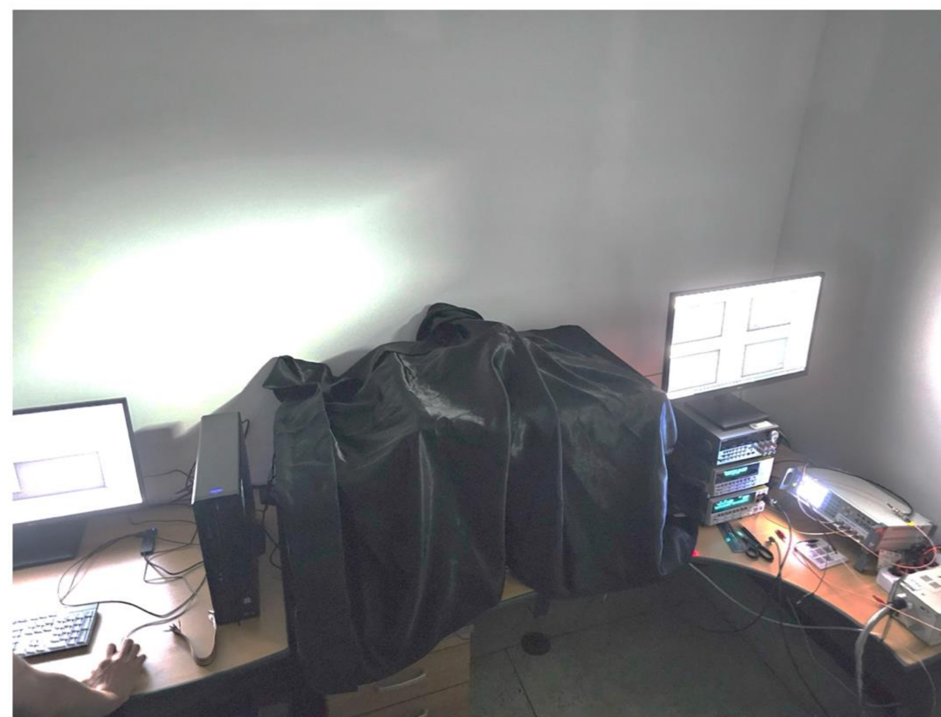
IV measurement results with the current system



- Measured 5 different pads by manually changing the channels
- The IV curves look reasonable and are consistent each other

Probe card - IV test

- 16x16 array
- Total current



CMS *W9b 16x16(diced)*

col9 row1 96 ground
col9 row1 192 ground
col9 row1 256 ground

256 GND
192 GND
96 GND

Total Current (mA)

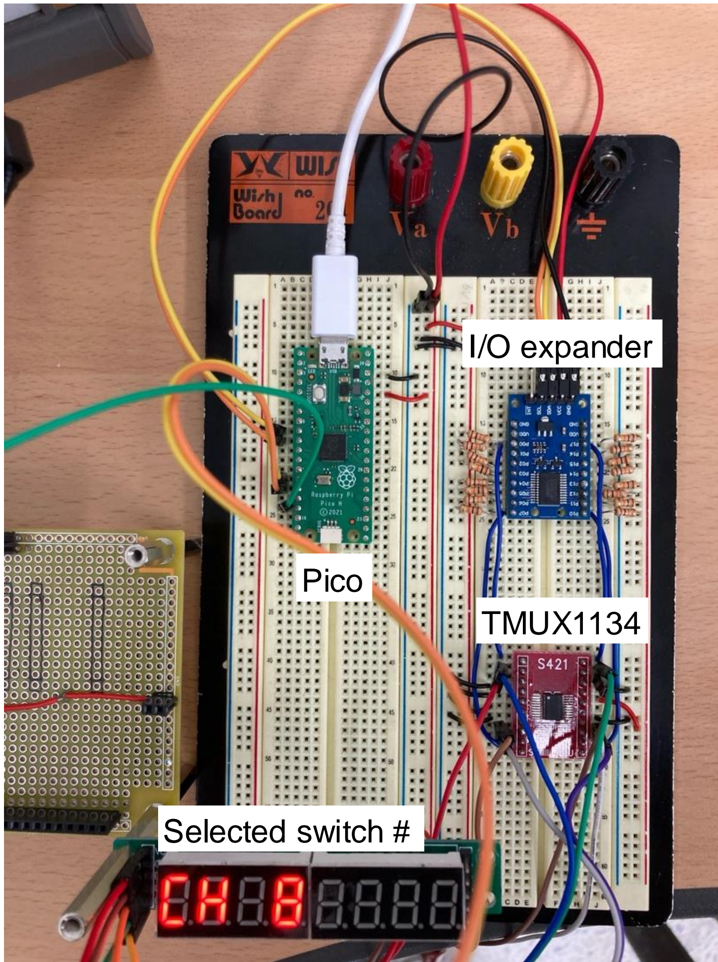
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}

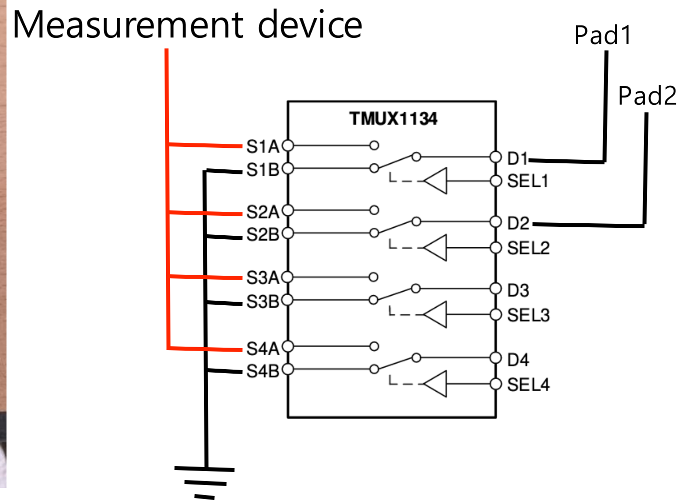
0 25 50 75 100 125 150

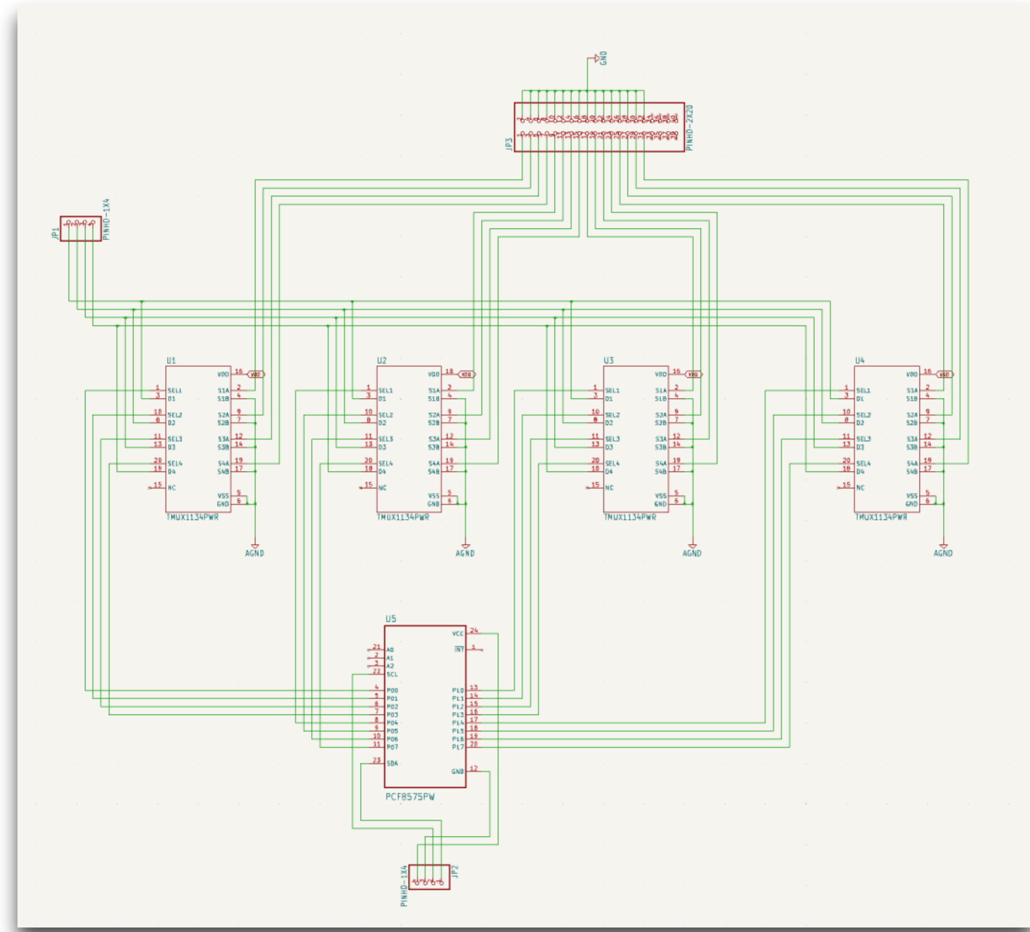
Bias Voltage (V)

Switching matrix development

Switch matrix module design for 16x16 LGADs

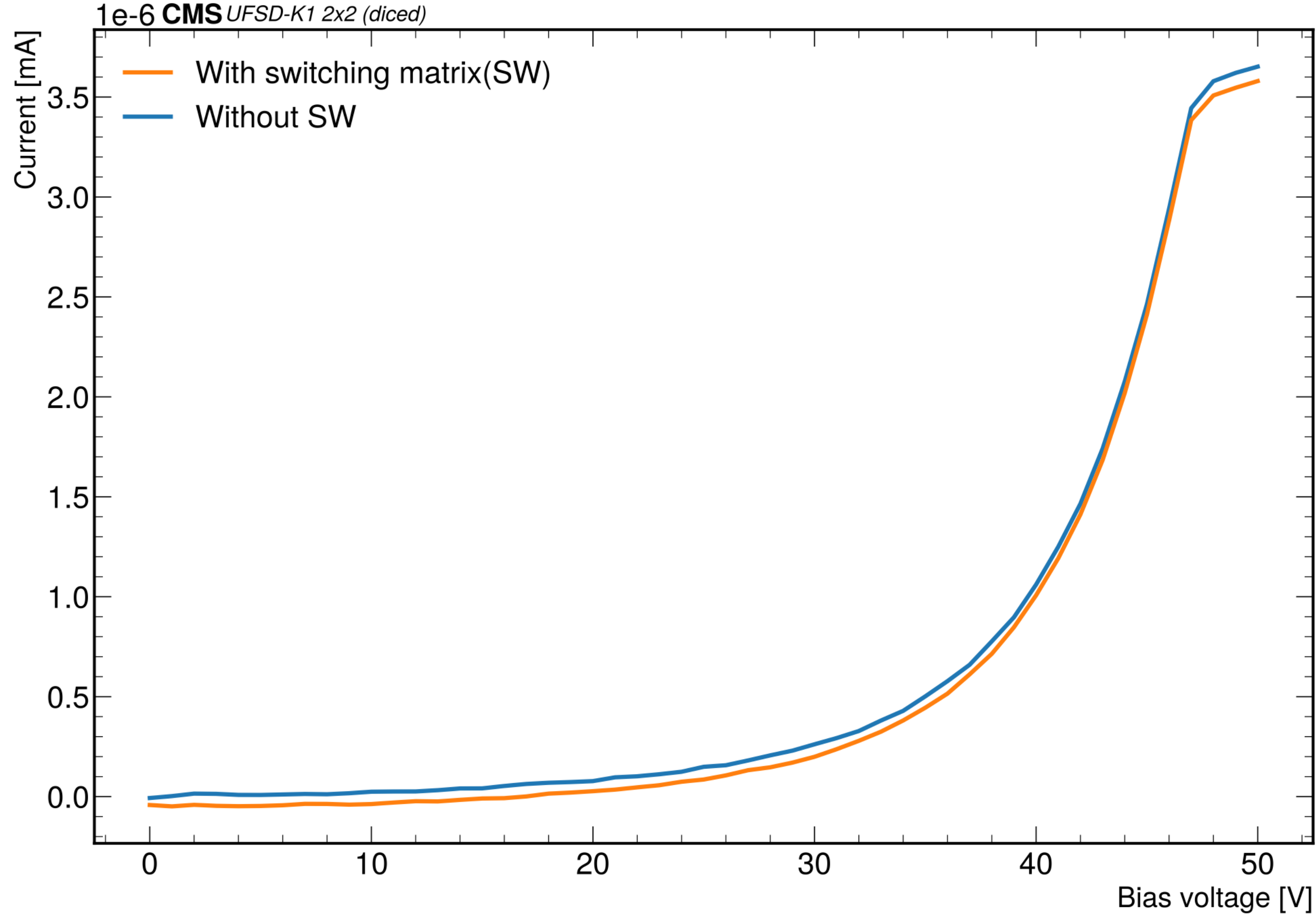






- Tested this design concept using 2x2 LGAD sensor.
- Plan to use this design concept for a module to measure 16x16 sensors.

Switching matrix test on 2x2 sensor



We checked the result with switching matrix is consistent!

IV, CV Measurements Software update

https://github.com/jhkim06/lgad_ivcv/tree/v1_gui

IV Measurement GUI

LGAD Measurements

Switch Matrix | Status | Switch matrix is not ready

IV setup | CV setup

IV measurement

SMU		PAU	
Sensor Name	FBK	Col Number	1
Initial Voltage (V)	0	Row Number	1
Final Voltag (V)	-250	Voltage Steps	1, (-30, -100, 2)
Current Compliance	1e-05		

☑ Return Sweep ☑ Live Plot

Start Measurement

Status IV measurement selected

CV Measurement GUI

LGAD Measurements

Switch Matrix | Status | Switch matrix is not ready

IV setup | CV setup

CV measurement

LCR		PAU	
Sensor Name	FBK	Col Number	1
Initial Voltage (V)	0	Row Number	1
Final Voltag (V)	-60	Voltage Steps	1, (-20, -25, 0.1)
AC Level	0.1	Frequency	1000

☑ Return Sweep ☑ Live Plot

Start Measurement

Status CV measurement selected

- Used column and row number of a pad of a sensor for output file postfix
- Enable variable voltage steps according to voltage range
  - ➢ Expect to reduce IV measurement time later.
  - ➢ Will be useful to study steep curve (ex) near breakdown in IV and full depletion voltage at CV).

Current Korea CMS Activities and Future plan

- Significant contributions to prototyping towards production
- LGADs prototyping and validation
  - Detailed testing of prototype LGADs informed vendor qualification
  - Probe station measurements to verify quality and uniformity of full-size wafers
  - Preparing the test bench setup with probe card and switching matrix
  - Participating various test beam at CERN and Fermilab
- System testing with LGAD+ETROC
  - Will receive 12-inch ETROC2 wafers from CERN
  - Active in System testing with LGAD+ETROC2, including test beam campaigns for validation of the performance of the LGADs +ETROC chain
- LGAD Wafer processing
  - Exploring wafer processing with one of the qualified LGADs vendors for wafer thinning, dicing, and surface preparation at Korean companies for the production phase
- Bump-bonding
  - Process testing with Korean vendors for LGAD-to-ETROC bump-bonding during production
- Module assembly
  - Korean vendor (Memspack) showed excellent performance for module assembly process with the die bonding machine.
  - Plan to irradiation test for encapsulation and glue using the KOMAC test beam October and December.