BNL report

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Introduction

Initial Research (Training, Preparation) for developing an ASIC for Strip-type AC-LGAD (BTOF AC-LGAD)

Motivation

> Development study of Barrel TOF in EIC accelerator experiments

♦Purpose

- Evaluate the performance together with Alessandro, Prithwish, who is developing ASIC+AC-LGAD on site at BNL.
- Reproduce BNL test environment at Hiroshima University after returning to Japan

♦Goal

- Learn how to evaluate ASIC performance. (Also how to evaluate performance with lasers)
- Perform and report the performance evaluation of EICROC0 by myself

EICROC0 (ASIC)

- ◆EIC Reed Out Chip ver.0
- 4x4 channel AC-LGAD readout ASIC designed for precise charge and timing information

Final EICROC specifications :

- 32x32 pixels / ASIC
- •~1 mW/channel
- Charge detection range 1-50 fC
- Timing jitter ~15-20 ps
- Input capacitance : cD = 1-5 pF



Wire-bonded and Bump-bonded AC-LGAD+EICROC0



■ No AC-LGAD (A2 board)

The performance difference between the two is not yet known. This is one of the tests we will be looking into.

Test Bench



Interface board

• Analog data is analyzed through an oscilloscope.

Flow chart

Data acquisition (on FPGA)
Select injected channel, charge value
Threshold scan

Plotting.py (convert .dat file \rightarrow .csv file)

Data check (on PC)

➢referenceValue.csv

>threshold sweep(wide range)

Find an optimal threshold for each charge

Data acquisition (on FPGA)

➢ For analysis, fixed threshold, 10000events

Once you have the data for analysis...

Data Analysis (on PC)
See TDC and ADC distribution
Calculate jitter
Data construction

My Codes

We use a new farmwear made by Dominiqu, Adrien & team (Thanks a lot)

Data Construction



ADC 2025/03/13 (Thu)

ADC -> Waveform



2025/03/13 (Thu)

TDC ADC Hitbit

Every channel has a unique gain \rightarrow Unique threshold for every channel

Data Format: {TDC, ADC, HB} x 8

Th=70 DAC Low threshold



Th=160 DAC Optimal threshold

Event #	Т	А	Н	Т	А	Н	Т	А	Н	Т	А	Н	Т	А	н	Т	Α	н	Т	А	Н	Т	А	Н
52838449618	0	88	0	0	88	0	0	88	0	157	88	0	0	88	0	0	88	1	0	88	0	0	88	0

Th=220 DAC High threshold

Event #	Т	А	Н	Т	Α	Н	Т	А	Н	Т	А	Н	Т	А	н	Т	А	н	Т	А	Н	Т	А	Н
62320292269	0	88	0	0	88	0	0	88	0	0	88	0	0	88	0	0	88	0	0	88	0	0	88	0



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Gain_A

Th_B

Th A

Gain_B

Analysis Code



1. TDC distribution and ADC distribution

- ✓ charge DAC = [0,10, 20, 30, 40, 50, 60] (0.5 fC 24 fC) charge value= [0.5, 4, 8, 12, 16, 20, 24] fC
- ✓ threshold DAC= [250, 280, 310, 340, 370, 400, 430] (I decided the values to look at threshold_sweep)
- ✓ TDC range = 1 1023
- ✓ 10000 events for each charge
- ✓ A2 board (No sensor) and B1 board (Bump-bonded)

2. TDC_sigma and ADC_mean trend with error

(0,0) pixel Analysis charge is injected to a pixel (0,0)

TDC, ADC distributions (for example)



TDC_sigma and ADC_mean trends ([0,0] pixel, without overflow) 14



Sigma tended to take a stable value with a smaller sigma for larger charge value.

Positive proportional relationship between the amount of injected charge and the digital signal.

TDC ADC distributions

Entries: 10000

Mean: 44.60

Sigma: 1.46

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ADC Value [DACu]

55



= 0

 $\mathbf{\Omega}$

N_event: 10000 Entries: 9593 Mean: 488.33 **Sigma(StdDev) : 3.44**



N_event: 10000 Entries: 9593 **Mean: 42.71** Sigma(StdDev) : 1.45 N_event: 10000 Entries: 10000 Mean: 490.25 **Sigma(StdDev) : 1.78** N_event: 10000 Entries: 10000 Mean: 44.60 Sigma(StdDev) : 1.46

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Q = 10



ADC Distribution

Counts

10

10

10

35

.

40

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TDC ADC distributions











ADC Distribution



N_event: 10000 Entries: 10000 Mean: 489.93 **Sigma(StdDev) : 0.58** N_event: 10000 Entries: 10000 **Mean: 52.68** Sigma(StdDev) : 1.45 N_event: 10000 Entries: 10000 Mean: 489.78 Sigma(StdDev) : 0.54

N_event: 10000 Entries: 10000 Mean: 59.77 Sigma(StdDev) : 1.43

TDC ADC distributions

Q = 40





Q = 50





ADC Distribution

N_event: 10000 Entries: 10000 Mean: 492.79 **Sigma(StdDev) : 0.53** N_event: 10000 Entries: 10000 **Mean: 67.00** Sigma(StdDev) : 1.44 N_event: 10000 Entries: 10000 Mean: 494.63 Sigma(StdDev) : 0.64

N_event: 10000 Entries: 10000 Mean: 74.11 Sigma(StdDev) : 1.43

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TDC ADC distributions of EICROC0 (ASIC)



I analyzed the digital signal of EICROC0 by charge injection.

- ✓ TDC sigma tended to take a stable value with a smaller sigma(~13 ps) for higher charge value.
- ✓ ADC distribution appeared to have a positive proportional relationship between the amount of injected charge and the digital signal.

Next to do in HU

- ✓ Replicate what we did at BNL.
- ✓ AC-LGAD + EICROC0(wire-bonded) analysis with radiation source
- ✓ Install the laser system in HU this year.



Back up

Continuity of Time sample

Analog Signal of EICROC0



Hitbit can only be 1 for at most 2 consecutive time samples.

(I will check the digital data of this analog signal)

ADC_mean trend for each time samples

$\Omega = 0$	ADC	[0]	/	AD(C[1]		A	DC[2]		A	NDC[3]		ADC	[4]	A	DC[5]		A	DC[6]	ŀ	ADC[[7]
15909746629	0 44	4 0	(05	6 0		0	51 ()	0	44	0	() 39	0	487	39 ()	0	44	0	(51	1
Q = 10 25131773979	0	42 0		0 5	54 0		0	47 C)	0	39	0	0	39	0	490	41 0		0	45	0	() 50	1
Q = 20 5303621029	1 0	42	0	0	55	0	0	49	0	0	44	0	0	45	0	490	48	0	0	53	0	0	52	1
:																								
Q = 60 7967872197	5 0	34	0	0	44	0	0	39	0	0	42	0	0	59	0	494	79	0	0	80	0	0	50	1

TDC has only one value, so we can extract it. However, ADC has a value in every time sample, so it is necessary to discuss which value should be obtained.

ADC_mean trend for each time samples



The larger the injected charge, the larger the ADC value.

TDC sigma trend for each time sample



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Except Overflow(?) for Q = 0 DACu

11111



All pixel analysis charge is injected to all pixels

Threshold & Charge Correction

Before Correction

Pixels in which we inject signal : All pixels

Threshold values tested : [230 - 330]

Number of cmd_pulse per event : 100

Charge values tested : [12]

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After Correction



 Adjust "vth_cor_opt" by myself while watching Threshold_sweep.

All channels now fall at 270 DACu when charge value is [12]

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No correction threshold sweep (A2 board)



No correction threshold sweep



Threshold and ADC charge correction

#Q = 0 DAC #th = 250 #vth_cor_list = [62, 46, 47, 54, 46, 61, 40, 39, 51, 44, 62, 48, 56, 57, 47, 50] #vref_cor_list = [64, 70, 79, 79, 66, 78, 79, 79, 70, 82, 76, 85, 78, 84, 77, 78]
#Q = 10 DAC #th = 280 #vth_cor_list = [75, 60, 62, 68, 60, 76, 54, 54, 66, 59, 78, 62, 72, 72, 63, 66] #vref_cor_list = [64, 70, 79, 79, 66, 77, 79, 79, 70, 82, 76, 85, 78, 84, 77, 78]
#Q = 20 DAC #th = 310 #vth_cor_list = [79, 54, 56, 62, 55, 71, 50, 48, 58, 54, 83, 56, 65, 65, 56, 58] #vref_cor_list = [64, 70, 79, 79, 66, 77, 78, 79, 70, 82, 76, 85, 77, 83, 77, 78]
#Q = 30 DAC #th = 340 vth_cor_list = [74, 52, 54, 59, 54, 68, 49, 46, 54, 51, 70, 54, 62, 64, 54, 57] vref_cor_list = [64, 70, 80, 79, 66, 77, 79, 79, 70, 81, 76, 86, 78, 83, 77, 78]
#Q = 40 DAC #th = 370 #vth_cor_list = [88, 57, 62, 63, 62, 76, 58, 53, 55, 57, 81, 65, 72, 75, 62, 67] #vref_cor_list = [64, 70, 79, 79, 66, 77, 78, 79, 70, 81, 75, 85, 77, 83, 77, 78]
#Q = 50 DAC #th = 400 #vth_cor_list = [92, 53, 60, 60, 59, 74, 56, 48, 43, 53, 80, 62, 69, 75, 60, 66] #vref_cor_list = [64, 70, 80, 79, 66, 77, 79, 79, 70, 81, 76, 86, 78, 83, 77, 78]
#Q = 60 DAC #th = 420 #vth_cor_list = [93, 44, 53, 51, 54, 69, 52, 41, 23, 47, 79, 58, 64, 72, 53, 62] #vref_cor_list = [64, 70, 80, 79, 66, 77, 79, 79, 71, 81, 75, 86, 78, 84, 77, 79]
#Default #vth_cor_list = [64, 64, 64, 64, 64, 64, 64, 64, 64, 64,

New firmware

A2 Board EICROC0 (No AC-LGAD)

A2 Board (only EICROC0)



A2 Board (only EICROC0)



- I can correct the threshold sweep and charge for Q = 0, 10, 20, ..., 60
- Q = 20 is a bit strange because ch 0, 5, 10 is a bit larger value than my setting value.
- The other charges have roughly the same value but are less efficient, making all-pixel analysis possible.

A2 board TDC ADC distribution (10000 events)



- Q = 0 is no entry (all events are not only one hitbit cell = 1)
- Q = 10 and 20 are very small entries because they are lost in the noise (?)
- ADC distribution looks better

A2 board TDC ADC distribution



Q = 30

Q = 30 and 40 are all entries and small TDC sigma But, in both cases, there are many entries in the 248 DACu bin. The reason is unknown.

A2 board TDC ADC distribution



Q = 50 and 60 are all entries and small TDC sigma But, in both cases, there are many entries in the 248 DACu bin. The reason is unknown. (same for Q = 30, 40)

B1 board (No HV of AC-LGAD)

Correction Values

#=======B1 Board==			==#												
#Q = 0 DAC #th = 250 #vth_cor_list = [30 #vref_cor_list = [64	, 31, , 71,	14, 64,	29, 75,	28, 66,	26, 61,	44, 69,	25, 66,	39, 67,	26, 72,	45, 74,	32, 83,	31, 76,	35, 81,	32, 72,	34] 83]
#Q = 10 DAC #th = 280 #vth_cor_list = [44 #vref_cor_list = [64) , 45, , 71,	28, 64,	44, 75,	42, 66,	34, 61,	52, 69,	35, 66,	53, 67,	34, 72,	54, 74,	46, 83,	46, 76,	50, 81,	46, 72,	50] 83]
#Q = 20 DAC # th = 3 #vth_cor_list = [55 #vref_cor_list = [64	L0 , 54, , 71,	31, 64,	55, 75,	50, 66,	31, 61,	53, 69,	41, 66,	60, 67,	35, 72,	53, 74,	54, 83,	59, 76,	59, 81,	53, 72,	63] 83]
#Q = 30 DAC #th = 340 #vth_cor_list = [68 #vref_cor_list = [64) , 58, , 71,	31, 64,	63, 75,	54, 66,	30, 61,	56, 69,	44, 66,	64, 67,	37, 72,	54, 74,	60, 83,	72, 76,	63, 81,	56, 72,	73] 83]
#Q = 40 DAC #th = 370 #vth_cor_list = [73 #vref_cor_list = [64) , 64, , 71,	30, 64,	68, 75,	58, 66,	31, 61,	62, 69,	48, 66,	70, 67,	42, 72,	58, 74,	67, 83,	80, 76,	67, 81,	60, 72,	80] 83]
#Q = 50 DAC #th = 400 #vth_cor_list = [77 #vref_cor_list = [64) , 70, , 71,	28, 64,	73, 75,	62, 66,	30, 61,	67, 69,	54, 66,	75, 67,	46, 72,	62, 74,	74, 83,	87, 76,	74, 81,	67, 72,	88] 83]
#Q = 60 DAC #th = 430 vth_cor_list = [82, vref_cor_list = [64,) 77, 2 71, 0	26, ' 54, '	79, 6 75, 6	58, 3 56, 6	31, 7 51, 6	74, 9 59, 0	59, 8 56, 6	33, 5 57, 5	51, 0 72, 5	58, 8 74, 8	33, 9 33, 5	94, 8 76, 8	30, 7 31, 7	72, 9 72, 8	96] 33]

New firmware

B1 Board EICROC0 (Bump bonded)

B1 board (No HV of AC-LGAD)



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B1 board (No HV of AC-LGAD)



B1 board TDC and ADC distributions



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AC-LGAD Analysis @HU

AC-coupled Low Gain Avalanche Detector (AC-LGAD)

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Silicon semiconductor detectors capable of achieving the required performance of TOF^[1]

AC-LGAD used for Barrel TOF

- Strip type
- 0.05 x 1 cm² pitch, 64 x 4 ch read out sensor
- 3.2 x 4.0 cm²



Prototype AC-LGAD



Time resolution \rightarrow 30 ps Spatial resolution \rightarrow 30 µm

[1] https://arxiv.org/pdf/2201.07772

Experimental Environment





AC-LGAD signal rate:~ 1 /s

Experiment photos





- 80 µm x 1 cm pitch
- 4 mm x 10 mm size
- 50 ch read out sensor
- 16 ch wire-bonded



Strip type **AC-LGAD** (made by HPK)





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Strip type AC-LGAD Rayout

C1: PMT Signal (Trigger; -150mV)



10 mm

Max Amplitude Histogram



Background Fitting Range: 0 - 5 mV Fitting Function: Gaussian

Channel	Mean [mV]	Sigma
2	2.893 ± 0.005	0.769 ± 0.003
3	3.555 ± 0.005	0.761 ± 0.003
4	3.027 ± 0.005	0.748 ± 0.003
5	2.934 ± 0.005	0.748 ± 0.003
6	2.717±0.005	0.786 ± 0.004
7	2.74 ± 0.005	0.777 ± 0.003
8	3.156 ± 0.006	0.839 ± 0.004

- Total events = 30000
- Filtered by the channel that is max amplitude in each event



AC-LGAD: Bias Voltage (Temperature dependence)



Purpose

Large current and voltage applied to AC-LGAD \rightarrow large load and noise

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- Find the optimum value where the signal becomes large without load
- Bias voltage applied to AC-LGAD depends on temperature^[1]

Result

- Current value surges from around 190 V
- \succ High signal & low current \rightarrow Determined to be -185 V
- \succ Unstable behavior at low voltages \rightarrow depletion layer peculiar to semiconductors is in the process of forming

[1] S. Kita et al, Nuclear Inst. and Methods in Physics Research, A 1048 (2023) 168009

How to evaluate time resolution of AC-LGAD

1. β-rays from 90Sr radiation source irradiated to AC-LGAD and trigger (MCP PMT: ~10 ps)

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- 2. Measure the arrival time difference Δt between the trigger signal and the AC-LGAD signal
- 3. Fit the time distribution of Δt with a Gaussian and calculate the time resolution σ



AC-LGAD time resolution (2nd test)



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EICROCO Analysis @ HU

EICROC0 charge injection Setup



Time jitter Evaluation



I measured signal, noise, rise time. Then, I calculated Time jitter by this formula

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Time jitter evaluation



Pixel / Channel Mapping	Column 0	Column 1	Column 2	Column 3
Line 0	Pixel (0,0)	Pixel (1,0)	Pixel (2,0)	Pixel (3,0)
	#00	#04	#08	#12
Line 1	Pixel (0,1)	Pixel (1,1)	Pixel (2,1)	Pixel (3,1)
	#01	#05	#09	#13
Line 2	Pixel (0,2)	Pixel (1,2)	Pixel (2,2)	Pixel (3,2)
	#02	#06	#10	#14
Line 3	Pixel (0,3)	Pixel (1,3)	Pixel (2,3)	Pixel (3,3)
	#03	#07	#11	#15

↑ Each channel of EICROC0

Time jitter evaluation



Time jitter evaluation

Time Jitter



eform_0_7 Time Jiller: 0.7 ps

#00

orm_4_7 Time Jitter 7 it po

#04

rm_8_7 Time Jiller 5.5 ps

#12

#08

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Backup