5/12日本語ミーティング

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概要

・タイミング信頼性

・ハーフエントリー

タイミング信頼性検証

この分野に関係するシリコンセル

①INTT2(packet_id = 3003) & module = 9 & chip_id = 16

②INTT3(packet_id = 3004) & module = 13 & chip_id = 19

③INTT5(packet_id = 3006) & module = 3 & chip_id = 16

やってること

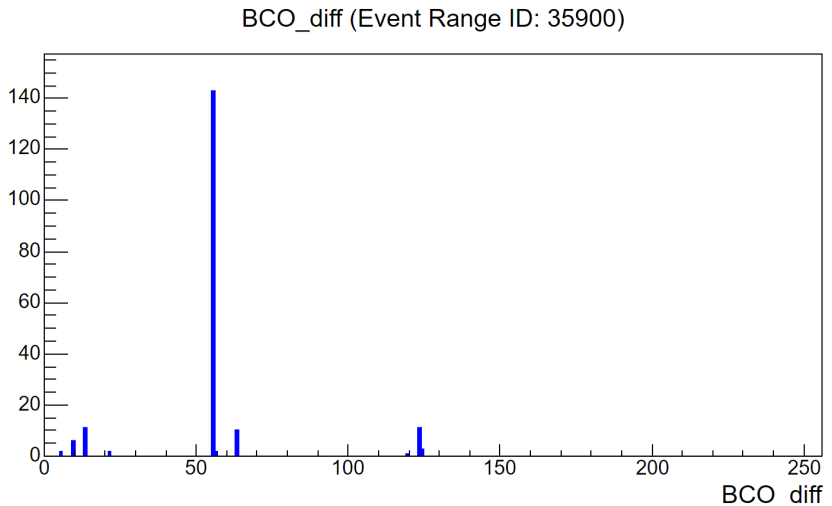
DST INTT Contents

Variables and Accessors under INTTRAWHIT Node [edit | edit source]

INTTRAWHIT table

Type	Name	Description
uint64_t	bco	A 40-bit beam clock counter common across the entire sPHENIX system.
int32_t	packetid	Parameters to indetify servers. The range is 3001 to 3008.
uint32_t	word	Hit parameters before decording ? > Takashi?
uint16_t	fee	Parameter to identify harf ladders. The range is 0 to 13.
uint16_t	channnel_id	Parameter to identify silicon strips within the FPHX chip. The range is 0 to 127.
uint16_t	chip_id	Parameter to identify FPHX chips within a half-ladder. The range is 1 to 26.
uint16_t	adc	ADC value with 3bit.
uint16_t	FPHX_BCO	Value of the beam clock counter in the FPHX chip, ranging from 0 to 127.
uint16_t	full_FPHX	For debug? It is not usually used.
uint16_t	full_ROC	For debug? It is not usually used.
uint16_t	amplitude	Pulse height generated within the ROC used for calibration, with a range of 0 to 64.
uint32_t	event_counter	Event counter?

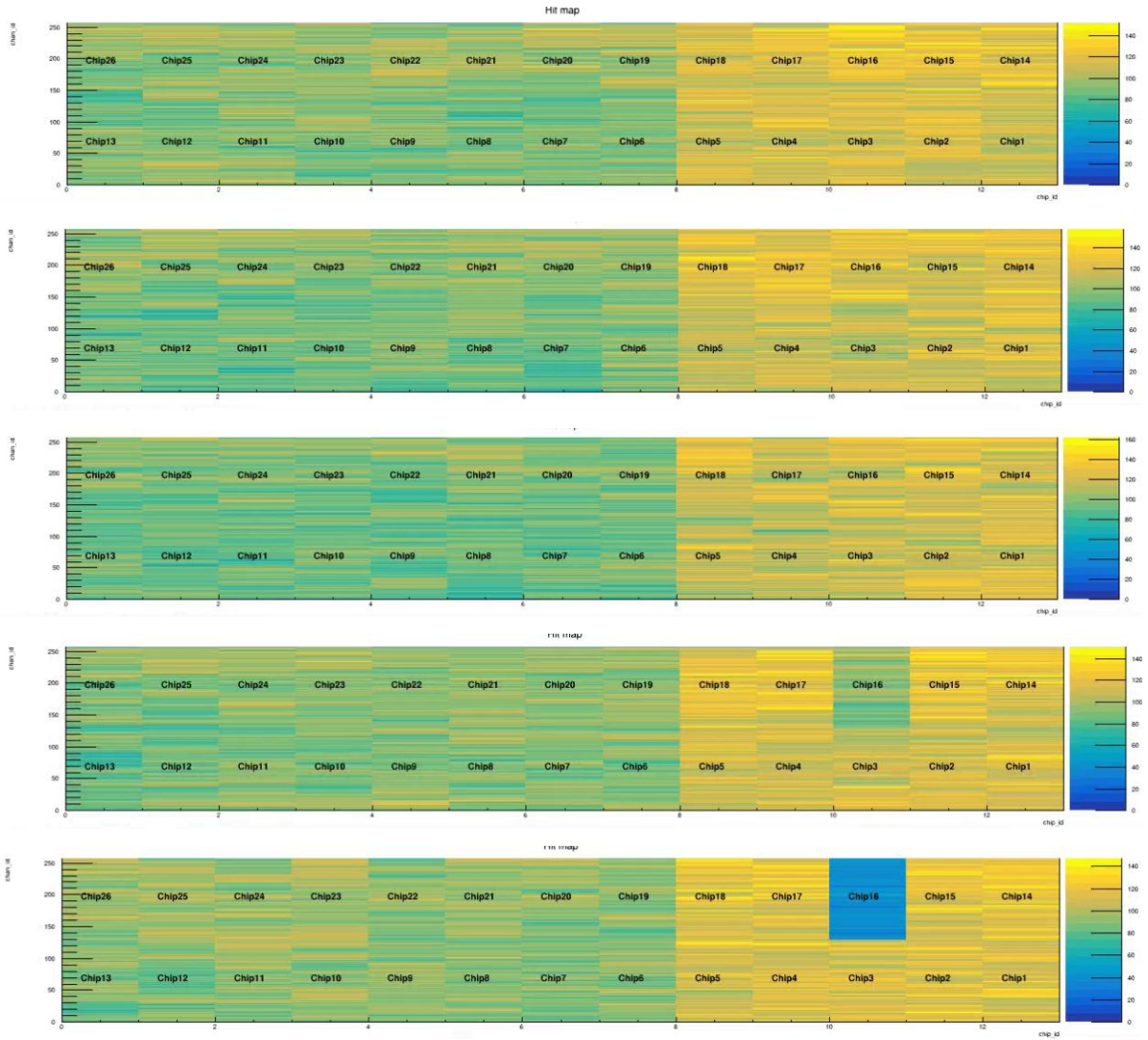
Bco_diff = bco(7ビット分) – FPHX_bco(7ビット)
として、カットをかけたときの振る舞いをみてる



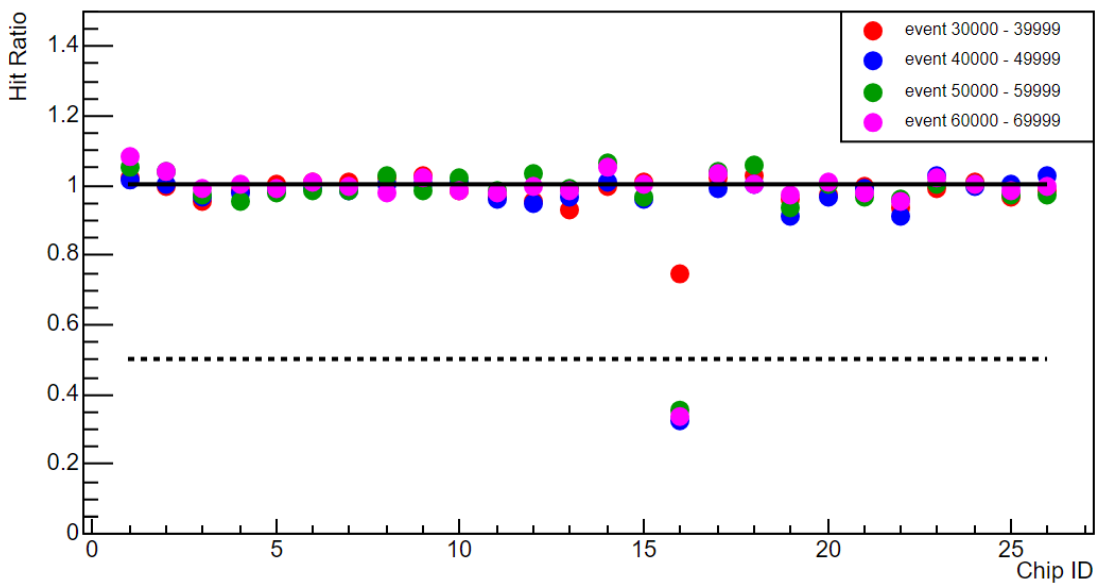
https://wiki.sphenix.bnl.gov/index.php?title=DST_INTT_Contents

タイミング信頼性検証

①INTT2(packet_id = 3003) & module = 9 & chip_id = 16



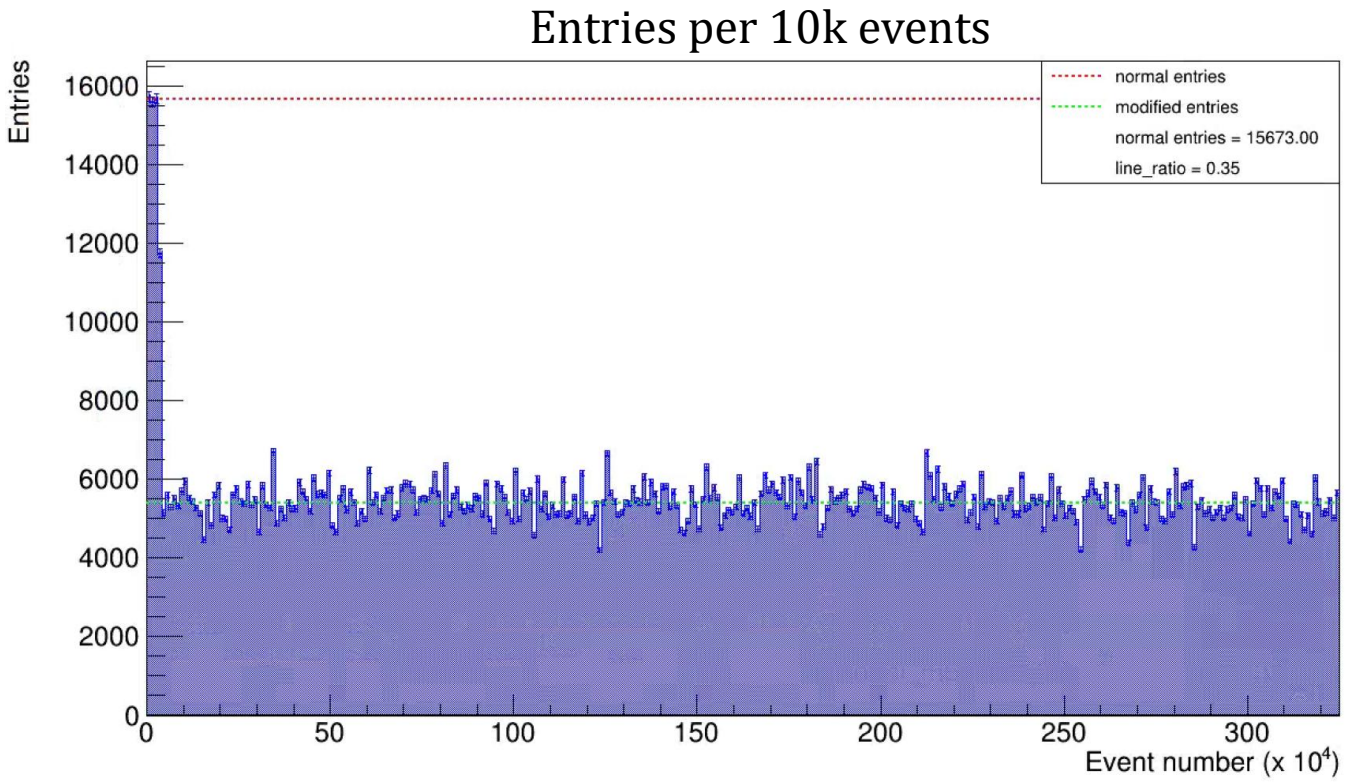
Event number

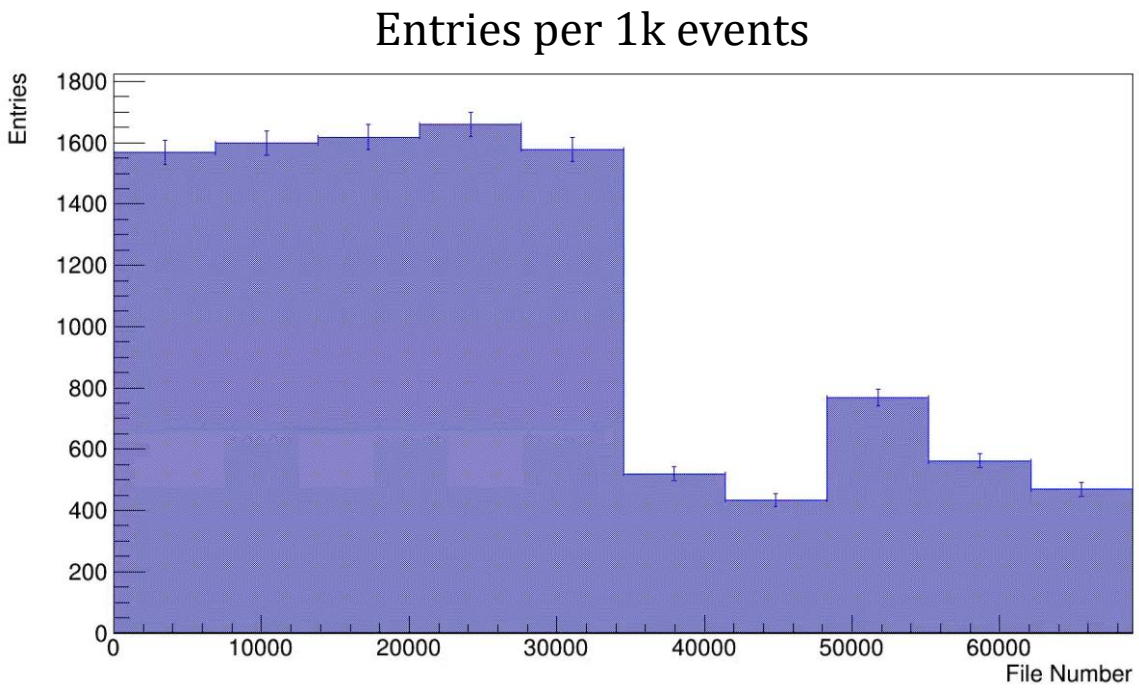


Once the timing was off, it never healed, and number of entries dropped to 35％.

タイミング信頼性検証

①INTT2(packet_id = 3003) & module = 9 & chip_id = 16



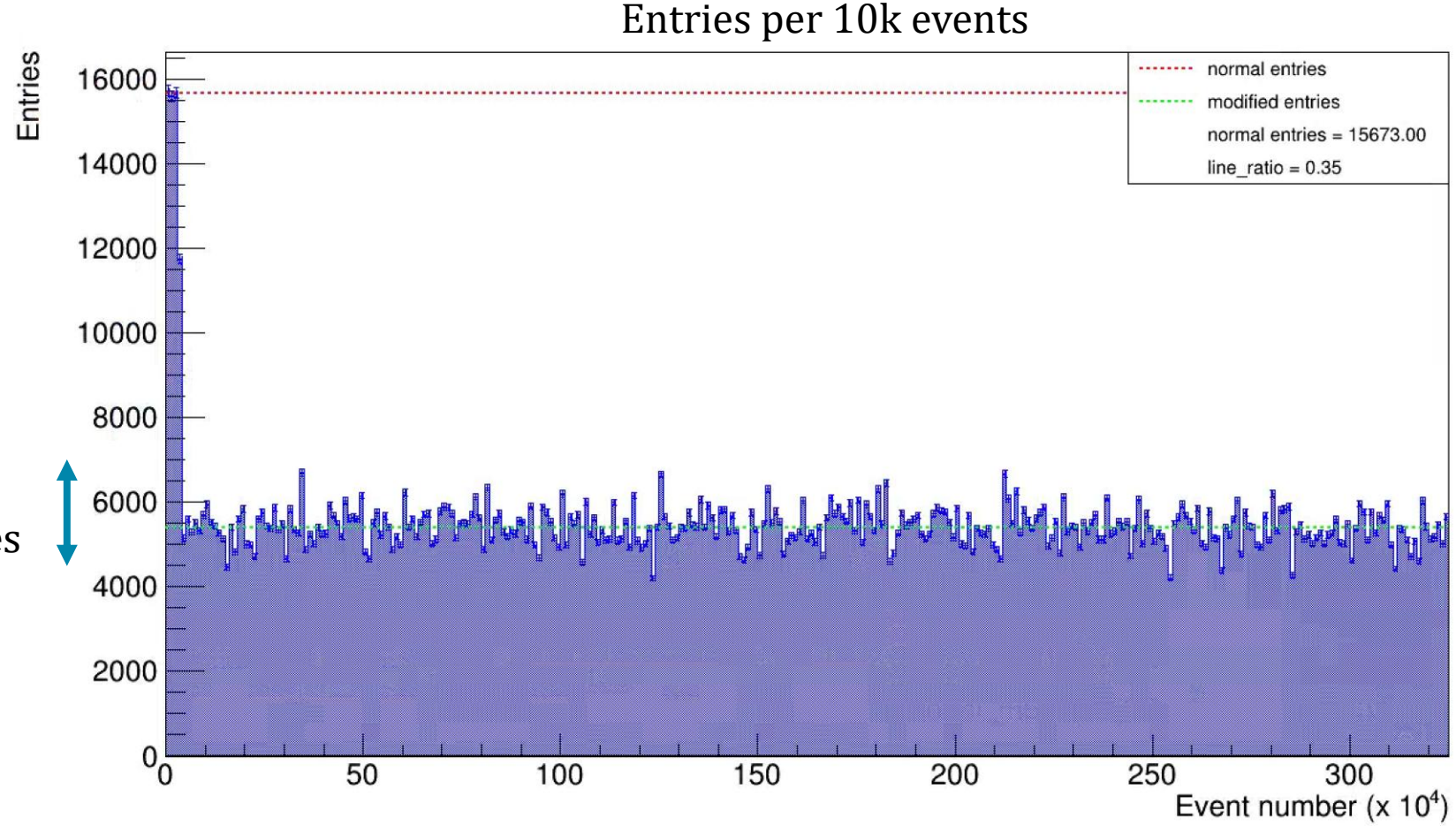


If I narrow the width of the bin, I found that the timing did not get progressively worse, but at the point this problem occurred.

タイミング信頼性検証

①INTT2(packet_id = 3003) & module = 9 & chip_id = 16

25% ～45% entries
compare to normal entries

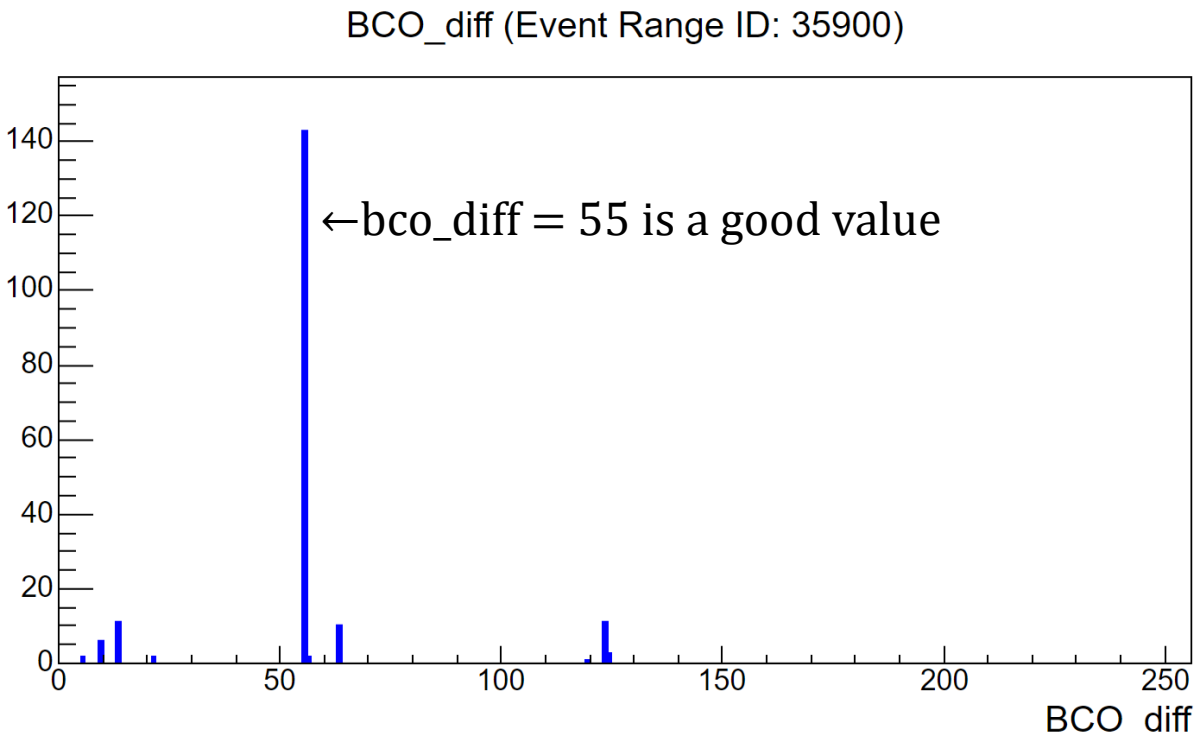


The number of entries differs from event to event, but the number of entries is lower than the half entries.

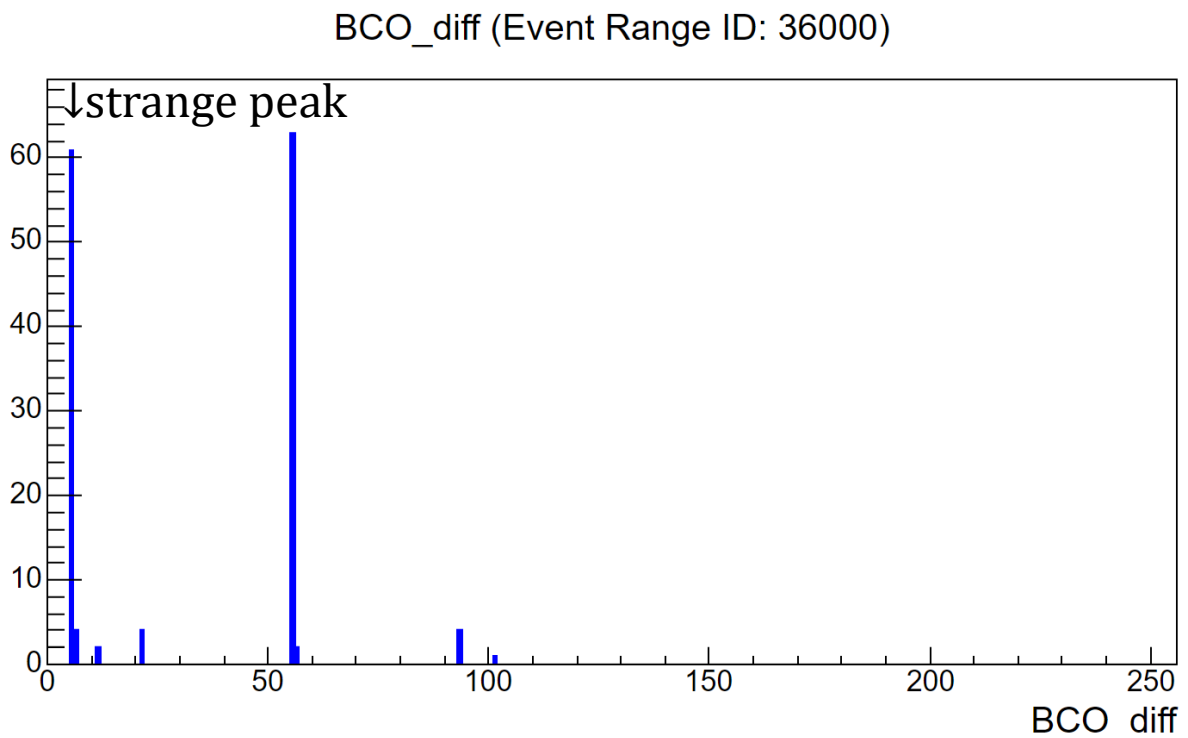
タイミング信頼性検証

①INTT2(packet_id = 3003) & module = 9 & chip_id = 16

bco_diff for each 100 events



Event 35900～35999

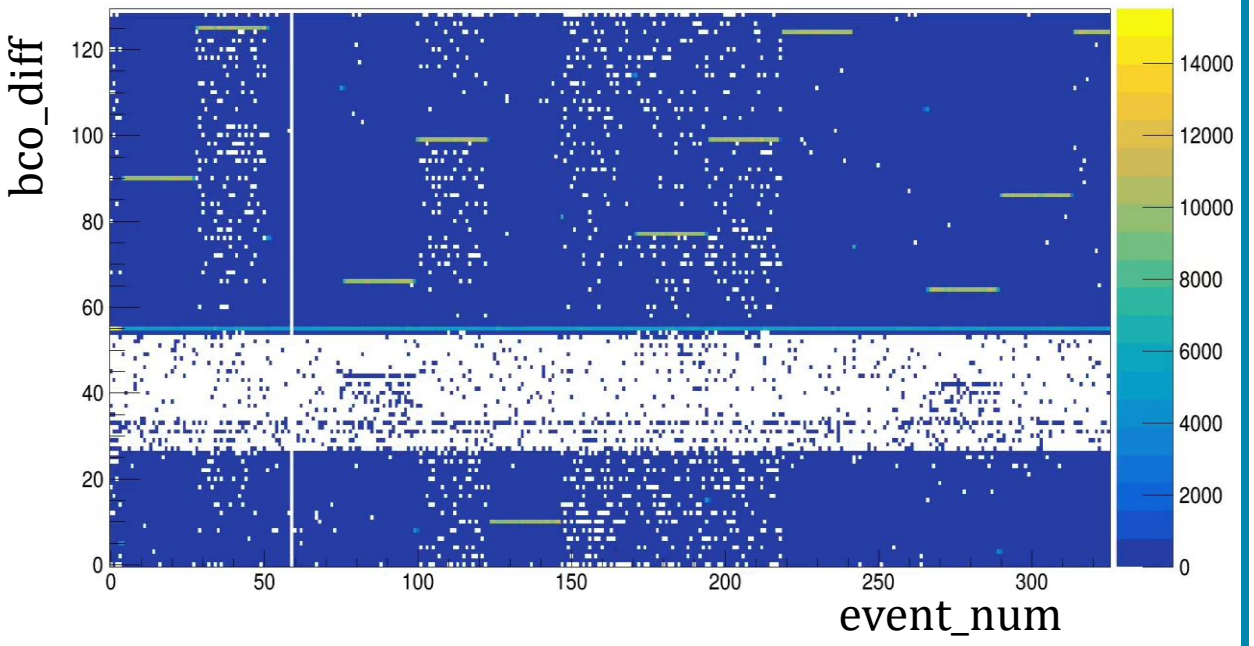


Event 36000～36099

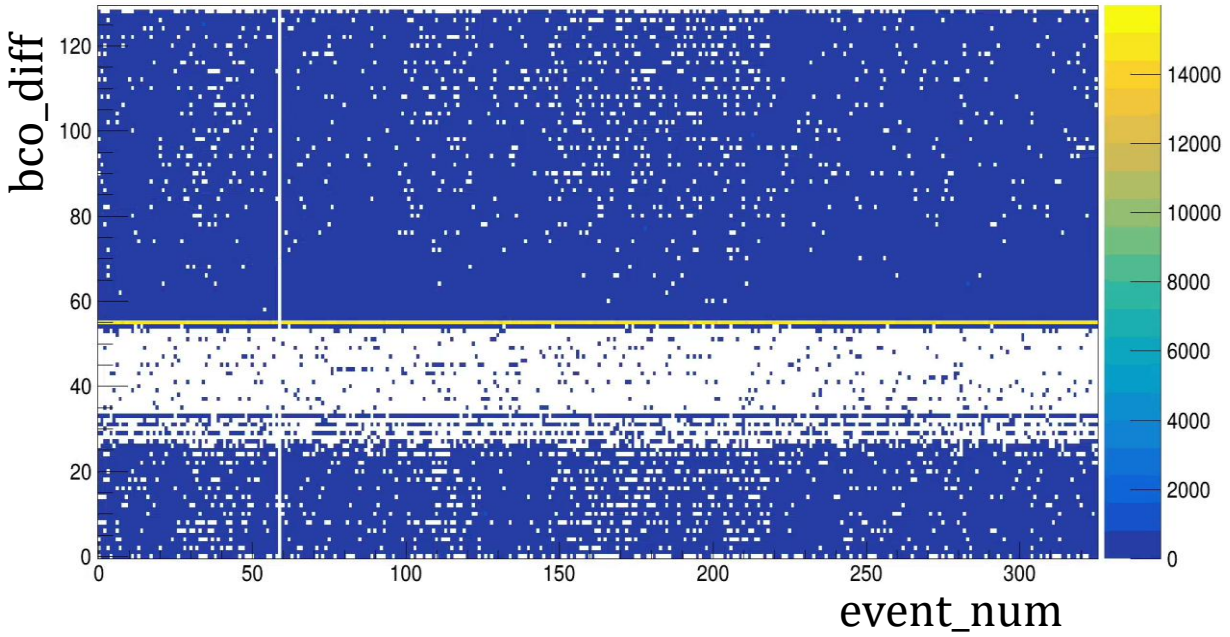
The ratio of entries between two plots (at bco_diff = 55 ± 1) is 0.43 → 43%

タイミング信頼性検証

①INTT2(packet_id = 3003) & module = 9 & chip_id = 16

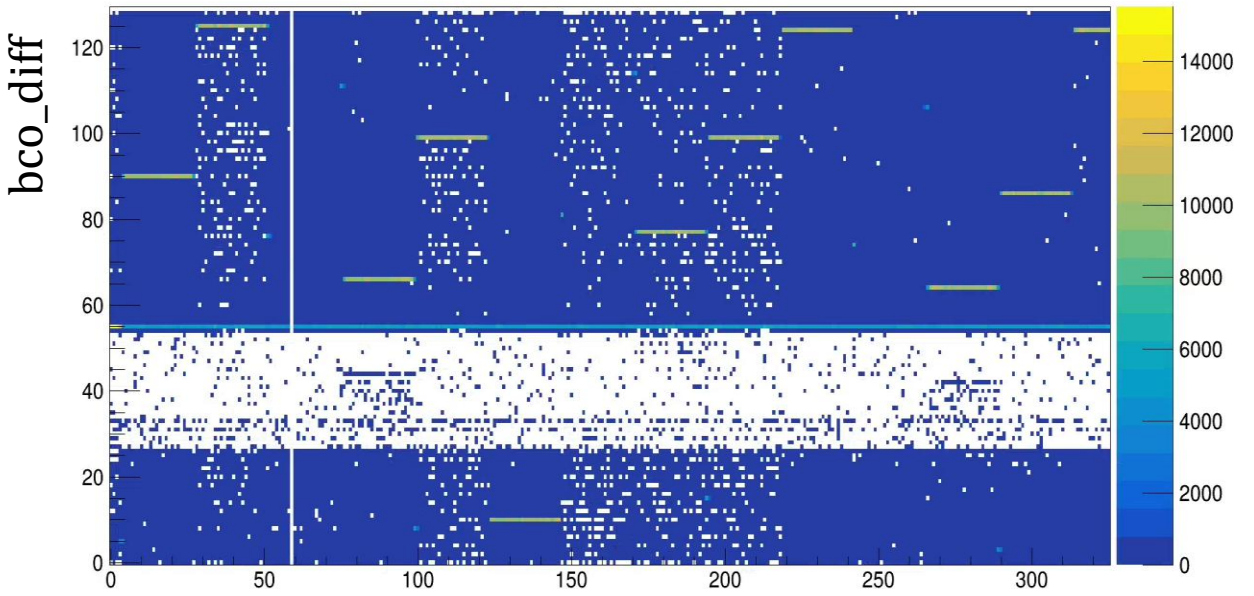


Normal chip
INTT2(packet_id = 3003) & module = 9 & chip_id = 15



タイミング信頼性検証

①INTT2(packet_id = 3003) & module = 9 & chip_id = 16



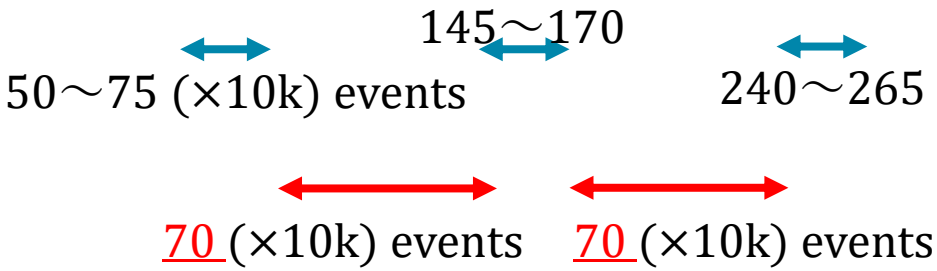
There are three no-peak timing points. (the left figure on the next page)

Oddly, the number of events between peaks was also constant, although with the number of events differing from the length of the peak.

With 10k event breaks, there is a type of beginning and end of peak.

length of the peak is 22 or 23 (×10k) events

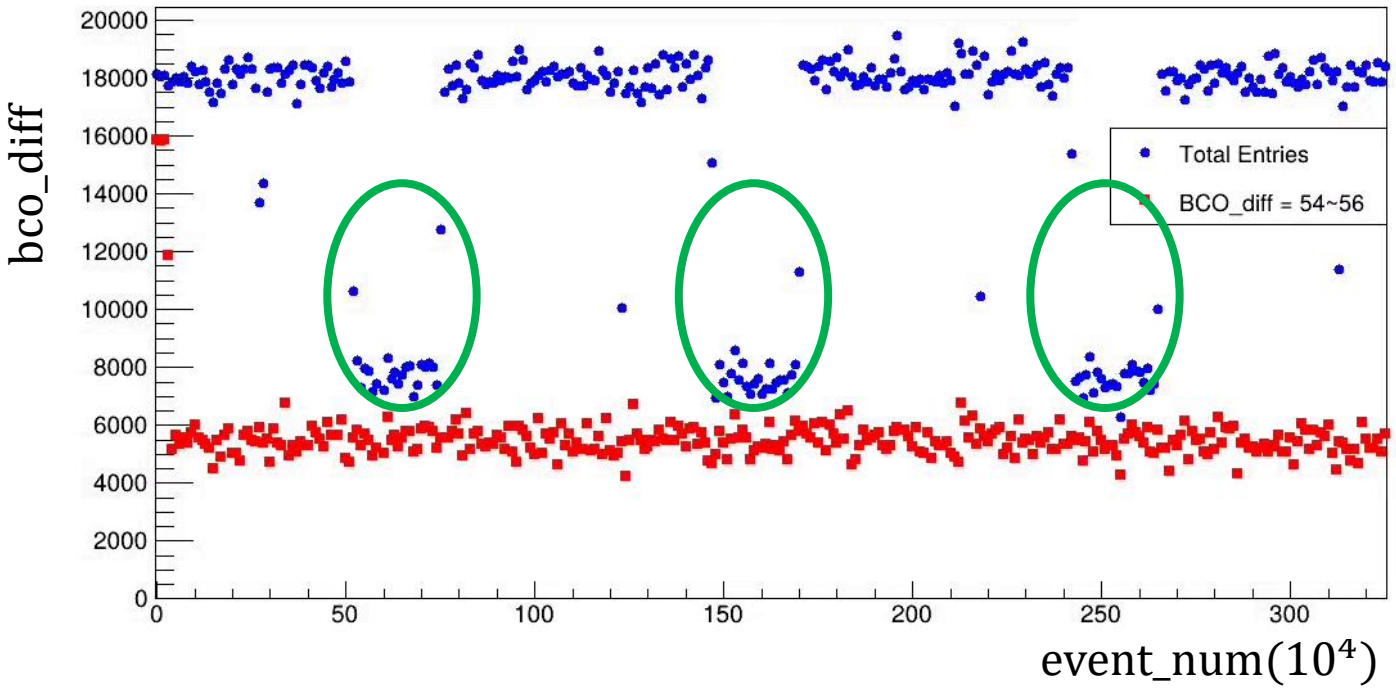
no peak range

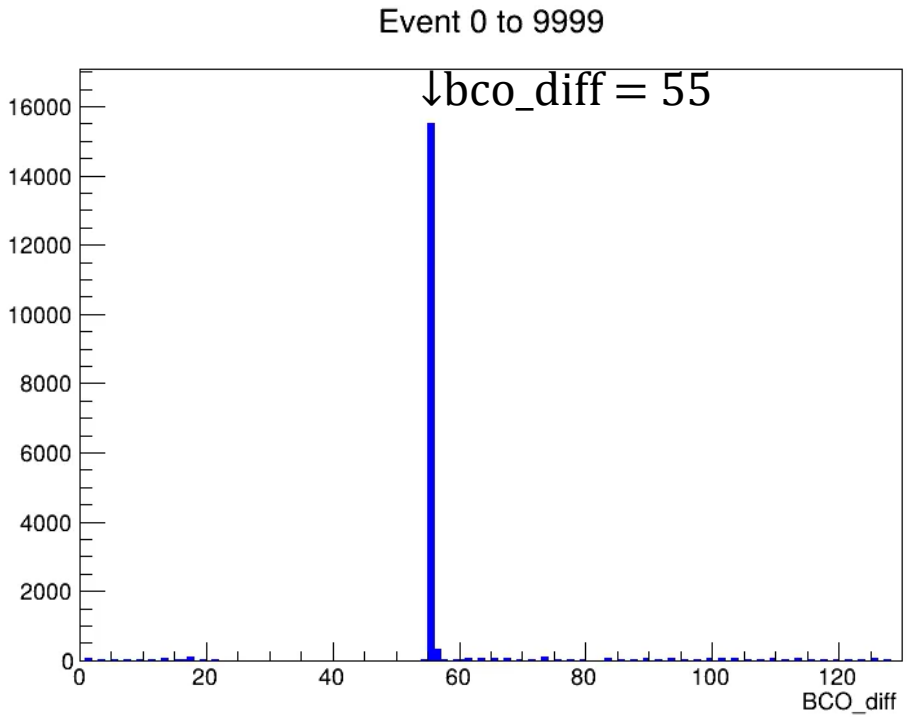


The number of events between no peak regions is also constant.

タイミング信頼性検証

①INTT2(packet_id = 3003) & module = 9 & chip_id = 16





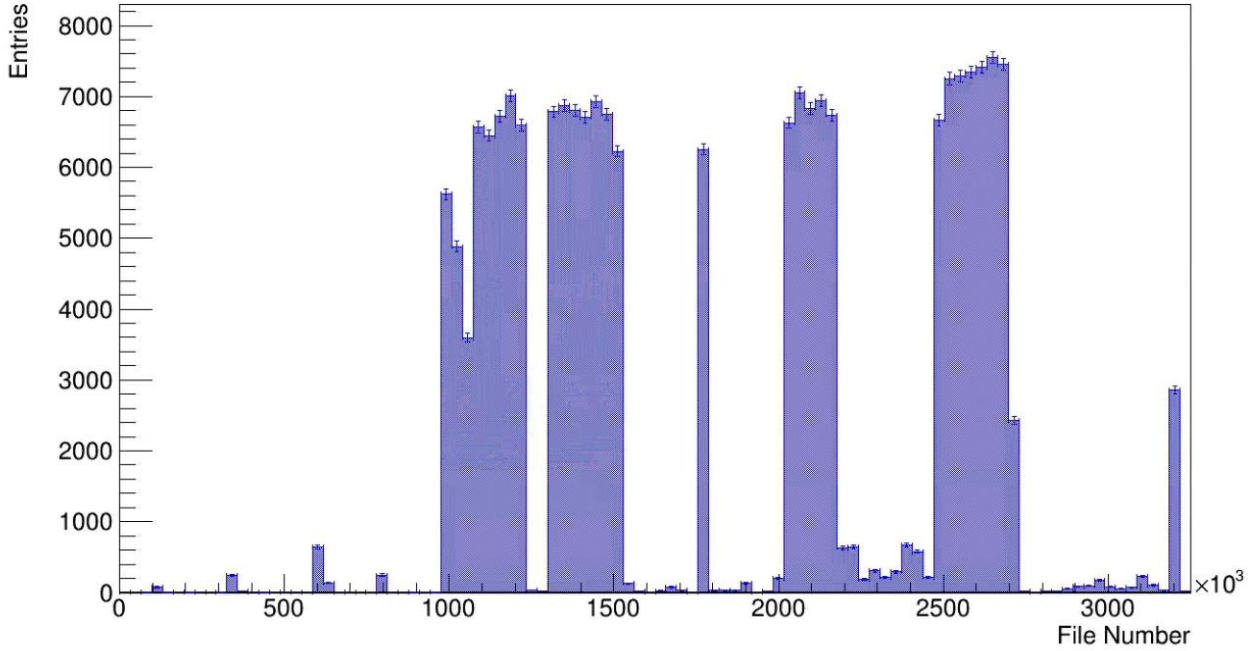
Sorry, I made a mistake that I swiched red and blue compare to the figure on previous page☺.

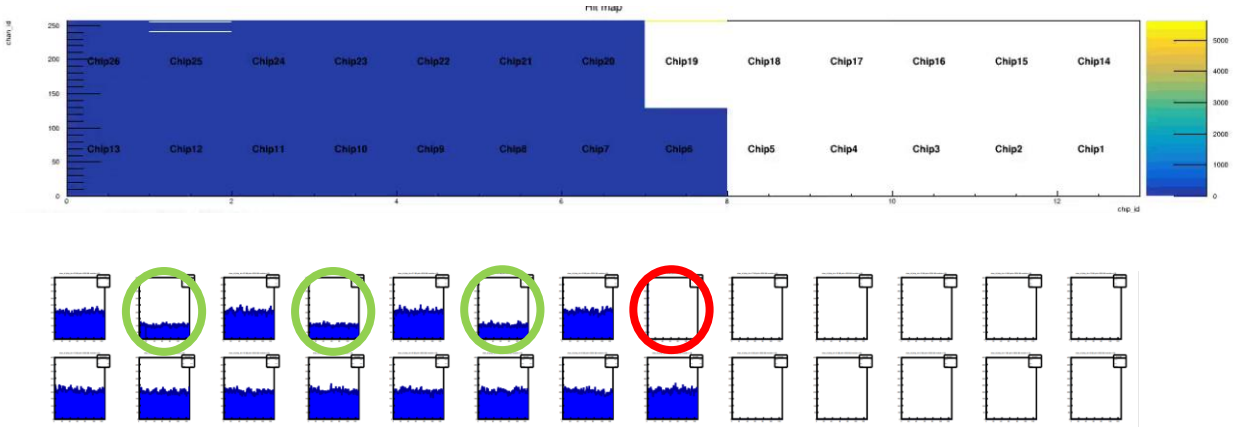
Where there are no strange peaks, total entries are down to begin with.

As Itaru's speculated, this study may have relationship with half-entry issue.

タイミング信頼性検証

②INTT3(packet_id = 3004) & module = 13 & chip_id = 19

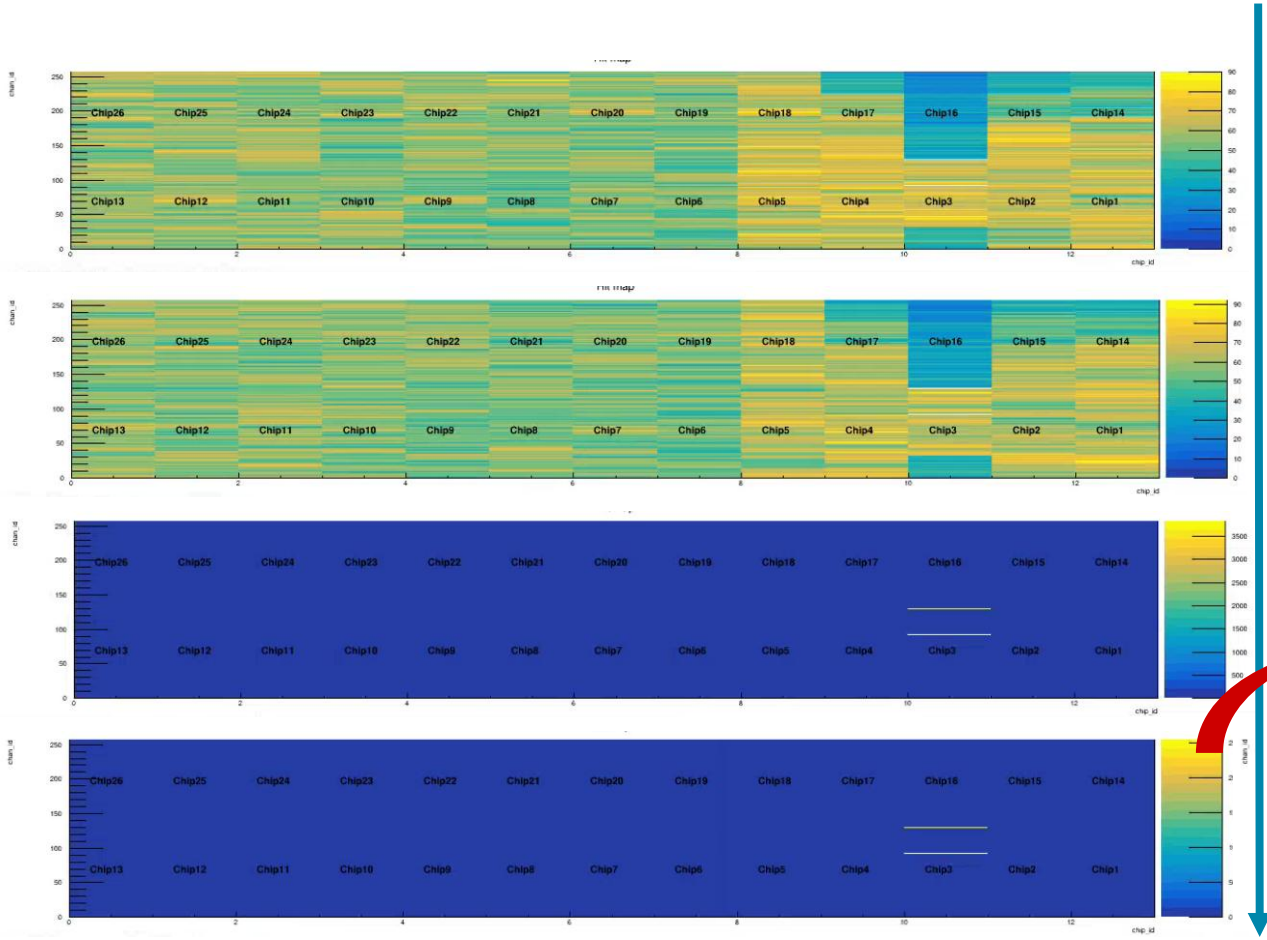




There was chip with varying numbers of entries. However, since this chip is essentially a no-entry-chip, the mask should resolve the issue. Also, the entry was only on chan_id==0.

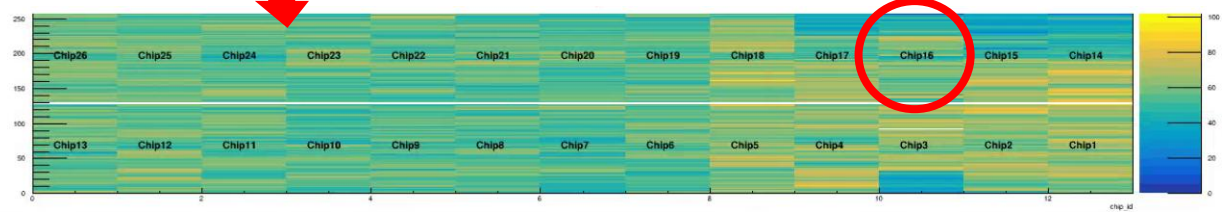
タイミング信頼性検証

③INTT5(packet_id = 3006) & module = 3 & chip_id = 16



beginning, the chip 16 had half -entry issue.
And at some point, this issue was self-recovered.
But in addition, the channel 127 of chip16 became very hot.

cutting channel127

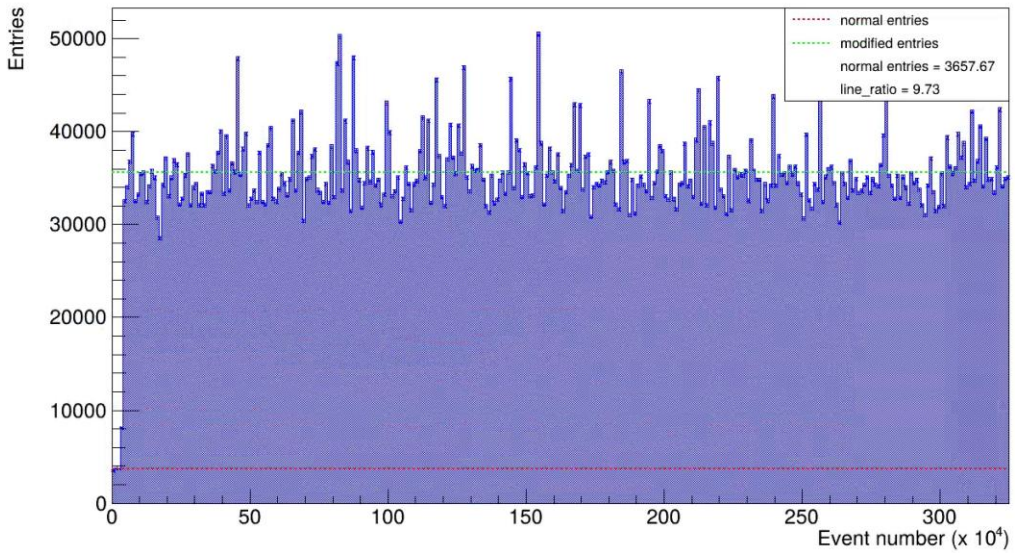


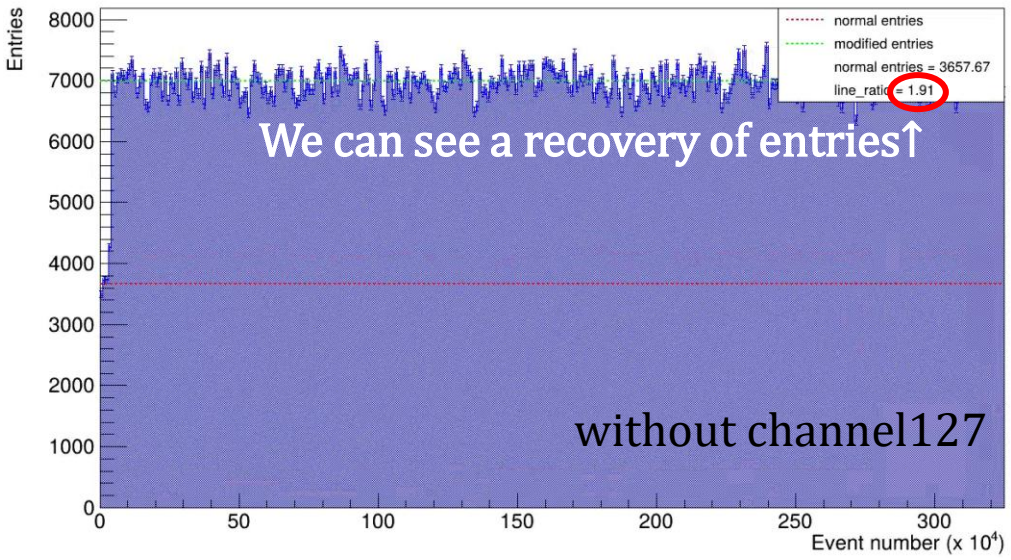
Event number

When it comes to noisy-chip, does half-entry disappear?

タイミング信頼性検証

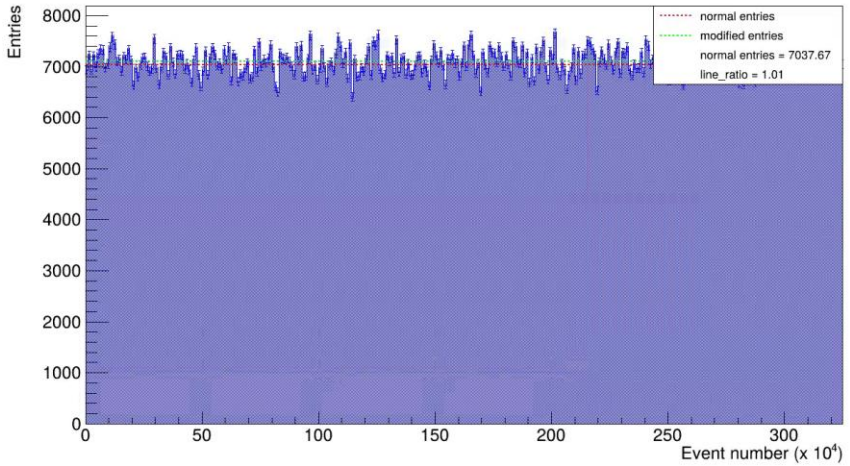
③INTT5(packet_id = 3006) & module = 3 & chip_id = 16



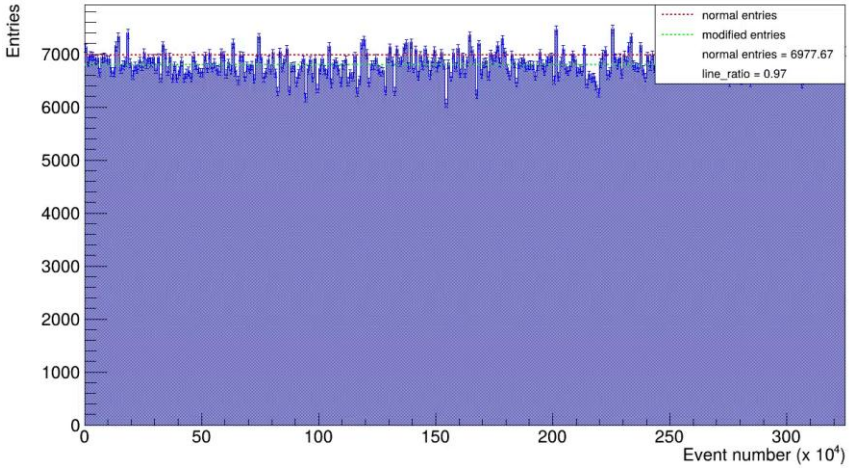


cutting
channel127

chip_id = 17



chip_id = 19

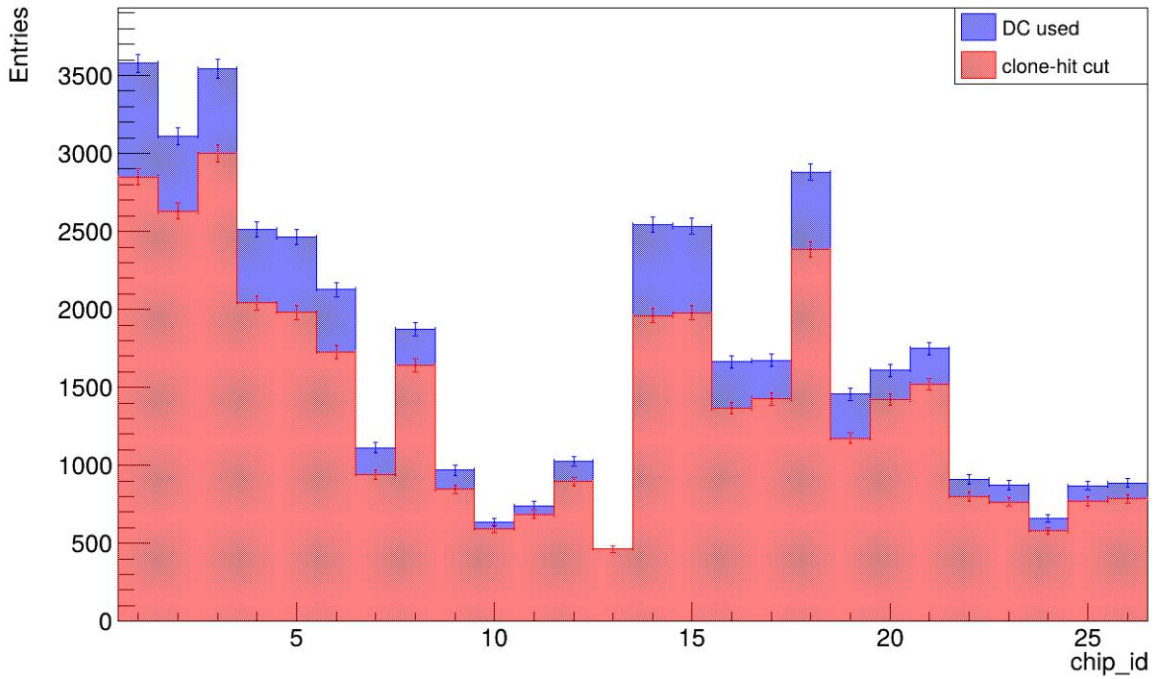


Normal chips are not affected.

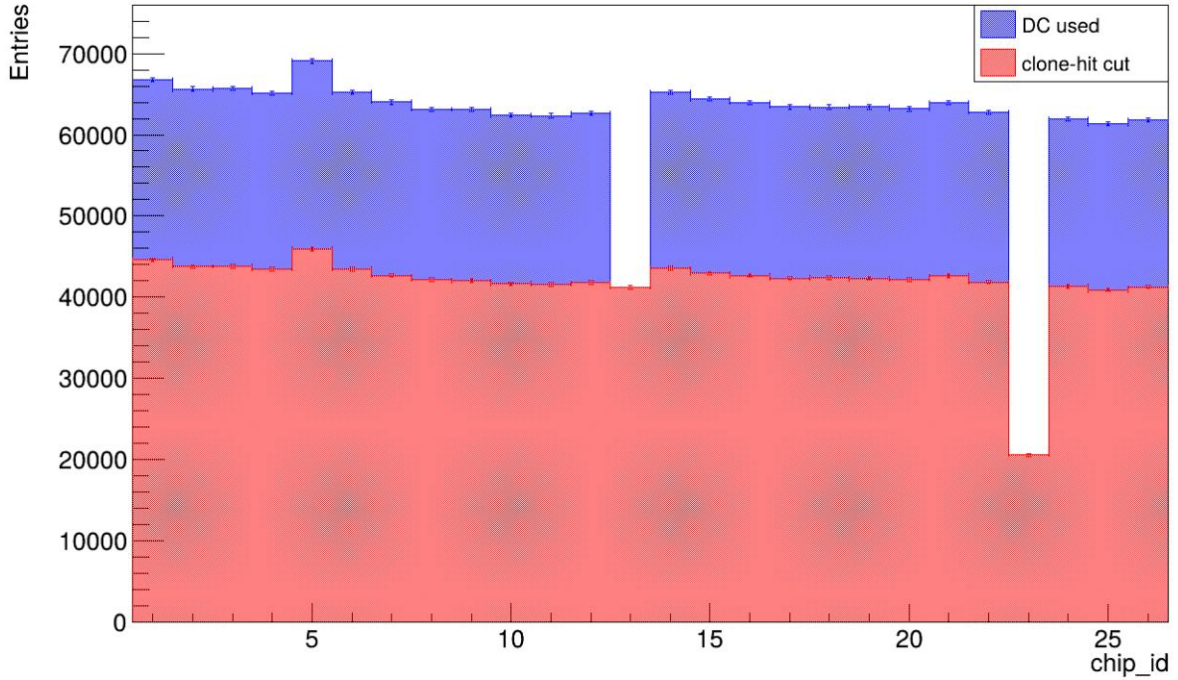
ハーフエントリー

ハーフエントリー

noise data



Calibration test data



- chip13, 23 is half-entry
- Data Using Digital-Control to all chips(Blue data)
- Data from which clone-hit were removed(Red data)

- Applying Digital Control to all chips caused irregular recovery in noise data.
- Even normal chips showed entry count fluctuations.

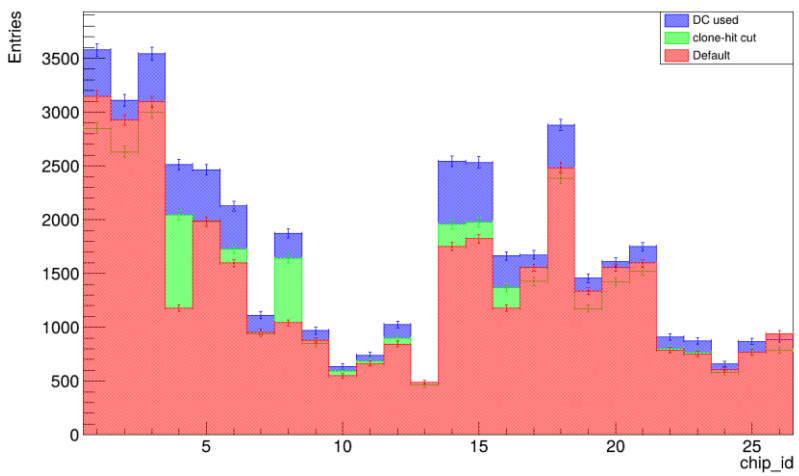
ハーフエントリー

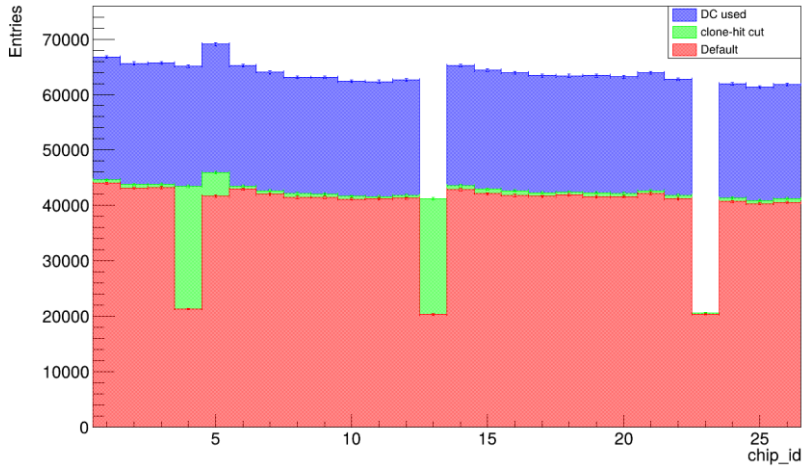
Noise data

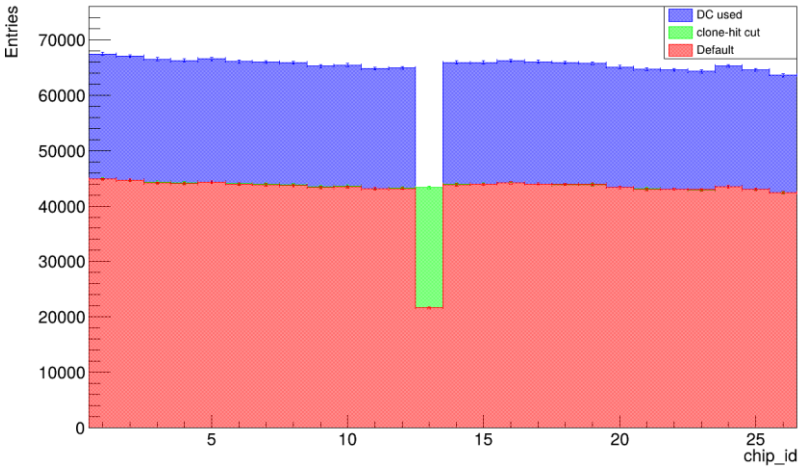
Calibration test data

Bias off

Bias on







A lot ← Noise → A few

ハーフエントリー

やってること

・自分の解析コードをFun4All化
→いまのところDST-fileからハーフエントリーを特定し、ハーフエントリーがあるところのヒットマップを描写