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## The Ladder and Readout Cables of Intermediate Silicon Strip Detector for sPHENIX

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| <b>Abstract:</b>          | <p>A new silicon-strip-type detector was developed for precise charged-particle tracking in the central rapidity region of heavy ion collisions. A new detector and collaboration at the Relativistic Heavy Ion Collider at Brookhaven National Laboratory is sPHENIX, which is a major upgrade of the PHENIX detector. The intermediate tracker (INTT) is part of the advanced tracking system of the sPHENIX detector complex together with a CMOS monolithic-active-pixel-sensor based silicon-pixel vertex detector, a time-projection chamber, and a micromegas-based detector. The INTT detector is barrel shaped and comprises 56 silicon ladders. Two different types of strip sensors of <math>78\text{-}\mu\text{m}</math> pitch and <math>320\text{-}\mu\text{m}</math> thick are mounted on each half of a silicon ladder. Each strip sensor is segmented into <math>8\times 2</math> and <math>5\times 2</math> blocks with lengths of 16 and 20 mm. Strips are read out with a silicon strip-readout (FPHX) chip. In order to transmit massive data from the FPHX to the down stream readout electronics card (ROC), a series of long and high speed readout cables were developed. This document focuses on the silicon ladder, the readout cables, and the ROC of the INTT. The radiation hardness is studied for some parts of the INTT devices in the last part of this document, since the INTT employed some materials from the technology frontier of the industry whose radiation hardness is not necessarily well known.</p> |
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# The Ladder and Readout Cables of Intermediate Silicon Strip Detector for sPHENIX<sup>\*</sup>

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## ABSTRACT

A new silicon-strip-type detector was developed for precise charged-particle tracking in the central rapidity region of heavy ion collisions. A new detector and collaboration at the Relativistic Heavy Ion Collider at Brookhaven National Laboratory is sPHENIX, which is a major upgrade of the PHENIX detector. The intermediate tracker (INTT) is part of the advanced tracking system of the sPHENIX detector complex together with a CMOS monolithic-active-pixel-sensor based silicon-pixel vertex detector, a time-projection chamber, and a micromegas-based detector. The INTT detector is barrel shaped and comprises 56 silicon ladders. Two different types of strip sensors of 78  $\mu\text{m}$  pitch and 320  $\mu\text{m}$  thick are mounted on each half of a silicon ladder. Each strip sensor is segmented into 8 $\times$ 2 and 5 $\times$ 2 blocks with lengths of 16 and 20 mm. Strips are read out with a silicon strip-readout (FPHX) chip. In order to transmit massive data from the FPHX to the down stream readout electronics card (ROC), a series of long and high speed readout cables were developed. This document focuses on the silicon ladder, the readout cables, and the ROC of the INTT. The radiation hardness is studied for some parts of the INTT devices in the last part of this document, since the INTT employed some materials from the technology frontier of the industry whose radiation hardness is not necessarily well known.

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**Table 1**

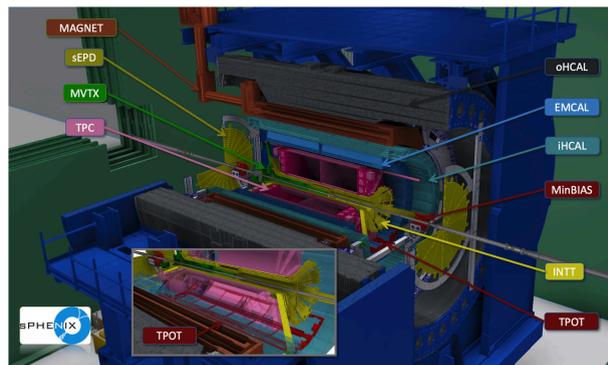
Number of the INTT silicon ladders of the inner and outer layers of the INTT barrel detector.

|                   | Inner | Outer |
|-------------------|-------|-------|
| Number of ladders | 24    | 32    |

## 1. Introduction

The sPHENIX detector [3] at the Relativistic Heavy Ion Collider (RHIC) at Brookhaven National Laboratory, USA, is a major upgrade of the PHENIX detector [2], which was decommissioned in 2017. The sPHENIX experiment collects high-statistics proton-proton, proton-nucleus, and nucleus-nucleus data, enabling state-of-the-art studies of jet modification, upsilon suppression, and open heavy-flavor production to probe the microscopic nature of the strongly-coupled quark-gluon plasma. Such measurements are complementary to those of experiments at the Large Hadron Collider (LHC) at CERN, and will also allow a broad range of cold quantum chromodynamic studies [8].

The sPHENIX detector provides precision vertexing, tracking, and electromagnetic and hadronic calorimetry in the central pseudorapidity region  $|\eta| < 1.1$  with full azimuthal coverage at the full RHIC collision rate of 15 kHz in Au+Au at  $\sqrt{s} = 200$  GeV. A comprehensive assessment of these requirements led to the development of the reference design shown in Fig. 1. In its overall layout, sPHENIX follows the typical geometry of modern collider detectors. The tracking system comprises a CMOS monolithic-active-pixel-sensor (MAPS) microvertex detector (MVTX), a silicon-strip intermediate tracker (INTT), and a time-projection chamber (TPC). For calibration, a micromegas based detector (TPOT) [7] partially covers the outside of the TPC acceptance. The calorimeter stack includes a tungsten/scintillating fiber electromagnetic calorimeter (EMCAL) and aluminum/scintillator and steel/scintillator tile hadronic calorimeter (HCAL), divided into inner and outer parts. The inner HCAL sits inside the 1.4 T superconducting solenoid, which was refurbished from the decommissioned BaBar detector [6].



**Figure 1:** The mechanical drawing of the sPHENIX detector.

This document describes the details of the INTT silicon ladder, its readout cables, and the readout electronics card.

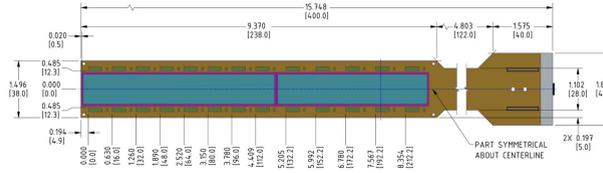
## 2. Detector Overview

The barrel-type INTT detector comprises inner and outer layers of INTT silicon ladders. Adjacent ladders are staggered to prevent dead space in azimuthal acceptance. The inner and outer barrels have 24 and 32 ladders, respectively, as summarized in Table 1. Details of the INTT barrel are beyond the scope of this document, and a separate paper is under preparation.

The designs of the INTT ladder and its readout are constrained by the specification of the FPHX [11, 13, 23] readout chip and the readout card (ROC) of the Forward Vertex (FVTX) detector [4] in PHENIX. Since the INTT reuses the FPHX design and ROCs, the rest of INTT detector was designed to be compatible with these readout chip and electronics. Thus, new copies of FPHX chips were produced for the INTT detector, while the ROCs were recycled.

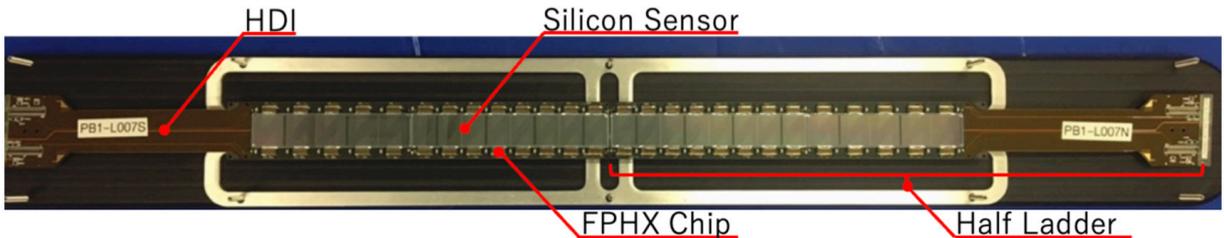
74 The major difference between the FVTX and the INTT detectors is in the mechanical concept. The INTT is a barrel  
 75 type with 2 layers, while the FVTX was a disk type with 4 layers.

76 Two silicon sensors and 26 FPHX readout chips [4, 13, 23] are mounted on a high-density interconnect (HDI)  
 77 flexible print cable to form an INTT silicon module. The schematics of the silicon module are shown in Fig. 2. The  
 78 layout of the silicon sensors and the FPHX chips with respect to the HDI cable is defined in the figure.

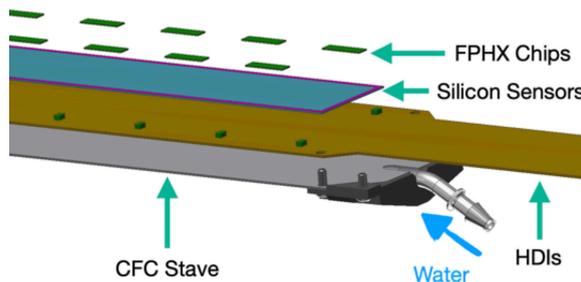


**Figure 2:** Schematics of the INTT module and the dimensions of each components, i.e. the silicon sensors, FPHX chips, and the HDI cable. Dimensions are given in inches, while numbers in brackets are in millimeters.

79 These components of the INTT silicon module and the ladder are summarized in Table 2. Two INTT modules are  
 80 aligned longitudinally and glued to a carbon fiber composite (CFC) support stave to form an INTT silicon ladder, as  
 81 shown in Fig. 3. To show the structures of the INTT ladder, the stackup of the components of the ladder is illustrated  
 82 in Fig. 4.



**Figure 3:** Photo of the INTT ladder with sensors facing up. Note the center line dividing the two halves of the sensor and the rows of FPHX chips along the sensor edges.



**Figure 4:** The stackup of the components of the INTT ladder.

83 Both glue and carbon fiber have high thermal conductivity to diffuse heat generated by the FPHX chips. A water  
 84 cooling system removes heat from the barrel through a carbon tube integrated within the body of the stave. Figure 4  
 85 also shows the tube attached to the edge of the CFC stave, which is an inlet for cooling water.

86 The data of a given ladder are read out from both longitudinal ends for each silicon module. Thus, each HDI cable  
 87 transmits data from half of a ladder. The data are further transmitted downstream from the HDI by a bus extender  
 88 (BEX) cable [14] and a conversion cable (CC). The BEX is a 1.11 meter long flexible print cable (FPC) employing

**Table 2**

The components and total number of channels of the INTT module and ladder. The details of silicon strip sensor type-A and B are discussed in the section 3.1.

|                | Component                | Quantity       |
|----------------|--------------------------|----------------|
| Silicon module | Silicon strip sensor     | 2 (Type-A & B) |
|                | FPHX Chips               | 26             |
|                | HDI                      | 1              |
|                | Total number of channels | 3,328          |
| Silicon ladder | Silicon module           | 2              |
|                | Stave                    | 1              |
|                | Total number of channels | 6,656          |

**Table 3**

The dimensions of type-A and type-B silicon strip sensors [10].

| Item                       | Type-A             | Type-B             | Type-A+B Total     |
|----------------------------|--------------------|--------------------|--------------------|
| Physical dimensions        | 130.0 mm × 22.5 mm | 102.0 mm × 22.5 mm | 232.0 mm × 22.5 mm |
| Active area dimensions     | 128 mm × 19.968 mm | 100 mm × 19.968 mm | 228 mm × 19.968 mm |
| Active area fraction       | 87.4%              | 87.0%              |                    |
| Active cell dimensions     | 16 mm × 19.968 mm  | 20 mm × 19.968 mm  | N/A                |
| # of cells                 | 8                  | 5                  | 13                 |
| Active block dimensions    | 16 mm × 9.984 mm   | 20 mm × 9.984 mm   | N/A                |
| # of blocks                | 16                 | 10                 | 26                 |
| Number of blocks per cell  |                    | 2                  |                    |
| Number of strips per block |                    | 128                |                    |
| Strip pitch                |                    | 78 $\mu$ m         |                    |
| Number of strip channels   | 2,048              | 1,280              | 3,328              |

liquid-crystal polymer as a dielectric material to suppress losses in transmission lines. In both ends, the conversion cable comprises three components; 1)  $\mu$ -coaxial harness, 2) power and ground cables, and 3) connector print boards. The downstream end of the conversion cable is connected to the read-out card (ROC) which collects data from up to seven half-ladders, and then transmits reformatted data to further downstream electronics via an optical fiber connection. The downstream electronics beyond the ROC and data acquisition system are beyond the scope of this document.

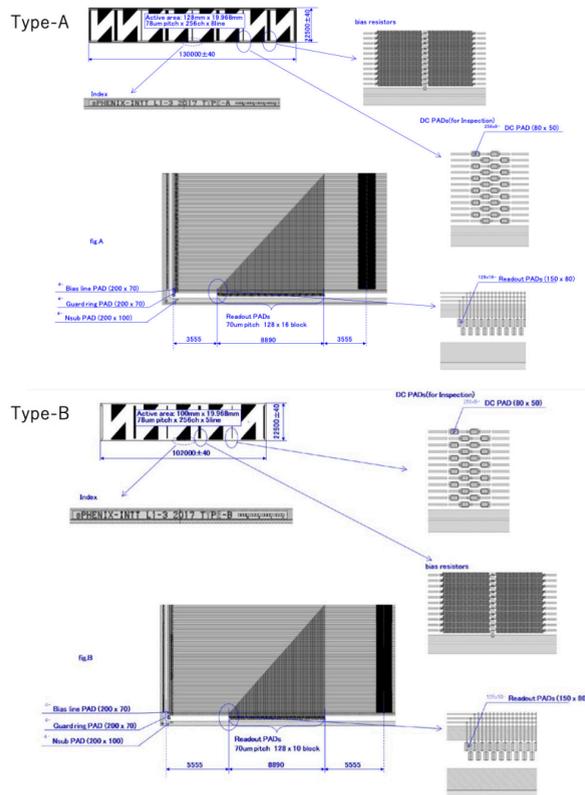
### 3. INTT Ladder

This section describes the electrical components and support systems used to read out and power the INTT. The silicon-strip sensors and the FPHX readout chips are introduced in subsections 3.1 and 3.2, respectively. The HDI that provides power, bias voltage, and slow-control signals to the sensor is discussed in subsection 3.3. The stave support structure is discussed in subsection 3.4. The material budget of the ladder in the radial direction is discussed in subsection 3.5. Lastly, the dead space of the silicon ladder is evaluated in subsection 3.6.

#### 3.1. Silicon Sensors

The silicon-strip sensor [10] is single-sided and AC-coupled. The design is based on and modified from the PHENIX FVTX silicon mini-strip sensors [4]. The sensors (model S14629-01), as well as the FVTX sensors, were fabricated by Hamamatsu Photonics K.K. There are two types of sensors (type-A and type-B), which are distinguished by the length of strips and number of blocks. The type-A sensor has an active area of  $128 \times 19.968$  mm that is segmented into 8 rows and 2 columns of blocks, each of which consisted of 128 strips with 78  $\mu$ m pitch and 16 mm long. Each strip oriented in the longitudinal direction. Similarly, the type-B sensor has an active area of  $100 \times 19.968$  mm that is segmented into 5 rows and 2 columns of blocks, each of which comprises 128 strips in 78  $\mu$ m pitch and 20 mm long that are also oriented in the longitudinal direction. Table 3 summarizes these dimensions.

109 The small gap between adjacent blocks where the DC pads are laid out on the surface is completely active. The  
 110 sensors were fabricated with p-implants on a 320  $\mu\text{m}$  thick n-type substrate. The strips are AC-coupled and biased  
 111 through individual 15 M $\Omega$  poly-silicon resistors to a typical operating voltage of 100 V. The aluminum metallization  
 112 width of the strips is 20  $\mu\text{m}$ , which is wider than the implant width of 10  $\mu\text{m}$ . This provides field-plate protection  
 113 against micro discharges, which are known to grow with radiation-induced increases in the leakage current. These  
 114 specifications of the silicon sensor are summarized in Table 4. The strips are also protected by two p-implant guard  
 115 rings and an n+ region between the guard rings and the sensor edge. These designs follow from the silicon-strip sensors  
 116 of the FVTX [4]. Figure 5 shows details of the sensor layout, including guard rings, bond-pad locations, and mechanical  
 117 fiducial marks.



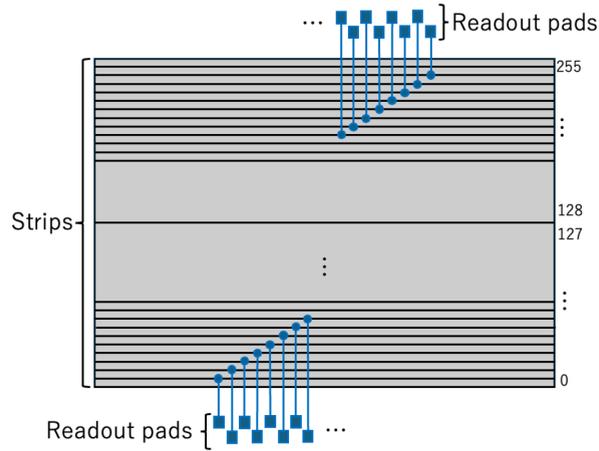
**Figure 5:** The layout design of the type-A (top) and type-B (bottom) silicon sensors [10].

118 In Fig. 6, the strip runs horizontally (longitudinal direction). The readout lines of each strip are wired perpendicular  
 119 to the strips orientation using double-metal technology. The other end of the readout lines are connected to readout  
 120 pads, which transmit data to the FPHX chips using a wire bonding. The strips channel 0 to 127 are wired to the readout  
 121 pads laid out on the bottom of the figure, while the strips from 128 to 255 are wired to the pads on top of the figure.

### 3.2. FPHX chip

123 A custom 128-channel front-end ASIC, the FPHX [11, 13, 23], was developed at Fermilab for use in the PHENIX  
 124 FVTX Detector [4]. The size of the chip is 9 x 2 mm. The chip is operated at 2.5 V and consumes power as low as  
 125 64 mW per chip. The FPHX is a mixed-mode chip with two major and distinct sections: the analog front-end, and the  
 126 digital back-end.

127 The analog section consists of an integration/shaping stage, followed by a 3-bit ADC stage. The FPHX chip  
 128 integrates and shapes signals from 128 channels of strips, digitizes and sparsifies the hit channels for each beam  
 129 crossing, and serially reads out the digitized data.



**Figure 6:** The schematics of the double metal structured strips and their readout lines [10].

**Table 4**

Specifications of the silicon strip sensors [10].

| Item                         | Specification     |
|------------------------------|-------------------|
| SSD type                     | AC-SSSD           |
| Nominal operating voltage    | 100 V             |
| Bias Providing Type          | Poly-Si bias      |
| Poly-Si resistance           | 15 M $\Omega$     |
| Silicon thickness            | 320 $\mu\text{m}$ |
| Strip implant width          | 10 $\mu\text{m}$  |
| Strip readout aluminum width | 20 $\mu\text{m}$  |

**Table 5**

Specifications of the FPHX readout chip [11, 13, 23].

| Item               | Specification      |
|--------------------|--------------------|
| Dimensions         | 9 mm $\times$ 2 mm |
| Operation voltage  | 2.5 V              |
| Power consumption  | 64 mW              |
| Number of Channels | 128                |
| ADC channels       | 3 bits             |
| Data Transmission  | 200 MHz            |

130 The back-end is a novel, triggerless, data-push architecture that permits operation without deadtime and high-  
 131 speed readout with very low latency. It has been designed to process up to four hits within four RHIC beam crossings.  
 132 Although it takes longer, it can process more than 4 hits from a given crossing.

133 A fully processed hit pattern is zero suppressed, and contains a 7-bit timestamp in the unit of RHIC repetition  
 134 frequency 9.4 MHz ( $\sim 1/106$  ns), a 7-bit channel ID, and a 3-bit ADC value. The data word is output over two LVDS  
 135 serial lines in alternating order at a rate of up to 200 MHz. A summary of FPHX specifications [11, 13, 23] is given in  
 136 Table 5.

137 In addition, to be as self-sufficient as possible, the FPHX chip provides its own internal bias voltages and currents  
 138 with minimal external support circuitry. For the user to be able to control the internal parameters and biases, a digital

slow-control interface is provided on each chip to enable programming. Adjustable parameters include gain, threshold, rise time, fall time, input transistor bias current, channel masking, and several additional fine-tuning parameters [23].

### 3.3. High-density interconnects

The HDI is a flexible print circuit board used to read out a half ladder, which comprises two silicon sensors with 26 FPHX chips. The basic layer design of the HDI structure follows from the FVTX [4]. The geometric constraint for the silicon ladder is somewhat less stringent for the INTT than for the FVTX. Thus, the circuit design parameters such as line and space are relaxed from the FVTX, which results in an improved yield rate in the fabricating process.

The HDI was designed by HAYASHI-REPIC Co., Ltd. and fabricated by YAMASHITA MATERIALS CORPORATION in Japan. The width of the HDI is 38 mm in the sensor area and 43 mm at the connector end. The length is 398 mm, which is the longest limit of industry fabrication for the multilayer FPC in an automated manner using dedicated fabrication machines.

The HDI is seven-layered, with each layer comprising 9 μm thick electrolytic copper foil, 12.5 to 50 μm thick polyimide, and 15 to 25 μm thick resin glue. The total thickness is 418 μm in the sensor area. As discussed in subsection 3.5, the total thickness of copper layers is 68 μm, and is the greatest contribution to the material budget of the INTT ladder. The top and bottom copper foil layers were plated with 15 μm of copper<sup>1</sup>. The cross section of the seven-layer structure of the HDI is shown in Fig. 7.

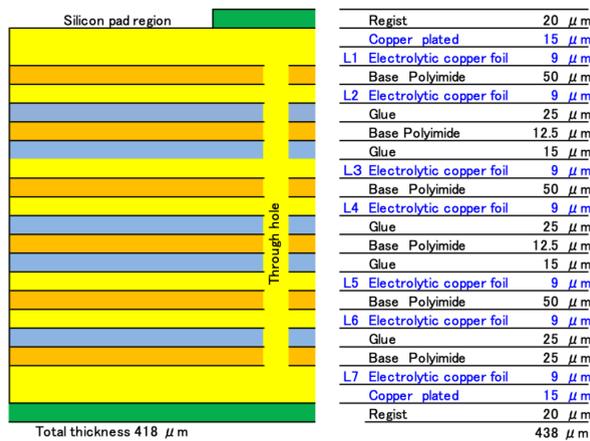


Figure 7: Seven layer structure of HDI.

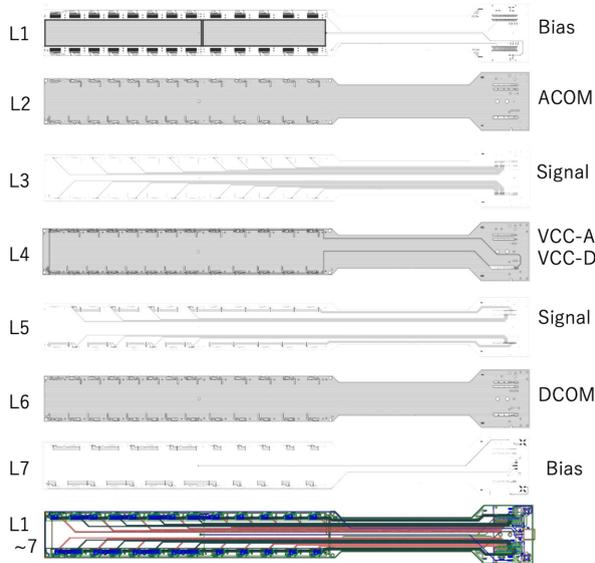
The schematic of each layer is shown in Fig. 8. From top to bottom, each layer is for: transmitting bias for the type-B silicon sensor (L1), analog ground (L2), signals (L3), DC power for the analog and digital parts of FPHX (L4), signal (L5), digital ground (L6), and for the type-A sensor and signals (L7). There are two thermostats implemented on the L7 to monitor the cooling status of heat generated during operation from the FPHX chips.

There are 122 signal lines per HDI cable: 52 pairs of output data lines, 8 pairs of slow-control & clock LVDS lines, and two dedicated lines to inject calibration pulses to the FPHX. Signal transmission lines are mainly placed in layers 3 and 5 to be shielded from external electromagnetic (EM) fields by keeping these layers between solid-copper layers which are assigned for either analog or digital grounds or the DC power. The line and space are both 60 μm. The characteristic impedance is designed to provide a 100 Ω differential for these LVDS pair lines to ensure matching with the rest of the readout cable chain.

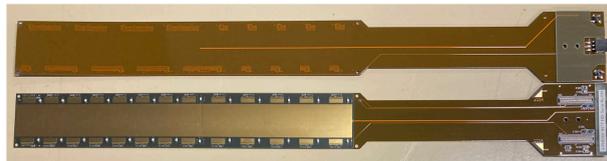
Some signal lines in the sensor region L7 are not of the same design as in the FVTX. These signal lines were changed to keep the HDI width as narrow as possible and would not have otherwise fit within the signal layers. This narrow width enables the barrel detector to be as round as possible by minimizing physical interference between adjacent ladders. Because the back plane of L7 is not shielded by the solid foil ground nor the power layers, the signal lines are exposed to external EM fields. Thus, the length of the lines were kept as short as possible (centimeter lengthscale).

<sup>1</sup>The copper plate was 15 μm thick for the 1st and 2nd batches of the HDI production. The thickness increased to 25 μm for the 3rd batch in HDI production. The total radiation length of the silicon ladder was increased by 3%.

170 Figure 9 shows a photo of the HDI cables with L1 and L7 face up. Table 6 summarizes the major specifications of the  
 171 HDI cable.



**Figure 8:** The schematic of each layer of the HDI. The ACOM and DCOM layers provide analog and digital grounds to FPHX chips, respectively. The 2.5 V power lines for the analog and digital parts of the FPHX chip are electrically isolated from each other within L4. The bottom schematic figure shows (in different colors) the overlay of line patterns for all seven layers.



**Figure 9:** Photo of the HDI cables with L1 face up (bottom) and L7 face up (top).

172 Pairs of connectors for data, LV power for the FPHX, and grounds are implemented in the end of the HDI. The  
 173 model of data connector is the Hirose Co. DF18C-100DP-0.4V(51) plug, which consists of 100 channels with a 400  $\mu\text{m}$   
 174 pitch between conducting pins. Also, there are two bias connectors and a 3-pin thermostat connectors implemented in  
 175 the end of the HDI.

### 176 3.4. Stave

177 The stave is a mechanical support made mainly of carbon fiber composite (CFC) skins. The stave itself, plus an  
 178 extension for mechanical attachment, spans 497 mm long and 38 mm wide. This matches the HDI width around the  
 179 sensor area and accommodates two silicon modules per stave, forming the INTT silicon ladder. The heat load expected  
 180 from each half ladder is 64 mW  $\times$  26 FPHX chips, or approximately 1.7 W. The total heat load over the entire INTT  
 181 is about 186 W for 112 half ladders.

182 The stave is required not only for the rigidity of the support structure, but also for high thermal conductivity to  
 183 dissipate local heat generated by the FPHX chips. The main component of the stave is made of a carbon fiber reinforced  
 184 plastic prepreg (CFRP). The GRANOC prepreg sheet model NT91500-520S of Nippon Graphite Fiber Co. was used,  
 185 which comprises 25R epoxy and XN-90 carbon fiber with a high thermal conductivity of 500 W/mK, with resin  
 186 weight fractions of 20% [17]. The thickness of 0.10 mm with density of 2.19 g/cm<sup>3</sup> prepreg provides satisfactory

**Table 6**

Specifications of the HDI cable. The characteristic impedance is for the LVDS pair.

| Item                                | Specification  |
|-------------------------------------|----------------|
| Dimensions                          | 398 mm × 38 mm |
| Width of connector ends             | 43 mm          |
| Total thickness (sensor pad region) | 418 μm         |
| Conductive material                 | Copper         |
| Dielectric material                 | Polymide       |
| Number of layers                    | 7              |
| Number of signal lines              | 122            |
| Line and space                      | 60 μm & 60 μm  |
| Characteristic impedance            | 100 Ω          |

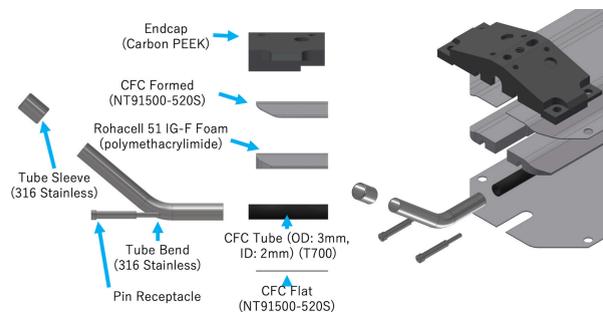
**Table 7**

Specifications of the CFRP prepreg.

| Item                  | Specification          |
|-----------------------|------------------------|
| CFRP prepreg          | NT91500-520S [17]      |
| Carbon fiber          | XN-90                  |
| Resin                 | 25R epoxy              |
| Resin weight fraction | 20 %                   |
| Density               | 2.19 g/cm <sup>3</sup> |
| Thermal conductivity  | 500 W/mK               |
| Tensile module        | 860 GPa                |
| Tensile strength      | 3430 MPa               |
| Thickness             | 100 μm                 |

187 mechanical strength with tensile module and strength of 860 GPa and 3430 MPa, respectively. Table 7 summarizes the  
 188 specifications of the CFRP prepreg.

189 Figure 10 shows the stack up of the stave and the mechanical attachments of its edge. The shells of the stave are  
 190 CFC plates at the top and bottom are flat and formed, respectively. The formed plate is U-shaped to accommodate  
 191 the 3 mm diameter cooling tube between two CFC plates with 3 mm thick ROHACELL 110 RIST form [9] that tapers  
 192 down near the edge forming a structural core. The cooling tube is made of Toreyca T700C carbon fiber prepreg [21]  
 193 fabricated by Kimuraya Co., Ltd., Japan. The NT91500-520S sheet is unidirectional with high thermal conductivity. To  
 194 provide omnidirectional rigidity, each CFC plate has three unidirectional sheet layers with high thermal conductivity  
 195 oriented in longitudinal, transverse, and longitudinal directions. The thickness of the CFC plate is 0.33 mm and the  
 196 total thickness of the stave is 3.76 mm.



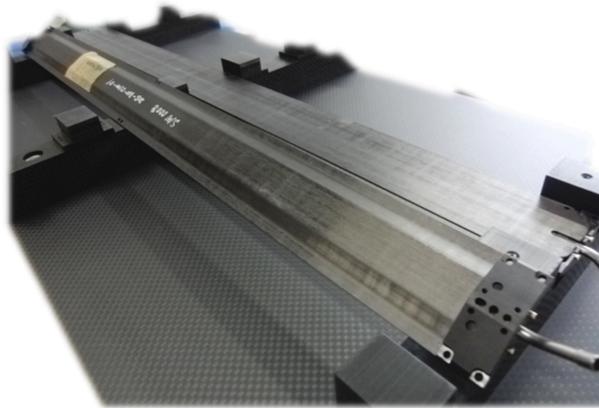
**Figure 10:** The mechanical design of the edge of the stave. The HDI is assembled on the bottom flat CFC plate.

**Table 8**

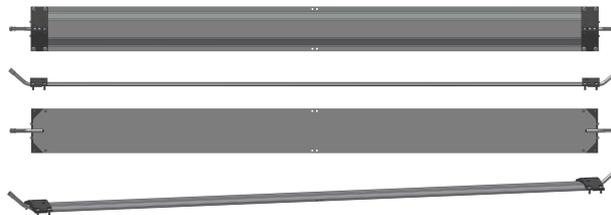
The material list of stave components and specifications. The total thickness is at the sensor region.

| Item                        | Model/Specification      |
|-----------------------------|--------------------------|
| Dimensions                  | 497 mm × 38 mm           |
| Total thickness             | 3.76 mm                  |
| Adhesive for stave assembly | MasterBond EP75-1 [15]   |
| Structure core              | ROHACELL 110 RIST [9]    |
| End cap                     | Ketron CA3 PEEK [16]     |
| CFC cooling tube            | Toreyca T700C [21]       |
| Cooling tube extension      | SUS316                   |
| Cooling tube adhesive       | Henkel LOCTITE 9396 [20] |

197 The mechanical attachment of both edges of the stave comprise the end caps, SUS316 cooling-tube extensions,  
 198 and pairs of pin receptacles manufactured by Mill-Max MFG Co. for grounding. The endcap is made of Ketron CA30  
 199 PEEK [16] manufactured by Mitsubishi Chemical Co. The stainless tubes and the cooling tubes were glued using  
 200 Henkel LOCTITE EA 9396 adhesive [20]. The rest of the stave pieces are assembled using the graphite conductive  
 201 EP75-1 epoxy adhesive (MasterBond Co.) [15]. Figure 11 and Figure 12 show the photo and the engineering drawing  
 202 of the INTT stave. Table 8 summarizes the material list of stave components and specifications.



**Figure 11:** The photo of the INTT staves.



**Figure 12:** The INTT stave drawings from four different view angles. The HDI is assembled on the bottom flat CFC plate.

203 The staves were fully fabricated by Asuka Co., Ltd., Japan, including the baking process of the CFC plates. To  
 204 ensure meeting the requirements, the following four tests were applied to staves and to every cooling tube (after the  
 205 stainless extensions were glued). Only components that passed examination were used.

**Table 9**

The material budget of the silicon ladder. TC-2810 is the thermally conductive glue. The radiation thickness of the HDI listed in the table is for production batches 1 and 2.

| Item           | Thickness<br>mm | Radiation Length<br>$X/X_0$ % |
|----------------|-----------------|-------------------------------|
| Silicon Sensor | 0.32            | 0.34                          |
| Silver epoxy   | 0.01            | 0.02                          |
| HDI            | 0.42            | 0.43                          |
| TC-2810        | 0.05            | 0.02                          |
| Stave          | 3.76            | 0.33                          |
| Total          | 4.56            | 1.14                          |

**Table 10**

The effective thickness of the HDI's copper layers.

| Layer | Function    | Residual copper<br>fraction % | Effective<br>thickness $\mu\text{m}$ |
|-------|-------------|-------------------------------|--------------------------------------|
| 1     | Bias + AGND | 71.3                          | 17.1                                 |
| 2     | AGND        | 93.5                          | 8.42                                 |
| 3     | Signal      | 6.5                           | 0.59                                 |
| 4     | Power       | 94.0                          | 8.64                                 |
| 5     | Signal      | 7.2                           | 0.65                                 |
| 6     | DGND        | 93.2                          | 8.38                                 |
| 7     | Bias+Signal | 4.7                           | 1.12                                 |
| Total |             |                               | 44.7                                 |

- 206 1. Burst test : Tube does not burst for 1 hour at  $60 \pm 2$  psi
- 207 2. Leak test : less than 0.2 ml-mbar/min
- 208 3. Heat-cycle test :  $40 \leftrightarrow 0^\circ\text{C}$  (one cycle)
- 209 4. Flatness  $< 100 \mu\text{m}$  of the flat side of the stave and alignment positions are within specified tolerance

210 The staves were assembled with only those cooling tubes that passed the 1 and 2 examinations to keep the yield  
211 rate of the stave production reasonably high. The assembled staves were then examined for the above items 3 and 4.

### 212 3.5. Material Budget

213 Table 9 summarizes the material budget of the silicon ladder. The total thickness of the silicon pad area of the  
214 ladder is 4.57 mm and its effective radiation length  $X/X_0$  is 1.14%. The largest contributions to the budget is the  
215 HDI (with radiation length is  $X/X_0 = 0.43\%$ ), and the silicon and staves with radiation lengths  $X/X_0 = 0.34\%$  and  
216  $X/X_0 = 0.33\%$ , respectively.

217 The material budget of the HDI is largely governed by the copper layers. As shown in Fig. 7, there are 7 layers of  
218  $9 \mu\text{m}$  thick copper which total  $63 \mu\text{m}$ . Furthermore, both top and bottom surface layers are plated with  $15 \mu\text{m}$  thick  
219 copper<sup>2</sup>. While the simple stack up of these copper sheets results in  $93 \mu\text{m}$ , the effective amount of copper in the signal  
220 layers is much less than solid ground layers.

221 Table 10 summarizes the effective copper thickness of each layer, which was estimated based on the residual copper  
222 fraction after the etching process of the HDI fabrication. The effective total thickness is estimated to be  $44.7 \mu\text{m}$ ,  
223 approximately 48% of the  $93 \mu\text{m}$  total stack-up thickness, with corresponding radiation length  $X/X_0$  is 0.31%. The  
224 total thickness of polyimide and glue layers is  $325 \mu\text{m}$  with  $X/X_0$  of 0.11. The total radiation length of the HDI in the  
225 silicon pad area is thus 0.43%.

<sup>2</sup>The thickness of the copper plate was  $20 \mu\text{m}$  only for the last production batch, which increases the radiation length of the third batch HDIs by  $X/X_0 = 0.02\%$ .

**Table 11**

The dimensions of the dead space and region in the longitudinal direction of the half ladder.

| Longitudinal                               | Physical | Active   |
|--|----------|----------|
| Dead space I                               | 0.5 mm   | 0 mm     |
| Type-A                                     | 130 mm   | 128 mm   |
| Dead space II                              | 0.2 mm   | 0 mm     |
| Type-B                                     | 102 mm   | 100 mm   |
| Total                                      | 132.7 mm | 228.0 mm |
| The fraction of longitudinal active length |          | 98.0%    |

**Table 12**

The physical and active area of the half ladder.

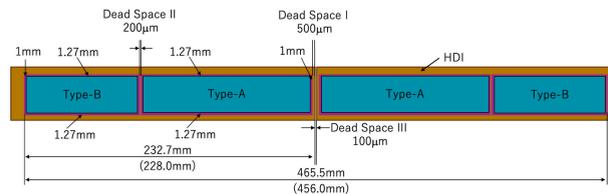
| Transverse                               | Physical | Active    |
|--|----------|-----------|
| Type-A & B                               | 22.5 mm  | 19.968 mm |
| The fraction of transverse active length |          | 88.7%     |

226 The silicon sensors were glued on the bias pads of the top layer of the HDI using electrically conductive silver  
 227 epoxy, i.e. Henkel LOCTITE ABLESTIC 2902 adhesive. The average thickness of the epoxy was designed to be  $9 \mu\text{m}$   
 228 based on the  $50 \mu\text{m}$  thick glue mask, which has total of 295 glue potting holes with 2 mm diameter each. The radiation  
 229 length of the silver epoxy was then calculated to be  $X/X_0 = 0.02\%$  based on the mixing ratio of the silver powder and  
 230 the epoxy of 0.21:0.79 [19]. Due to the short radiation length  $X_0 = 8.54 \text{ mm}$  of the silver material, the contribution  
 231 of the silver epoxy to the total material budget can be non-negligible. Without the glue mask, the contribution of the  
 232  $50 \mu\text{m}$  thick silver epoxy is as significant as 12% of the total material budget.

233 To diffuse the heat generated by the FPHX chips, highly thermally conductive epoxy adhesive glue, 3M<sup>TM</sup> TC-  
 234 2810 [1], was used to assemble the HDI and the stave. The radiation length for the  $50 \mu\text{m}$  thick the epoxy makes a very  
 235 small contribution to the total material budget of the silicon ladder, unlike the silver compound one.

### 3.6. Dead Space

237 Due to the precision limit of the silicon sensor alignment during the assembly process of the silicon sensors on the  
 238 sensor pads of the HDI, there are small dead spaces between the edge of the type-A sensor and the tip of the HDI (dead  
 239 space I), and also the type-A and type-B sensors (dead space II). They are 0.5 and 0.2 mm, respectively, as shown in  
 240 Figure 13.



**Figure 13:** Dead spaces of the INTT ladder. The number in parentheses is the longitudinal length of the active region of the type-A and B sensors altogether.

241 As the result of the dead spaces in the silicon alignment, the total distance from the boundary of the two half ladders  
 242 to the large rapidity end of the type-B sensor is 232.7 mm, while the length of the active region of type-A and type-B  
 243 sensors is 228.0 mm as tabulated in Table 3. This results in 98% coverage of the active region in the longitudinal  
 244 direction as summarized in Table 11. On the contrary, there is no additional dead space originating from the alignment  
 245 in the transverse direction. The fraction of the active region in the transverse direction is thus 88.7% as tabulated in  
 246 Table 12. The resulting fraction of the active area of the half ladder is 87.0% as tabulated in Table 13.

**Table 13**

The physical and active region of the half ladder.

|                             | Physical                | Active                  |
|-----------------------------|-------------------------|-------------------------|
| Area                        | 5235.75 mm <sup>2</sup> | 4552.70 mm <sup>2</sup> |
| The fraction of active area | 87.0%                   |                         |

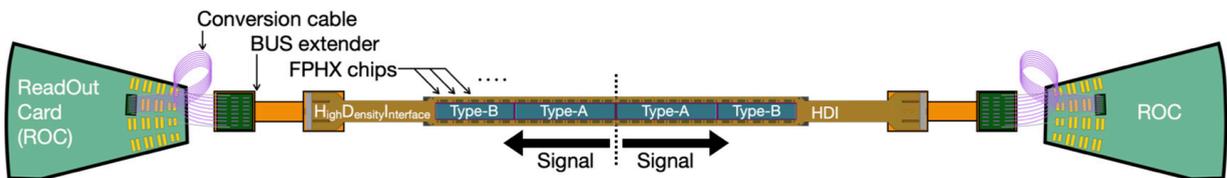
247 Lastly, there is another 0.1 mm of dead space between two half silicon ladders (Dead Space III in Figure 13)  
 248 originating from the alignment precision of the two half silicon modules on the stave. The resulting physical length  
 249 between the large rapidity end of the type-B sensors of two half ladders is 465.5 mm, while the total longitudinal length  
 250 of the active regions of 4 silicon sensors is 456.0 mm. This dead space is relatively minor enough, the fraction of active  
 251 area still stays as 98.0% in the longitudinal direction for the full ladder.

252 **4. INTT Readout Cables and Front End Circuit Board**

253 Because the entire INTT barrel must fit within the inner diameter of the TPC detector [3], the signal from the  
 254 barrel must be transmitted all the way to the outside of the TPC volume. The ROCs from the FVTX detector, which  
 255 are downstream electronics for signal processing, cannot fit within the inner diameter of the TPC.

256 Massive raw data generated from the INTT must be transmitted at high-speed to the ROC through a curved cable  
 257 path for longer than 1 m. Because no commercial cable satisfies the requirements, a novel bus-extender cable was  
 258 developed based on the FPC. This technology simultaneously satisfies the requirements of high-density signal lines,  
 259 flexibility, and long cable length. In contrast, the specification of line and space of the bus extender prevented its  
 260 connector-end design to be compatible with the input connector ports of the existing ROC. Therefore, another 15 to  
 261 25 cm conversion cable was developed to interconnect between the bus extender and the ROC. Flexibility in three-  
 262 dimensions for the conversion cable is required to guide the connection smoothly without introducing any stress at the  
 263 ROC input connector. This is needed to absorb the geometrical mismatch of the downstream end of the bus extender  
 264 and the corresponding input connector location of the ROC.

265 The schematics of the INTT silicon ladder and full readout cable chain up to the ROC is depicted in Fig. 14. The  
 266 data of each half ladder is readout from opposite side of the full ladder and processed by different ROCs.



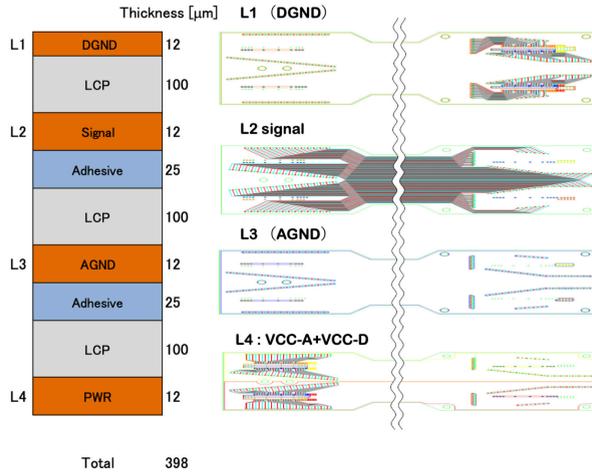
**Figure 14:** The schematics of the INTT silicon ladder and full readout cable chain up to the ROC.

267 **4.1. Bus Extender Cable**

268 Only key features of the bus extender (BEX) are described here, because details of the BEX cable are discussed  
 269 elsewhere [14]. This FPC cable comprises four layers of three flexible-copper-clad laminate (FCCL) as shown in  
 270 Fig. 15. The top and third layers are for the digital and analog grounds, respectively. The second layer is used for signal  
 271 lines. The bottom layer has the power supply lines for the FPHX chips. The choice of the four-layer structure, instead  
 272 of the seven-layer structure of the HDI, is primarily driven by fabrication constraints. The yield rate is a big concern  
 273 for the BEX. The main driver is the signal layer due to its required microfabrication accuracy over the extraordinary  
 274 length of 1.11 meters. Reducing the number of signal layers was chosen to minimize the risk in the fabrication process.  
 275 All of the BEX signal lines were thus integrated into a single layer.

276 Polyimide is the most popular market choice of a dielectric material for the FPCs and its fabrication technology  
 277 is well established in industry. For the BEX case, liquid crystal polymer (LCP) was chosen as the dielectric material

## INTT Silicon Ladder for sPHENIX



**Figure 15:** Four layer structure of the BEX (left), and schematics of each conductive layer (right) from L1 to L4.

**Table 14**

Specifications of the BEX cable.

| Item                       | Specification         |
|----------------------------|-----------------------|
| Dimension                  | 1.11 m × 34 mm        |
| Width (connector region)   | 43 mm                 |
| Total thickness            | 398 μm                |
| Dielectric material        | LCP                   |
| Dielectric model           | Panasonic FELIOS [18] |
| Dielectric layer thickness | 100 μm                |
| Bonding sheet thickness    | 25 μm                 |
| Number of layers           | 4                     |
| Number of signal lines     | 122                   |
| Line and space             | 130 & 130 μm          |

278 due to its lower transmission loss of signal amplitude and the availability of thicker FCCLs in the industrial market  
 279 compared to polyimide. These features are advantageous for the bus extender, whose design is strictly constrained by  
 280 the precision and yield limit in the fabrication process due to its extraordinarily long length.

281 The realistic limit of the line and space for the BEX were both found to be 130 μm. To achieve a reasonable yield  
 282 rate in the fabrication factory, which was Printed Denshi Kenkyusho Co., Ltd. Given the line and space, the thickness of  
 283 the dielectric material is required to be as thick as 100 μm to match the differential characteristic impedance of 100 Ω.  
 284 While such a thick polyimide is not available in the industrial market, the 100 μm thickness is available in the FELIOS  
 285 model LCP from Panasonic Industry Co., Ltd. [18]. The key specifications of the LCP to make the low transmission  
 286 loss possible are the dielectric constant  $\epsilon_r = 3.3$  and the dissipation factor  $\tan \delta = 0.002$ .

287 For the bonding sheet, a specially optimized model for LCP was employed with thickness of 25 μm chosen for  
 288 having a low dielectric constant. As a consequence of R&D, this was also a crucial choice to achieve decent yield rate  
 289 in the through-holes plating process [14] by Taiyo Manufacturing Co., Ltd. because the fabrication technology for the  
 290 LCP is not as well established as for the polyimide. Table 14 summarizes the specifications of the BEX cable.

291 Pairs of DF18C-100DS-0.4V(81) receptacle connectors manufactured by Hirose Electric Co. Ltd. are implemented  
 292 at both ends of the bus extender as shown in Fig. 16. The space between a pair of DF18 plugs is 26 mm which is  
 293 incompatible with the 10 mm spacing of the input connector pair of the ROC. This extra spacing between the connector  
 294 pairs of the BEX is caused by the difficulty to wire 122 signal lines of 130 μm line & space into the short connector

**Table 15**

The performance of the BEX cable. The insertion loss and return losses are the performance at 200 MHz. The characteristic impedance is the differential of the LVDS pair.

| Item                     | Performance |
|--------------------------|-------------|
| Insertion Loss           | -2.7 dB     |
| Return Loss              | -23 dB      |
| Characteristic impedance | 90 $\Omega$ |

spacing. Due to the incompatibility of the connector layout between the BEX and the ROC, a conversion cable was introduced which converts the connector spacing from the BEX to the ROC spacing.



**Figure 16:** A photograph of the 1.11 meter long BEX cable.

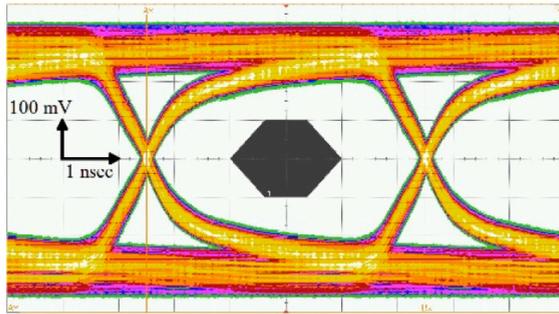
The bus extender successfully moderated the signal attenuation. However, the signal level is still questionable due to the extraordinarily long cable length as a multilayered FPC. The performance of signal transmission was evaluating with measurements using each of the following methods: 1) S-parameters, 2) eye-diagram, and 3) time-domain reflectometry (TDR). From the S-parameter measurement, the insertion and reflection losses are -2.7 and -23 dB, respectively at 200 MHz. The measured eye diagram is shown in Fig. 17. The waveform is confirmed to exhibit a sufficient margin to a defined mask<sup>3</sup> by observing 1 million waveforms of the 200 MHz signal (see the solid hexagon in the middle of Fig. 17). The measured characteristic impedance was 90  $\Omega$  differential in the TDR measurement. This is 10% smaller than the default 100  $\Omega$ , it is confirmed to be permissible by the return loss measurement of the daisy chain with the conversion cable as discussed in subsection 4.2. Table 15 summarizes the performance of the BEX cable.

#### 4.2. Conversion Cable

As discussed in previous sections, the FPC is the first choice of technology to satisfy the high-performance requirements of signal transmission, high signal-line density, and flexibility. However, it is difficult for the FPC to satisfy an additional and unique requirement as the last stage of the readout cable series. The requirement is flexibility in three dimensions to connect the downstream end of the BEX and the input connector ports of the ROC board without introducing any stress at the connection. Due to the geometrical mismatch between the INTT barrel ladders and the input connector layout of the ROC, flexibility in three dimensions is crucial for the conversion cable. If the FPC cable has directivity, then stress is induced at the connector end, which would bend the cable to the transverse direction of the cable plane.

A  $\mu$ -coax technology was chosen. Although the signal line density cannot be as high as the FPC, the three dimensional flexibility offers a good trade-off in the INTT readout design. According to an engineering study, due to its

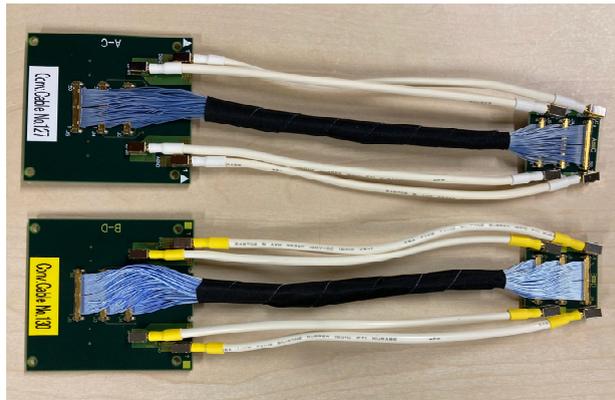
<sup>3</sup>Private communication with the FPHX chip developers.



**Figure 17:** The measured eye-diagram of the BEX as a result of transmitting 200 MHz signals for 1 million times [14].

318 lack of flexibility the FPC solution would require as many as 14 different designs in curving and length to interconnect  
 319 mismatching connector geometries between the BEX and input connectors of the ROC. Furthermore, spare cables of  
 320 all designs would be needed for risk management, which leads to high cost inefficiency. The  $\mu$ -coax solution reduces  
 321 the number of designs to be only two in different lengths.

322 The CABLINE-UX II model manufactured by I-PEX Inc. [12] was employed as the last stage of the signal  
 323 transmission cable chain for the INTT ladder. The AWG#44 harness is made of silver-plated copper alloy with a center  
 324 conductor insulated by  $30\mu\text{m}$  thick perfluoroalkoxy alkane (PFA) dielectric material from tinned copper alloy with wire  
 325 wrapping in the outer spiral shield. The shield is covered by the outermost jacket made of the PFA, as well forming a  
 326 four-layered coaxial cable with total thickness of  $0.24 \pm 0.01$  mm. The characteristic impedance of the harness is  $45\ \Omega$   
 327 ( $90$  differential for a LVDS pair). A slim plug and small connectors are assembled for both ends of the harnesses to  
 328 bundle 50 harnesses in the wire spacing with  $0.25$  mm pitch. Finally, the harness bundle is wrapped by an acetate cloth  
 329 adhesive tape.



**Figure 18:** Conversion cable type-AC (top) type-BD (bottom). The bundles in the middle of the cable are 15 cm length  $\mu$ -coax harnesses with four white jacket cables for the power and ground cables. The larger PC board is the connector for the BEX side and the smaller board is for the ROC side.

330 The conversion cable interconnecting between the BEX and ROC comprises three  $\mu$ -coax bundles, two power and  
 331 two ground cables, and the PC boards in both ends. The AWG#24 power and ground cables in both ends are assembled  
 332 with HJ-3 male pins manufactured by MAC EIGHT Co. Ltd.. The male pin and the receptacle connection are secured  
 333 by the HH-3-R lock. The wire gauge is optimized to be AWG#24 to drop the voltage properly and to provide the FPHX  
 334 chip power from the slightly higher regulator voltage output at the ROC. Details of the voltage drop is discussed in  
 335 Section 4.3.

336 Three UX II receptacles and four HH-3-G sockets (manufactured by MAC EIGHT Co. Ltd.) are implemented on  
 337 the top side of the PC board and two DF18C-100DS-0.4V(81) receptacle connectors are implemented on the bottom

**Table 16**

Specifications of the conversion cable. The characteristic impedance is given in differential of the LVDS pair.

| Item                         | Specification     |
|------------------------------|-------------------|
| $\mu$ -coax make             | I-PEX Inc.        |
| $\mu$ -coax model            | CABLIN-UX II [12] |
| Harness AWG                  | 44                |
| Characteristic impedance     | 90 $\Omega$       |
| Number of harness per bundle | 50                |
| Number of bundle             | 3                 |
| Power/ground cable AWG       | 24                |
| Number of power cable        | 2                 |
| Number of ground cable       | 2                 |
| Length                       | 15 & 25 cm        |

338 side of the board. The PC board is fabricated by Hayashi-REPIC Co. Ltd. and eight layered with dedicated layers for  
 339 the digital and the analog-power and ground. The dimensions are 48 mm wide  $\times$  52 mm long for the BEX end to match  
 340 the size of the connector end, while the ROC side is rather compact with dimensions 25 mm wide  $\times$  25 mm long. There  
 341 are two types of conversion cables namely "type-AC" and "type-BC" and the difference is so the channel mapping is  
 342 compatible with the channel map, which are differently designed for the columns A&C and B&D of the input ports  
 343 on the ROC. There are two different lengths of harnesses for the power and ground cables, which are 15 and 25 cm,  
 344 respectively.

### 345 4.3. ROC

346 The readout card (ROC) is a multilayered circuit board implemented outside of the TPC volume. The ROCs were  
 347 refurbished after the FVTX operation in the PHENIX experiment and reused for the INTT. ROC details are described  
 348 elsewhere [4]. Any aspects of ROC usage that are different from the FVTX or customized for sPHENIX are discussed  
 349 below.

350 Twelve pairs of DF18C-100DP-0.4V(51) plug connectors and four pairs of DF18C-60DP-0.4V(51) are imple-  
 351 mented in the ROC as input ports for a half ladder. The DF18C-60DP-0.4V(51) plug connector has 60 pins and is not  
 352 used for the INTT.

353 The ROC boards are originally implemented with 2.5 V regulators to provide analog and digital power for the FPHX  
 354 chips with an operating voltage of 2.5 V for both analog and digital [11, 13, 23]. The voltage drop in the power-transfer  
 355 line was minor in the FVTX owing to the short readout-cable length and low power consumption of the FPHX chip.  
 356 On the contrary, as has been discussed in the previous sections, the INTT operates in the higher-power consumption  
 357 mode due to its extraordinarily long readout cable chain. The FPHX operates with higher LVDS current for output data  
 358 transmission than do the FVTX chips so that the signal amplitude is kept well above the receiver driver threshold.

359 The maximum drawing current per half ladder (26 FPHX chips) for the analog and digital power of the FPHX  
 360 chips is measured to be 0.21 and 0.42 amps, respectively. Although the ROC are designed to allocate reasonably large  
 361 physical cross sections or american wire gauge (AWG) for the power transmission lines, the resistances of these cables  
 362 is a few hundred m $\Omega$ . The resulting voltage drop of the daisy chain of the readout cables amounts to as much as 0.2  
 363 to 0.4 V which is sizable enough for the FPHX chips to possibly malfunction due to insufficient voltage supply.

364 To compensate for the voltage drop, the surface mounted regulators for the FPHX power are upgraded to  
 365 supply larger output voltages. The pin layouts of the upgraded regulators match the pad pattern of the ROC. Newly  
 366 implemented regulators are MCP1700-2802E/TT and MCP1726-3002E/MF (Microchip Technology Inc.) with outputs  
 367 of 2.8 and 3.0 V for analog and digital power, respectively. With drawing currents increased for higher voltage outputs,  
 368 the supplied voltages at the FPHX location are calculated to be  $\approx$  2.5 to 2.6 V for both analog and digital.

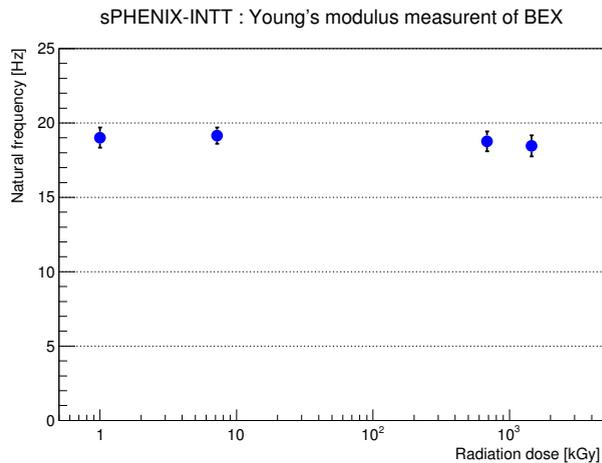
## 369 5. Radiation Hardness

370 In the INTT readout system (see Section 4), there are a few materials for which radiation hardness is either not  
 371 known or known to be not durable. In this section, the radiation hardness is evaluated for these items. Also discussed  
 372 is the study of the potential radiation damage of the ROC boards during the preceding PHENIX operation.

## 5.1. Bus Extender

The FPC with standard polyimide is widely used in radiation environments and its radiation hardness is well established. However, because LCP is a relatively new material being used for the dielectric layer of the FPC, the radiation hardness of the FPC with LCP has not been established as well as that of the polyimide. The radiation hardness of the LCP material itself is proven to be as durable as polyimide [22] although, the radiation hardness of the bonding sheet employed for the BEX was not known. The overall mechanical characteristics of the BEX after assembly was measured before and after a radiation exposure rather than investigating the radiation hardness of the bonding sheet itself. The primary concerns are the degradation in the flexibility of the BEX and the peel strength of the bonding sheet due to radiation damage.

A few samples of the BEX cable were exposed to  $^{60}\text{Co}$  source for 7.2 kGy, 685 kGy, 1.45 MGy at National Institutes for Quantum Science and Technology, Japan. The expected radiation dose at the location where the BEX is installed in sPHENIX is approximately 5 kGy for five years operation<sup>4</sup>. The mechanical performances were evaluated by the following two tests: 1) stress test to evaluate the flexibility, and 2) peel strength test between the copper and the LCP layers [14]. As the test item 1), the Young's modulus was measured for the samples before and after the radiation exposure. Figure 19 shows the Young's modulus of these samples based on natural frequency measurements. No degradation of flexibility was observed within the accuracy of the measurements (7%) in any samples. The error was estimated by the standard deviation of multiple samples within the same radiation dose group.



**Figure 19:** The Young's modulus measurement results of samples exposed to various radiation dose. The vertical axis is the natural frequency in the unit of Hz, while the horizontal axis is the radiation dose in the unit of kGy. The measurement of the sample with no radiation exposure is plotted purposely at 1 kGy.

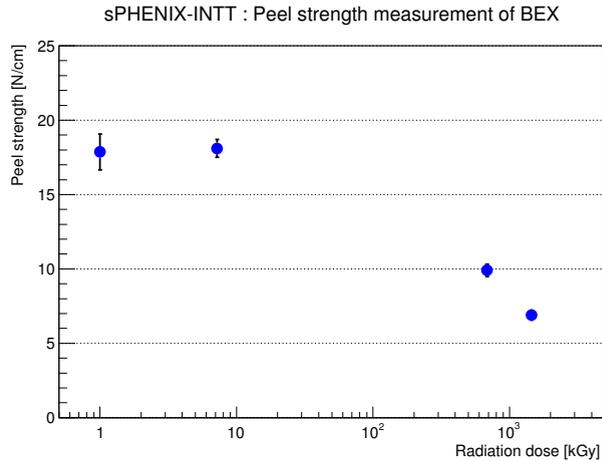
For test item 2), approximately 50% and 70% degradations were observed in the peel strength for 685 kGy and 1.45 MGy samples, respectively as shown in Fig. 20. However, the measured peel strength of 18 N/cm for the 7.2 kGy sample proved to be sufficiently strong and is similar to the typical level of polyimide-based FPC. Although the safety margin to keep this peel strength for possible unexpected extra radiation dose may be marginal, it is unlikely that FCCL layers would fall apart by gravity even if the peel strength were weakened by 50%. It was thus concluded that the radiation hardness of the BEX is expected to be durable for the duration of sPHENIX operation.

## 5.2. Conversion Cable

The material "fluorinated resin", which is used as a dielectric insulator for the  $\mu$ -coax cable [12], is reported to be weak against radiation [22] compared to popular dielectric insulator materials like polyimide or LCP. The estimated equivalent neutrons at the location of conversion cables to be installed is  $0.15 \times 10^{12}$  for three years of sPHENIX operation.

In order to address the radiation hardness of the  $\mu$ -coax harness for three years of sPHENIX operation, the effect of radiation was studied at the RIKEN Accelerator-driven compact neutron systems facility (RANS), Japan. Three

<sup>4</sup>Including an extra two years of operation beyond the officially approved three years.



**Figure 20:** The peel strength measurement results of samples exposed to various dose radiation doses. The vertical axis is the peel strength in units of N/cm, while the horizontal axis is radiation dose in units of kGy. The measurement of the sample with no radiation exposure is plotted at 1 kGy on purpose.

403 samples of harness bundle were exposed to the RANS neutron beam at energies up to 5 MeV. Each sample was  
 404 exposed to  $1.3, 2.6,$  and  $4.0 \times 10^{12}$  equivalent neutrons. These are factors of 9, 17, and 27, respectively, more than the  
 405 estimated radiation dose for the INTT operation in sPHENIX. The signal transmission performances were compared  
 406 before and after the irradiation to evaluate the radiation effect. The comparisons were made for the S-parameters, the  
 407 eye diagrams, and the TDR. No degradation was observed for all samples in any of these measurements, regardless  
 408 of the exposed radiation dose. Thus, it is reasonable to conclude that the radiation hardness of the conversion cable is  
 409 durable for the INTT operation as well.

### 410 5.3. ROC

411 The radiation dose of the ROC boards throughout five years of operation of the FVTX detector in PHENIX is  
 412 estimated to have been approximately 300 Gy, while the corresponding radiation dosage for three years of the INTT  
 413 operation in sPHENIX is estimated to be approximately 50 Gy. The dose for the INTT is moderate owing to the  
 414 relatively farther distance of the ROC position from the collision point compared to that of the FVTX in PHENIX.  
 415 Here the radiation hardness of the ROC board with respect to the total dose of 350 Gy is evaluated.

416 The ROC board is designed to be radiation hard and in fact it utilizes the FLASH-based ACTEL ProASIC3E  
 417 FPGAs [4] which is known to be radiation hard. The optical data transmission system of the ROC board comprises the  
 418 model TLK2711 (Texas Instruments) as the serializer/deserializer of data. There is a study of the radiation tolerance  
 419 of the TLK2711 [5]. In this study, the increase of leakage current and the bit-error rate was monitored as a function of  
 420 radiation dose. The first bit error appeared  $\approx 280\text{--}420$  Gy and the TLK2711 encountered functional failure as low as  
 421 700 Gy depending on the beam condition of the radiation exposure, e.g., high (low) intensity and short (long) duration.  
 422 While the leakage current stays the same up to 400 Gy, a rather rapid increase of current was observed beyond that  
 423 point.

424 According to the above study, the condition of the TLK2711 are already in the range that some bit error symptom  
 425 may start after the FVTX use. Although it was preferable to replace them all before the reuse for the INTT, the model  
 426 was discontinued. Unfortunately, insufficient quantities were available in the market place to replace them all. Hence,  
 427 the replacement candidates are prioritized and limited to only those which already have bit-error symptoms. The only  
 428 ROCs installed are those which passed the various function tests including no bit-error symptoms.

## 429 6. Summary

430 A new silicon-strip detector was developed for the sPHENIX experiment at RHIC. The silicon ladder consisted of  
 431 silicon-strip sensors, FPHX chips, HDIs, and a high thermally conductive carbon-fiber stave. The ladder was designed  
 432 to be as thin as  $X/X_0 = 1.14\%$ . The bus extender and the conversion cables were developed to transmit signals from the

ladder to the ROC board. The 1.11 m long bus extender cable employs the novel low attenuation LCP as the dielectric material of the FPC. The conversion cable employs  $\mu$ -coaxial harnesses to secure flexibility in three dimensions in order to connect the bus extender end to the input/output ports of the ROC board without introducing any stress at the connection.

The result of the study indicated that both the bus extender and the conversion cables are sufficiently radiation hard against estimated radiation dose for three years of the INTT operation in the sPHENIX experiment. In contrast, the exposed dose for TLK2711 chips of the ROC board throughout five years of the FVTX operation in the PHENIX experiment caused some bit errors to start to appear. Any chips showing these symptoms were replaced with new chips. The ROCs are installed relatively far away from the collision point for INTT operation in sPHENIX as opposed to FVTX in PHENIX. Thus, the radiation dose for the ROC boards in three years of INTT operation in sPHENIX is estimated to be relatively moderate, i.e. 1/6 of that of the FVTX in PHENIX.

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